Experimental analysis of an MIM capacitor with a concave shield

Liu Lintao(刘林涛)†, Yu Mingyan(喻明艳), and Wang Jinxiang(王进祥)

(Microelectronic Center, Harbin Institute of Technology, Harbin 150001, China)

Abstract: A novel shielding scheme is developed by inserting a concave shield between a metal–insulator–metal (MIM) capacitor and the silicon substrate. Chip measurements reveal that the concave shield improves the quality factor by 11% at 11.8 GHz and 14% at 18.8 GHz compared with an unshielded MIM capacitor. It also alleviates the effect on shunt capacitance between the bottom plate of the MIM capacitor and the shield layer. Moreover, because the concave shields simplify substrate modeling, a simple circuit model of the MIM capacitor with concave shield is presented for radio frequency applications.

Key words: MIM capacitor; concave shield; quality factor; model
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1. Introduction

MIM capacitors are very important passive components used in DC decoupling, biasing circuits, low noise amplifiers (LNA) and oscillators. Some papers aim to reduce signal injections into the Si substrate when a MIM capacitor is used in mixed-signal and RF design. A shield layer connected to ground is designed under the bottom plate of the MIM capacitor[1, 2]. Chip measurements reveal that these techniques can reduce cross-talk through the substrate[2]. For the 1P6M CMOS process, metal 4 is close to the bottom plate of the MIM capacitor, so the shield layer should be designed by metal 4 to isolate the substrate effectively[3]. However, a plane shield between the MIM capacitor and substrate still allows image currents to flow, which can degrade the overall Q factor[3]. Another significant drawback of using the plane shield is the decrease in self-resonant frequency (SRF), which results from the increase in shunt capacitance between the bottom plate of the MIM capacitor and the ground shield plane[4].

A shield layer can be patterned in-plane with breaks that are perpendicular to the direction of image current flow[5]. The use of such patterned ground shields (PGS) is attractive because losses and cross-talk are both reduced. It improves the Q value because PGS avoids magnetically induced current flow and provides a low-resistance return path to RF ground. However, this structure is only suitable for on-chip inductors because MIM capacitors and on-chip inductors have different directions of image current flow.

To solve this problem, a concave shield structure is discussed in this paper. An MIM capacitor with a concave shield is fabricated in the 1P7M CMOS process, and the concave shield is inserted between the MIM capacitor and the silicon substrate. Experiments are carried out to study the effects of the concave shield on Q factor, parasitic capacitances and main capacitance compared with an unshielded MIM capacitor. In addition, results for a conventional plane shield are compared to demonstrate the effectiveness of the concave shield structure in alleviating parasitic capacitances. An on-wafer testing technique and a parameter extraction procedure are presented. Moreover, concave shields simplify substrate modeling. A simple circuit model of the MIM capacitor with a concave shield is presented for RF application.

2. Design consideration

In mixed-signal and RF circuit design, coupling noise has a significant effect on the analog circuit performance. Thus, a shield layer between sensitive circuit blocks is a crucial design issue. To enhance the shielding effect, the shield layer of an MIM capacitor should be in contact with the ground metal plane as close as possible to the bottom plate of the MIM capacitor. Metal 4 is therefore chosen as the shield layer because metal 4 is the nearest underground metal for the 1P6M CMOS process[3]. However, the quality factor does not show any improvement. According to Lenz's law, image current will be induced in the solid ground shield by the magnetic field of the MIM capacitor. This leads to energy loss in the MIM capacitor.

To improve the quality factor, the shield layer can be designed to be similar to PGS. However, image current flow is different between MIM capacitors and on-chip inductors. The image current will flow in a direction opposite to that of the current in a MIM capacitor. So, the shield should be designed with different structures to terminate electric field.

Another important factor is the parasitic capacitor between the MIM capacitor and the shield layer when the shield layer is designed. For the 1P6M CMOS process, metal 4 is chosen as the shield layer according to the previous discussion. However, metal 4 is not the optimum option for the parasitic capacitor between the MIM capacitor and the shield layer. Based on the formula of parallel-plate capacitors $C = \varepsilon S/4\pi kd$, metal 1 is better than metal 4. Therefore, there is a

† Corresponding author. Email: hgdllt@sina.com
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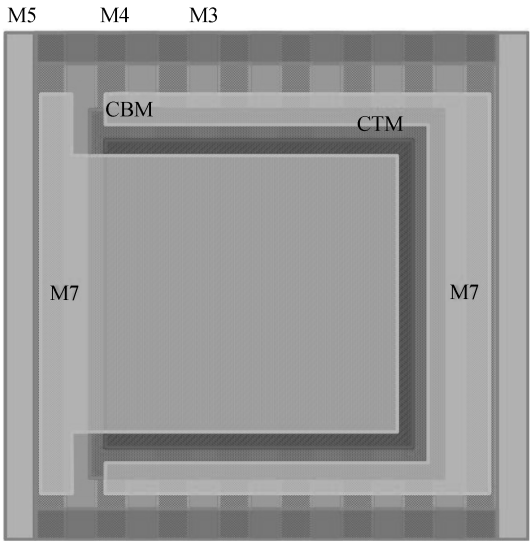

Fig. 1. Top view of MIM capacitor with concave shield.

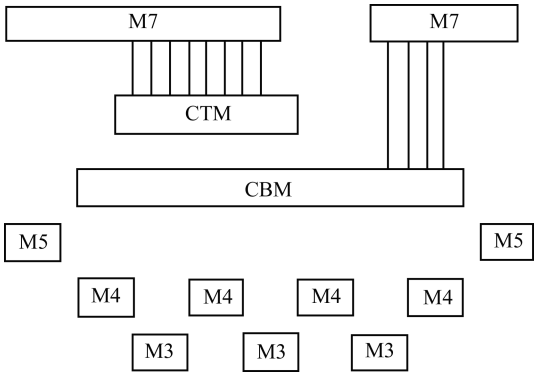

Fig. 2. Side view of MIM capacitor with concave shield.

trade-off when the metal layer is chosen as the shield layer.

3. Design of concave shield

In this section, an MIM capacitor with a concave shield, which has a two-port, parallel plate and square structure, is designed by the 1P7M CMOS process. The size of the MIM capacitor is $10 \times 10\ \mu m^2$. Top and side views of the proposed MIM capacitor are shown in Figs. 1 and 2 respectively.

In Figs. 1 and 2, the CTM is the top plate of capacitor, and the CBM is the bottom plate of capacitor. M3, M4, M5 and M7 are metal layers of metal 3, metal 4, metal 5 and metal 7 respectively. M3, M4 and M5 are all connected to ground. M7 is the top metal. CTM and CBM are connected separately to M7 by vias.

M5 is first chosen as the concave shield fringe because M5 is the nearest underground metal to the MIM capacitor for the 1P7M CMOS process. M4 and M3 are then arranged in a parallel direction which is perpendicular to the direction of image current flow. The whole concave shield (M3, M4 and M5) acts as an open circuit to cut off the path of the induced current. The concave shields are connected to ground by the top metal.

To investigate the effect of shield layout, a traditional MIM capacitor without a concave shield is fabricated. The

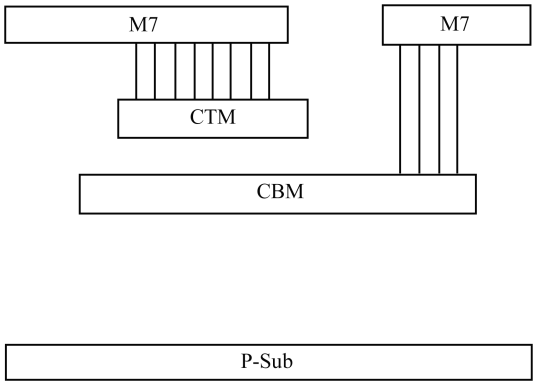

Fig. 3. Side view of MIM capacitor without concave shield.

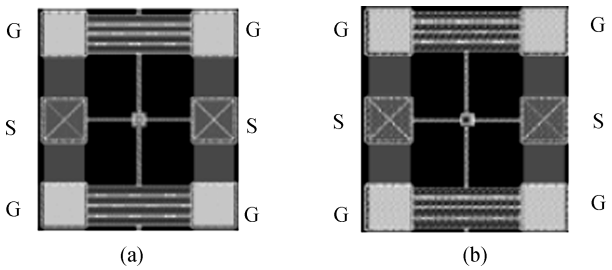

Fig. 4. GSG test structure of MIM capacitor (a) with concave shield and (b) without concave shield.

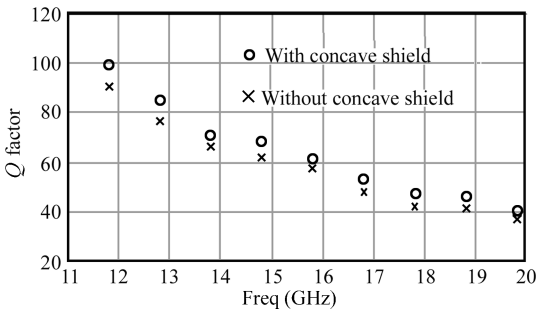

Fig. 5. Q factor of MIM capacitor.

only difference is that M3, M4 and M5 are not used. A side view of the MIM capacitor without a concave shield is shown in Fig. 3.

4. Experimental result

In order to measure the MIM capacitor, M7 is connected to RF pads to ensure measurement using GSG (ground signal ground) RF probes, as shown in Fig. 4. The open structure is also designed to perform de-embedding of measured capacitor scattering parameters.

The Q factor ($-\mathrm{Imag}(Y_{11})/\mathrm{Real}(Y_{11})$) is larger than that of the unshielded MIM capacitor in the frequency range from 11 to 20 GHz. As shown in Fig. 5, the Q factor increases by 11% at 11.8 GHz and 14% at 18.8 GHz respectively.

The C_{ox} ($-1/(\omega \mathrm{Im}\{Z_{21}\})$) is slightly larger than that of the unshielded MIM capacitor. However, the amount of increase is not significant. As a comparison, when only M4 is chosen as the shield layer, the C_{ox} of the MIM capacitor with a shield shows a significant improvement compared with that of the unshielded MIM capacitor[3], as shown in Table 1.

The circuit model of an MIM capacitor with a concave

Table 1. Comparison of C_{ox}.

MIM capacitor	C_{ox} (fF)
With concave shield	31.36
Without concave shield	27.36
With plane shield[3]	8.1
Without plane shield in shield[3]	1.3

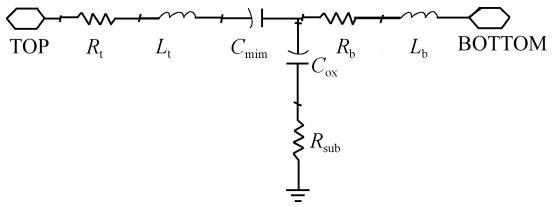

Fig. 6. Circuit model of MIM capacitor with concave shield.

shield is shown in Fig. 6. The circuit model is directly based on the design structure. In Fig. 6, C_{mim} is the main element of the capacitor. L_b represents the effects of the interlevel vias from M7 to CBM and L_t represents the effects of the interlevel vias from M7 to CTM. R_t and R_b are parasitics existing in the electrodes. Substrate modeling for passive components is a hard task. For our structure, the concave shield provides a well-defined RF ground reference, which is also simple to model. C_{ox} is the parasitic capacitance that represents the parasitics between the bottom metal plates and shield. For simplicity, we use only one resistor R_{sub} to model substrate resistance.

Two-port S-parameter data of the capacitors and pad frame were measured using a network analyzer and GSG RF probes. The S-parameter data were then converted to admittances. To de-embed the effects of the pad frame, admittances of the open structure were subtracted from the measured total admittances.

The following five equations are defined to calculate the values of the circuit model.

$$R_b = \mathrm{Re}\{Z_{22} - Z_{21}\},$$

$$R_t = \mathrm{Re}\{Z_{11} - Z_{21}\},$$

$$L_b = \frac{\mathrm{Im}\{Z_{22} - Z_{21}\}}{\omega},$$

$$C_{ox} = -\frac{1}{\omega \mathrm{Im}\{Z_{21}\}},$$

$$R_{sub} = \mathrm{Re}\{Z_{21}\}.$$

Other parameters in the circuit model are solved using random arithmetic and gradient arithmetic. Table 2 shows the extracted parameter values for the MIM capacitor. The total relative mean errors between the measured and the modeled Y-parameters of the proposed model are shown in Table 2.

The following equation was used to calculate total relative mean errors:

$$\mathrm{Error} = \frac{1}{4} \times \sum_{ij = 11, 12, 21, 22} \times \left[\left(\sum_{1}^{N_{freq}} \frac{|Y_{ij(\mathrm{measument})} - Y_{ij(\mathrm{proposed})}|}{|Y_{ij(\mathrm{measument})}|} \right) \times \frac{1}{N_{freq}} \right],$$

Table 2. Extracted parameters for MIM capacitor.

Parameter	MIM capacitor	
	Without concave shield	With concave shield
C_{mim} (fF)	116.7	116.7
R_t (Ω)	0.26	0.26
L_t (pH)	15	15
R_b (Ω)	1.15	1.15
L_b (pH)	0.44	0.44
C_{ox} (fF)	27.36	31.36
R_{sub} (Ω)	306	306
Error	2.2%	1.92%

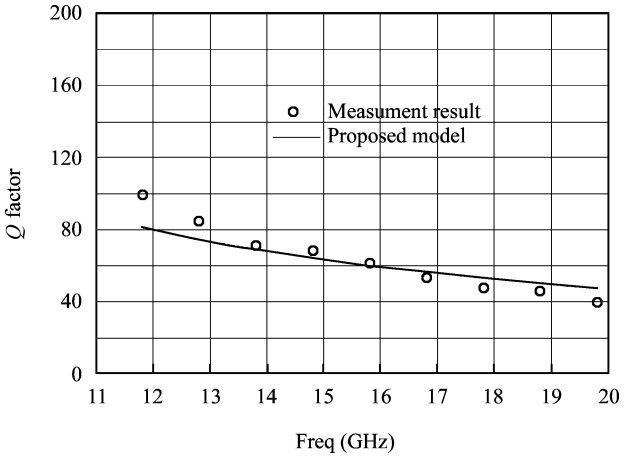

Fig. 7. Q factor of proposed model and measurement result.

where N_{freq} is the number of frequency points.

As shown in Table 2, the main capacitances C_{mim} are the same for the MIM capacitor with a concave shield and the MIM capacitor without a shield, which indicates that the concave shield has little effect on main capacitance. In Fig. 7, we compare the Q factor of the proposed model with that of measurements of the MIM capacitor with a concave shield.

5. Results and discussion

The experimental results suggest that a concave shield is a suitable structure for optimization of MIM capacitors. The concave shield improves the quality factor in the frequency range from 11 to 20 GHz and alleviates the effect on shunt capacitance between the bottom plate of the MIM capacitor and the shield layer. The Q factor increases by 11% at 11.8 GHz and 14% at 18.8 GHz respectively. Moreover, owing to a well-defined RF ground reference, cross-talk phenomena are inherently reduced. Lastly, a simple circuit model of the MIM capacitor with a concave shield is presented for RF applications because the concave shield simplifies substrate modeling. Another advantage is that no changes are made to the established CMOS process. The large silicon area under the MIM capacitor with a concave shield can potentially be used for the fabrication of other devices.

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