A 1-V 60-μW 85-dB dynamic range continuous-time third-order sigma–delta modulator*

Li Yuanwen(李渊文)[1,†], Qi Da(齐达)[1], Dong Yifeng(董一枫)[1], Xu Jun(许俊)[1], and Ren Junyan(任俊彦)[1,2]

(1 State Key Laboratory of ASIC & System, Shanghai 201203, China)

(2 Micro-Nanoelectronics Science and Technology Innovation Platform, Fudan University, Shanghai 201203, China)

Abstract: A 1-V third order one-bit continuous-time (CT) ΣΔ modulator is presented. Designed in the SMIC mixed-signal 0.13-μm CMOS process, the modulator utilizes active RC integrators to implement the loop filter. An efficient circuit design methodology for the CT ΣΔ modulator is proposed and verified. Low power dissipation is achieved through the use of two-stage class A/AB amplifiers. The presented modulator achieves 81.4-dB SNDR and 85-dB dynamic range in a 20-kHz bandwidth with an over sampling ratio of 128. The total power consumption of the modulator is only 60 μW from a 1-V power supply and the prototype occupies an active area of 0.12 mm^2.

Key words: analog-to-digital converter; continuous-time filter; low-power; low-voltage; sigma–delta modulation
DOI: 10.1088/1674-4926/30/12/125011 **EEACC:** 2570

1. Introduction

The market for portable electronic systems such as cellular phones, personal digital media, and battery-power medical devices is continuously expanding. Powered by batteries, low-power design is of great importance for these devices. Modern CMOS technology processes with their scaling feature sizes require a proportional reduction of the supply voltage. Low-voltage, low-power circuit techniques and system building blocks have thus become hot research topics recently.

An important performance limiting system building block is analog-to-digital converters (ADCs). Trading off the inevitable technology scaling and increasing stringent specifications of ADCs, one favorable option, especially in VLSI systems, is a ΣΔ ADC[1]. The traditional ΣΔ ADC is a discrete-time (DT) design utilizing switched-capacitor (SC) circuits. When moving into deep-submicron CMOS technologies, switches may fail to switch on or have considerable switch on resistance (R_{on}) under low supply voltages. Voltage boosting, low-V_T technology and a switched-opamp technique[2, 3] have been proposed to deal with low supply voltage problems in DT ΣΔ ADCs. But they have potential risks or need extra expensive processing steps, while in this design, a continuous-time (CT) third order loop filter is utilized to perform noise shaping instead of switched capacitor circuits. The use of a CT loop filter provides several advantages over SC implements. By eliminating switches within the loop filter, the CT ΣΔ modulator is very compatible with low supply voltages. A CT ΣΔ modulator operating from 0.5 V V_{DD} has been presented in Ref. [4]. The bandwidth requirements of the amplifiers in the CT ΣΔ modulator are relaxed compared with its DT counterparts[5, 11]. Moreover, the CT ΣΔ modulator has an inherent anti-aliasing function, which relaxes or even eliminates the demand on the preceding filter stage. Thus, power consumption is greatly reduced in the overall system.

In this paper, we present a single loop third-order CT ΣΔ modulator in SMIC mixed-signal 0.13 μm CMOS technology. A circuit design methodology for the CT ΣΔ modulator is proposed. Two-stage class A/AB amplifiers are adopted to optimize power consumption. The modulator achieves 81.4-dB SNDR and 85-dB dynamic range while consuming only 60 μW from a 1-V power supply.

2. Low-power third-order ΣΔ modulator

Extensive simulations in MATLAB show that a single-bit third-order modulator with an OSR of 128 can get a peak SNDR of 104 dB (Fig. 1), which is sufficient in this design. Due to its high power efficiency and low sensitivity, a chain of integrators with distributed feedback (CIFB) topology is adopted to implement the loop filter. The modulator topology is shown in Fig. 2, which also displays the dynamic scaling strategy. Active *RC* integrators are adopted to implement the CT loop filter. In active *RC* integrators, the coefficient for the

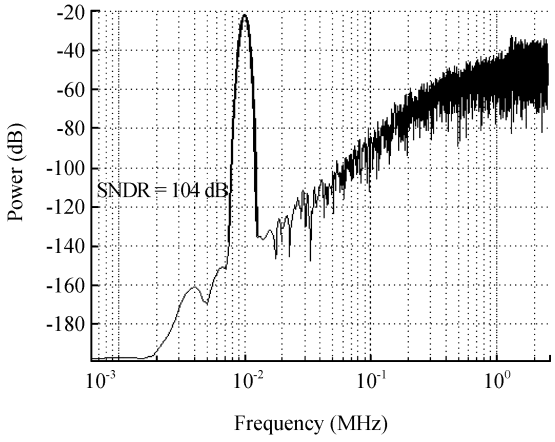

Fig. 1. Behavioral simulation for a single-bit third-order modulator with an OSR of 128.

* Project supported by the National High Technology Research and Development Program of China (No. 2008AA010702).
† Corresponding author. Email: 072021068@fudan.edu.cn
Received 4 May 2009, revised manuscript received 30 July 2009

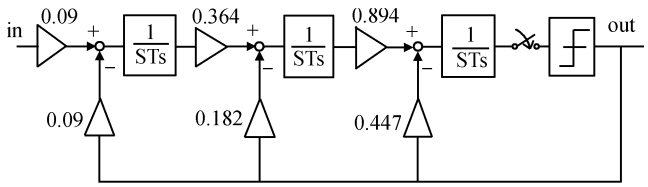

Fig. 2. Single-loop third-order CIFB topology.

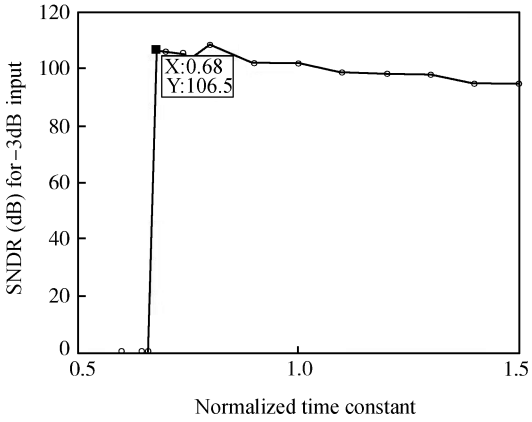

Fig. 3. SNDR versus normalized RC time constant.

transfer function is realized by the product of resistance R and capacitance C which are susceptible to processing variations. Careful system level simulation shows that the proposed modulator can sustain –32% to +50% RC variations without significant SNR degradation (Fig. 3). Time-constant tuning is thus not needed in the proposed robust topology.

3. Circuit implementation

3.1. Proposed circuit design methodology

One significant difference between CT and DT ΣΔ modulators is that the CT one integrates signal all the time, while the DT one integrates signal discretely. Thus, a DT ΣΔ modulator can be easily assessed and modified by observing the setting resolution of the SC circuits, while for a CT ΣΔ modulator one can only analyze its performance by the FFT result of the output data stream which requires a large simulation time. The traditional strategy for designing CT ΣΔ modulators is that designers analyze and improve the loop performance after all the circuit blocks have been designed. It is very difficult to locate the major design issues when performance degrades and it always leads to overdesign consuming much more power and area. We propose a methodology that builds a design-bench first where all the active circuit blocks are implemented with VerilogA models. The design-bench which has the ideal performance is used as a verification platform. Each active block replaces the corresponding VerilogA block after it has been designed. Simulation time is greatly reduced in this hybrid-model and modification in that exact circuit block is applied if SNR degrades severely. Thus, the design efficiency is greatly improved. As shown in Fig. 4, major building blocks in the proposed CT ΣΔ modulator include three amplifiers and a 1-bit quantizer. The VerilogA amplifiers in the design-bench were modeled with a DC gain of 80 dB, a GBW of 10 MHz and a

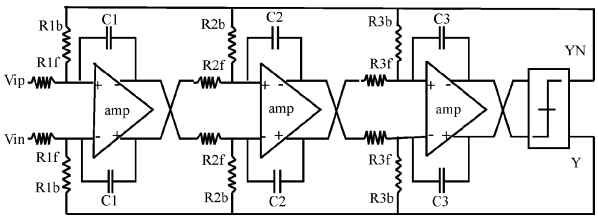

Fig. 4. Design-bench for the proposed CT ΣΔ modulator.

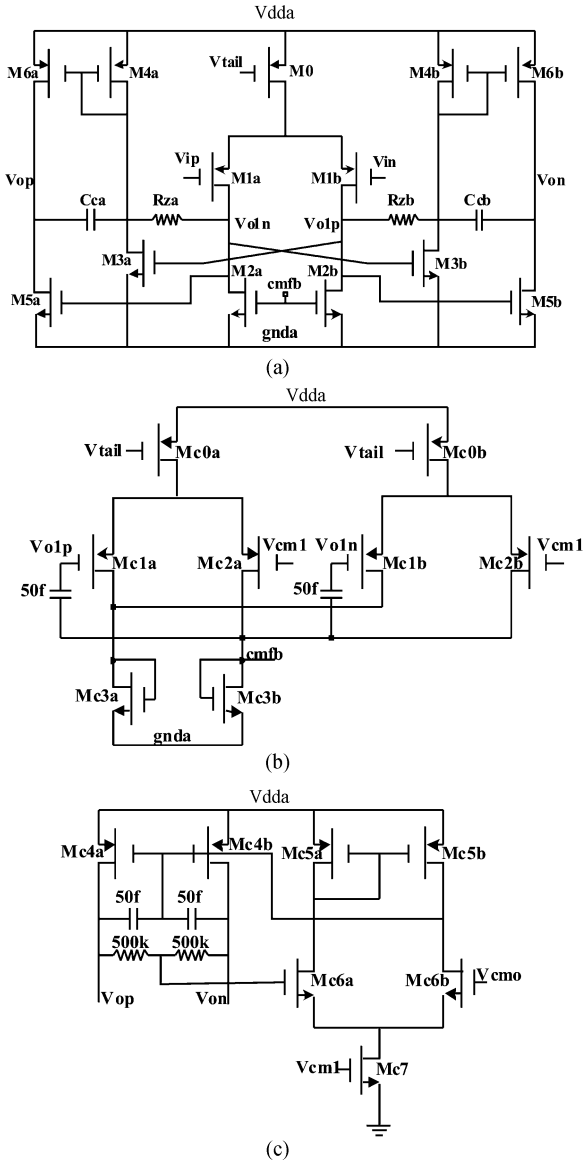

Fig. 5. Operational amplifiers used in the modulator: (a) Main amplifier; (b) Common-mode feedback (CMFB) for the first stage; (c) CMFB for the second stage.

slew rate of 10 V/μs. The following key blocks were designed and verified in this design-bench.

3.2. Operational amplifiers

The first operational amplifier has a dominant impact on modulator performance. The schematic of the opamp is shown in Fig. 5(a)[8, 9]. It is a two-stage class A/AB amplifier with Miller compensation resistor R_z and capacitor C_c. A long channel PMOS input pair M1a, b was used to lower the input-referred $1/f$ noise. Class AB output stage shows a good slew

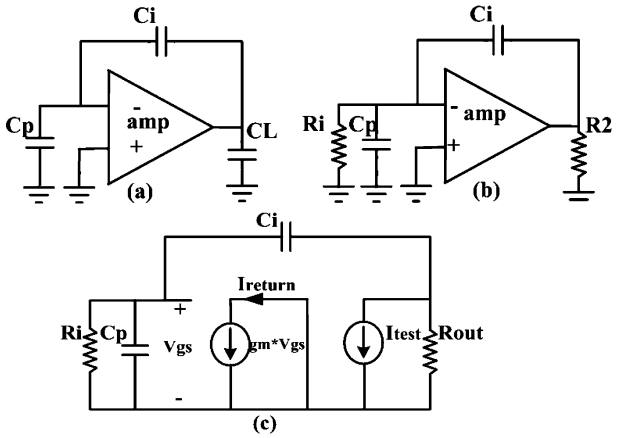

Fig. 6. (a) SC integrator during integration; (b) CT integrator during integration; (c) Small signal model for CT integrator in return ratio analysis.

rate performance which is very useful in large output swing CIFB topology. A drawback of class A/AB is that by using current mirrors in the second stage, the common-mode output voltage of the first-stage controls the currents in the second stage but does not affect the second-stage output voltage. Thus, two continuous-time common-mode feedback circuits are needed for both stages, schematics of which are shown in Figs. 5(b), 5(c)[9]. Since the voltage supply is 1 V, cascode transistors are avoided and all the transistors are biased with $V_{GS} - V_T$ from 60 to 90 mV.

The load of the opamp should be estimated before the opamp is designed. As in SC circuits, the effective load $C_{L,\text{eff}}$ can be calculated easily, during the integration phase in Fig. 6(a):

$$C_{L,\text{eff}} = C_L + \frac{C_i C_p}{C_i + C_p}, \tag{1}$$

where C_L is the load capacitance, C_i is the integrating capacitance, and C_p is the parasitic capacitance at the amplifier input node. For a CT integrator, it is difficult to gain the effective load; a simplified schematic is shown in Fig. 6(b), where R_i denotes the input feed-forward resistor and R_2 is the input feed-forward resistor of the next stage. As shown in the figure, the CT integrator's effective load is formed by a complex combination of resistors and capacitor. Return ratio analysis is adopted here to explore the effective load and investigate the stability issues. Taking one stage amplifier as an example, the simplified small signal model is shown in Fig. 6(c). The return ratio (loop gain) can be expressed as

$$T(s) = \frac{g_m R_{out} S C_i R_i}{1 + \left(1 + \dfrac{C_p}{C_i} + \dfrac{R_{out}}{R_i}\right) C_i R_i S + C_p R_{out} C_i R_i S^2}. \tag{2}$$

Assume that R_{out} and R_i have similar magnitudes, and integration capacitance C_i is much larger than input parasitic capacitance C_p. The two induced poles, thus, separate widely. The return ratio expression is simplified as:

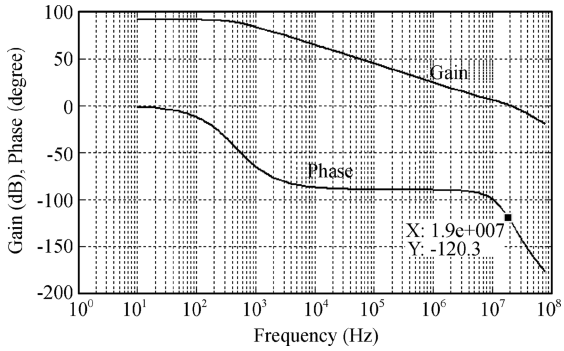

Fig. 7. Simulated class A/AB amplifier frequency response.

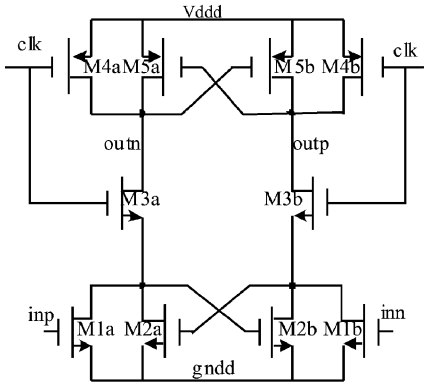

Fig. 8. Schematic of the quantizer.

$$T(s) = \frac{K g_m R_{out} \dfrac{S}{p_1}}{\left(1 + \dfrac{S}{p_1}\right)\left(1 + \dfrac{S}{p_2}\right)},$$

$$K = 1 + \frac{C_p}{C_i} + \frac{R_{out}}{R_i}, \quad p_1 = \frac{1}{K C_i R_i}, \quad p_2 = \frac{K}{C_p R_{out}}. \tag{3}$$

The phase shifts caused by pole p1 in the numerator and denominator cancel each other out. The non-dominant pole p2 has the same effect of attaching a parasitic capacitance of C_p/K at the amplifier output. In our class A/AB amplifier, the dominant pole is at the output of the first stage which is Miller compensated, and the non-dominant pole is at the output of the second stage. Thus the amplifier is designed by estimating that the effective load equals C_p/K, and a 200 fF capacitance is used here. The simulated frequency response of the proposed class A/AB amplifier is depicted in Fig. 7. The amplifier achieves 90-dB DC gain due to the long channel length used in the first stage, and the GBW is 19 MHz while the phase margin is 59.7 degrees, with a power consumption of only 22 μW. The amplifier was verified in the design-bench discussed previously, and achieved an SNDR of 97.94-dB. Operational amplifiers used in the second and third integrators share the same topology but with optimized scaled power consumption.

3.3. One-bit quantizer and latch

The design requirement for a one-bit quantizer is relaxed in the ΣΔ modulator. A fully symmetrical regenerative comparator (Fig. 8) is used[10]. The circuit is improved by adding cross-coupled transistors M2a, b to accelerate the regeneration process. When clk goes low, quantizer outputs are reset to V_{DD}.

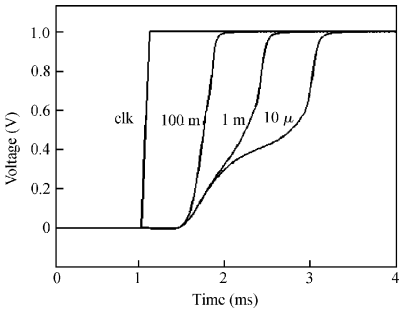

Fig. 9. Signal-dependent delay of the quantizer.

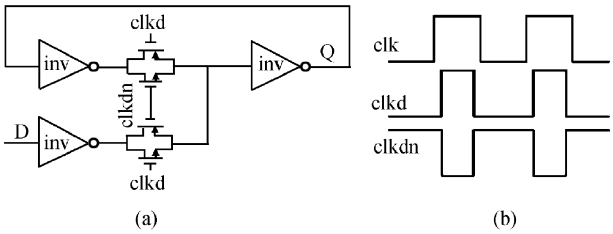

Fig. 10. (a) Schematic of the latch; (b) Clock waveform.

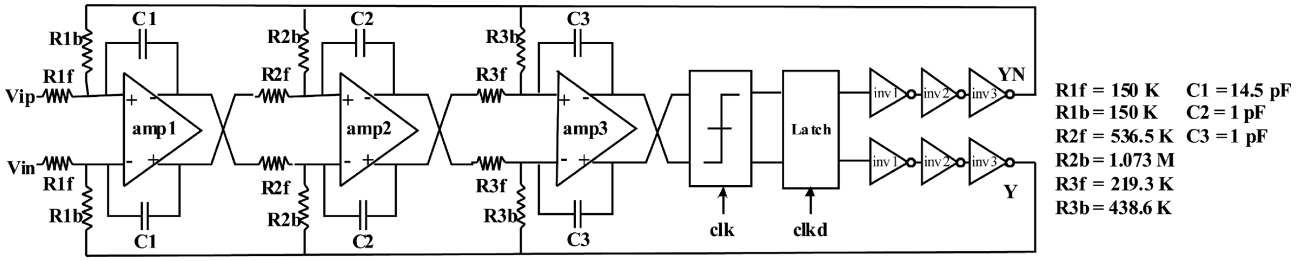

Fig. 11. Complete circuit of the presented modulator.

While clk goes high, the output nodes experience voltage drop and settle at the final state due to regeneration. The speed of the voltage drop depends on the input voltage of the quantizer. Thus, a signal-dependent delay is introduced during quantization. In a DT ΣΔ modulator, SNDR does not degrade even with a half period quantization delay, while in a CT ΣΔ modulator, signal-dependent delay has a similar effect to clock jitter and can significantly degrade SNDR. Figure 9 shows the simulated signal-dependent delay of the quantizer. The quantizer was verified in the proposed design-bench, and the SNDR dropped to 84 dB without any technique to deal with signal-dependent delay.

To absorb the signal-dependent delay, a latch with a delayed clock of 3.5 ns is introduced. Figures 10(a) and 10(b) show the schematic of the latch and the clock waveform respectively. An inverter chain is used to generate the delayed clock. Simulation in the design-bench shows that, even with the delayed clock varying from 2 to 5 ns, the quantizer plus the delayed latch get an improved SNDR of 100 dB. In the clock generation circuit, large decoupling capacitors are adopted on chip to reduce the supply noise induced clock jitter. Moreover, system level simulation shows that SNDR will not degrade seriously even with 200 ps clock jitter. Thus, clock jitter is not a severe problem in this low speed application.

3.4. DAC

The implemented NRZ feedback DAC consists of a feedback resistance, a positive ($+V_{\rm ref}$) and negative ($-V_{\rm ref}$) reference feedback voltage and switches. Power supply rails $V_{\rm DD}$ and GND are used as the feedback reference voltages. Two separate voltage pins with large decoupling capacitors are used to suppress noise interference. Switches are realized by cascaded scaling inverters which minimize loop delay and ensure a large slew rate.

3.5. Complete modulator

The complete modulator circuit is shown in Fig. 11. It includes three active *RC* integrators, a one-bit quantizer, a latch and a scaling inverter DAC. The resistor value of the first integrator is chosen to satisfy the thermal noise requirement as shown below:

$$R_{\rm i} = \frac{V_{\rm DD}^2/2}{4 \times 4kT f_{\rm B} \times {\rm DR}} \tag{4}$$

where T is the absolute temperature, and DR is the dynamic range. The value of resistance is selected as 150 kΩ. Other capacitors and resistors are set to satisfy the modulator coefficients shown in Fig. 2.

4. Experimental result

A third-order continuous-time ΣΔ modulator was designed in SMIC 0.13-μm mixed-signal CMOS technology. Metal–insulator–metal capacitors and high-resistivity poly resistors were used for their high linearity and small size. Figure 12 shows the layout photo. The modulator occupies an active area of 0.12 mm^2. Figure 13 shows the measured PSD (power spectrum density) result of the CT ΣΔ modulator; an SNDR of 81.4 dB is achieved. A summary of the performance is given in Table 1. The figure of merit (FOM) is defined as[5]

$${\rm FOM} = \frac{P}{2 \times f_{\rm B} \times 2^{({\rm DR}-1.76)/6.02}}, \tag{5}$$

where P and $f_{\rm B}$ DR denote the power dissipation and signal bandwidth respectively.

Table 2 shows a comparison between recently published low-voltage low-power ΣΔ modulators. The proposed CT third-order modulator achieved a FOM of 0.108 pJ/level, which is the best performance among these ΣΔ modulators that operates under 1.2 V.

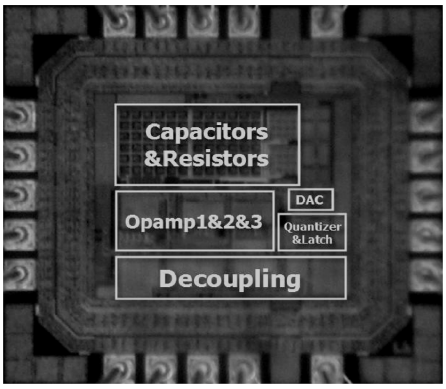

Fig. 12. Layout photo of the third-order CT ΣΔ modulator.

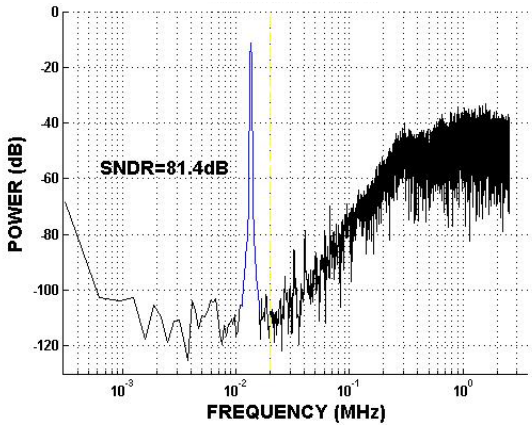

Fig. 13. Measured simulation PSD result of the modulator.

Table 1. Performance summary of the CT ΣΔ modulator.

Parameter	Value
Signal bandwidth/clock rate	20 kHz / 5.12 MHz
Technology	SMIC mixed-signal 0.13 μm
Supply voltage	1 V
Power consumption	60 μW
Active area	300×400 μm^2
SNDR/DR	81.4 dB / 85 dB
FOM	0.108 pJ/level

Table 2. Performance comparison.

Name, Year	Filter	Supply voltage (V)	SNDR (dB) / DR (dB)	Bandwidth (kHz)	Power (μW)	FOM (pJ/level)
Gerfers, 2003[5]	CT	1.5	70/80	25	135	0.330
Yao, 2004[6]	DT	1.0	81/88	20	130	0.158
Pavan, 2008[9]	CT	1.8	90.8/93.5	24	90	0.048
Roh, 2008[7]	DT	0.9	73.1/83	20	60	0.130
This work	CT	1.0	81.4/85	20	60	0.108

5. Conclusion

This paper presents a low-voltage low-power continuous-time ΣΔ modulator for audio application. A third-order active-RC loop filter with class A/AB amplifiers is implemented to perform noise shaping. A design methodology was proposed to enhance circuit design efficiency. Each active building block was verified and optimized in the proposed design-bench. The effective load of the amplifier in continuous-time integrators was deduced and power-efficient amplifiers were designed to ensure the low-power merit. The prototype was designed using SMIC mixed-signal 0.13-μm technology and the experimeatal results shown that an SNDR of 81.4-dB and a DR of 85-dB were achieved while dissipating 60 μW from a 1-V supply.

References

[1] Norsworthy S, Schreier R, Temes G. Delta-sigma data converters: theory, design, and simulation. New York: IEEE Press, 1996

[2] Dessouky M, Kaiser A. Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping. IEEE J Solid-State Circuits, 2001, 36(3): 349

[3] Sauerbrey J, Tille T, Schmitt-Landsiedel D, et al. A 0.7-V MOSFET-only switched-opamp ΣΔ modulator in standard digital CMOS technology. IEEE J Solid-State Circuits, 2002, 37(12): 1662

[4] Pun K P, Chatterjee S, Kinget P R. A 0.5-V 74-dB SNDR 25-kHz continuous-time delta-sigma modulator with a return-to-open DAC. IEEE J Solid-State Circuits, 2007, 42(3): 496

[5] Gerfers F, Ortmanns M, Manoli Y. A 1.5-V 12-bit power-efficient continuous-time third-order ΣΔ modulator. IEEE J Solid-State Circuits, 2003, 38(8): 1343

[6] Yao L, Steyaert M, Sansen W. A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS. IEEE J Solid-State Circuits, 2008, 39(11): 1809

[7] Roh J, Byun S, Choi Y, et al. A 0.9-V 60-μW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range. IEEE J Solid-State Circuits, 2008, 43(2): 361

[8] Rabii S, Wooley B. A 1.8-V digital-audio sigma-delta modulator in 0.8-μm CMOS. IEEE J Solid-State Circuits, 1997, 32(6): 783

[9] Pavan S, Krishnapura N, Pandarinathan R, et al. A power optimized continuous-time ΔΣ ADC for audio applications. IEEE J Solid-State Circuits, 2008, 43(2): 351

[10] Cho T B, Gray P R. A 10-b 20-Msample/s 35-mW pipeline A/D converter. IEEE J Solid-State Circuits, 1995, 30(3): 166

[11] Van der Zwan E, Dijkmans E. A 0.2-mW CMOS ΣΔ modulator for speech coding with 80 dB dynamic range. IEEE J Solid-State Circuits, 1996, 31(12): 1873