Structural and electrical characteristics of lanthanum oxide gate dielectric film on GaAs pHEMT technology*

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Abstract: This paper investigates the feasibility of using a lanthanum oxide thin film (La_2O_3) with a high dielectric constant as a gate dielectric on GaAs pHEMTs to reduce gate leakage current and improve the gate to drain breakdown voltage relative to the conventional GaAs pHEMT. An E/D mode pHEMT in a single chip was realized by selecting the appropriate La_2O_3 thickness. The thin La_2O_3 film was characterized: its chemical composition and crystalline structure were determined by X-ray photoelectron spectroscopy and X-ray diffraction, respectively. La_2O_3 exhibited good thermal stability after post-deposition annealing at 200, 400 and 600 °C because of its high binding-energy (835.6 eV). Experimental results clearly demonstrated that the La_2O_3 thin film was thermally stable. The DC and RF characteristics of Pt/La_2O_3/Ti/Au gate and conventional Pt/Ti/Au gate pHEMTs were examined. The measurements indicated that the transistor with the Pt/La_2O_3/Ti/Au gate had a higher breakdown voltage and lower gate leakage current. Accordingly, the La_2O_3 thin film is a potential high-k material for use as a gate dielectric to improve electrical performance and the thermal effect in high-power applications.

Key words: lanthanum oxide; XRD; XPS; pHEMTs

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1. Introduction

Recently, GaAs-based FETs have played a critical role in high-frequency communication applications, because of their high electron mobility, high breakdown voltage and low power consumption. As FET devices are scaled down, gate leakage currents are increased, reducing the breakdown voltage, and causing serious problems in the long-term reliability of the device. The main related issue is the lack of stable and high quality native oxides of the GaAs substrate[1]. As stated in some reviews[2, 3], Schottky gate leakage current and I_{ds}–V_{ds} hysteresis, which are both sensitive to the interface between GaAs and the gate electrode metal, limit device performance. Hence, pHEMTs must be fabricated from materials with a high dielectric constant (high-k), such as HfO_2, ZrO_2 and rare earth metal oxides (Y_2O_3, La_2O_3, Pr_2O_3). However, various dielectric constant k materials, such as Ta_2O_5, TiO_2, $SrTiO_3$ and $BaSrTiO_3$, also raise issues of thermal stability[4] associated with the poor quality of the interface between the oxide and the GaAs-based materials. Strictly, when a gate oxide layer is applied to a device, sufficient band offsets of over 1 eV must act as a barrier for both electrons and holes to reduce the gate leakage current, and its contact with the GaAs substrate must be stable[1]. Fortunately, La_2O_3 has several advantages over other oxide materials, such as high dielectric constant (~27), a strongly insulating character with a large band gap (~6 eV), and large conduction band offset (~2.4 eV) with GaAs substrate[1]. Clearly, La_2O_3 is also thermally stable. Consequently, a thermally stable material was used as a gate dielectric for the 1 μm GaAs pHEMTs in this work.

In this investigation, GaAs pHEMT with a La_2O_3 gate dielectric was examined by XPS and XRD to analyze the chemical bonding and crystalline structure following annealing at various temperatures. Then, the gate oxide, La_2O_3, was fabricated on the electron device, and the electrical characteristics of the transistor were studied and C–V measurements of the capacitor on GaAs pHEMTs were made. Finally, the DC and RF characteristics of the proposed Pt/La_2O_3/Ti/Au gate and conventional Ti/Au gate pHEMTs were summarized, and the La_2O_3 gate was thus demonstrated to be suitable for high-frequency and high-power applications.

2. Fabrication and structure of device

Figure 1 presents a cross section of the epitaxial layer structures of the E/D mode pHEMT, which was grown by MBE on a semi-insulating GaAs substrate. Between two Si planar δ-doping layers was sandwiched the InGaAs undoped channel layer for high-power operations. An undoped 28 nm AlGaAs was grown on an intrinsic GaAs as a Schottky layer, to yield a uniform gate recess depth and to reduce the Schottky gate tunneling current. For gate recess highly selective chemical etching, two 1.5 nm-thick undoped AlAs cap layers were grown on top of a 2 nm-thick undoped GaAs intrinsic layer, and a 30 nm-thick doped GaAs cap layer was inserted between these two AlAs cap layers. Finally, an n^+-GaAs cap layer with a thickness of 35 nm was grown to improve the ohmic contact resistivities.

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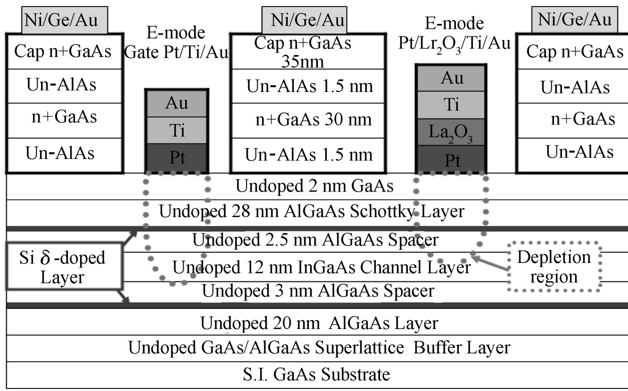

Fig. 1. Brief cross section of AlGaAs/InGaAs p-HEMT.

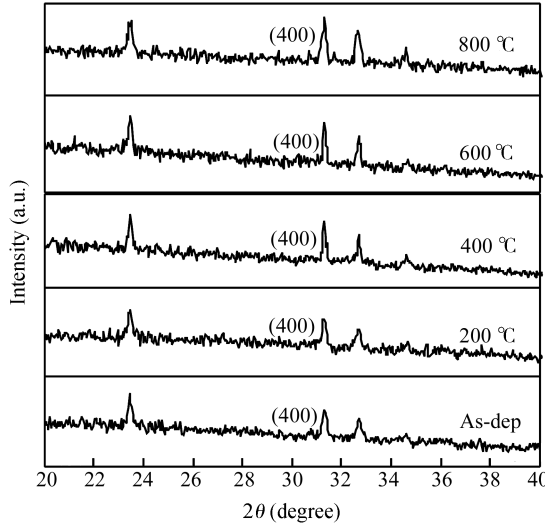

Fig. 2. XRD of La_2O_3 film after annealing at various temperatures.

To fabricate the E/D mode device, first, ohmic contacts formed from Ni/Ge/Au metals were deposited by electron-beam evaporation and patterned by a conventional lift-off process. Then, the wafer was loaded into a rapid-thermal-annealing system with an N_2-rich chamber and heated to 420 °C for 20 s to yield the final ohmic contacts. Then, an $NH_4OH/H_2O_2/H_2O$ solution was used for mesa etching. In the gate recess process, following chemical etching with highly selective succinic acid, the wafers were immediately loaded into an electron-beam evaporator. To fabricate a 1 μm-long gate, Pt/La_2O_3/Ti/Au (10 nm/10 nm/30 nm/150 nm) was deposited by electron-beam evaporation. In this stage, a 10 nm-thick lanthanum (La) metal was evaporated using an optimal oxygen flow rate of 5 sccm, at a chamber pressure of approximately 10^{-3} Torr. After the chamber pressure was reduced to 3×10^{-6} Torr, the conventional Ti/Au (30 nm/150 nm) gate metals were deposited. Finally, Ti/Au (30 nm/300 nm) was deposited to form interconnection and probe pads, then, a 300 nm-thick SiO_2 layer was carried out for device passivation.

3. Results and discussions

The intensity and thermal stability during the annealing of La_2O_3films were determined using XRD, as displayed in Fig. 2. The results indicate that the La_2O_3 as-deposited film yielded three obvious peaks at about 23.4°, 31.3°, and 32.66°,

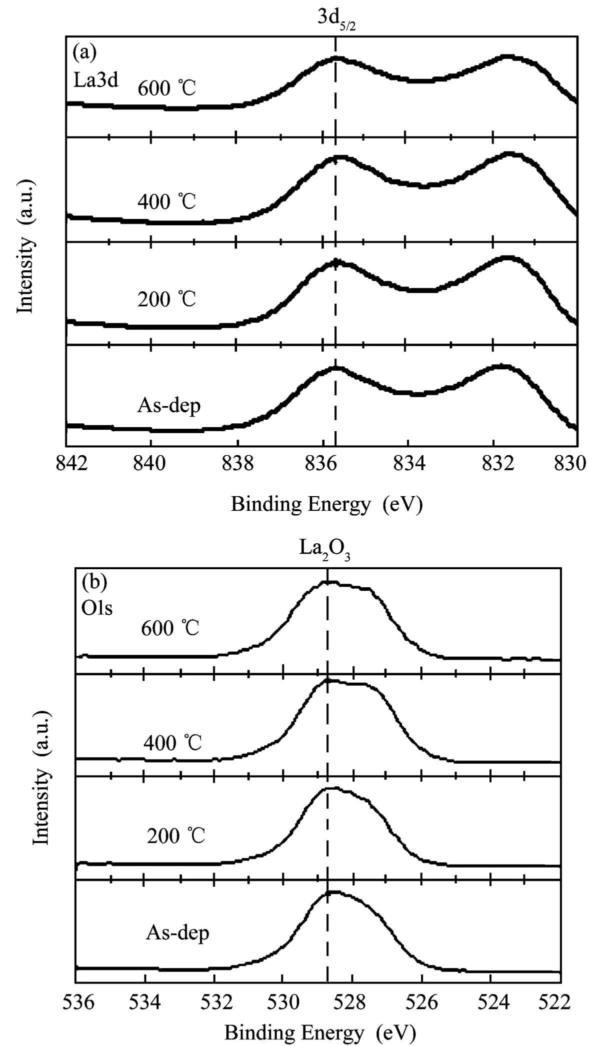

Fig. 3. XPS results of (a) La3d, (b) O1s in La_2O_3 films after annealing at various temperatures.

and several weak peaks. The XRD spectra revealed that the La_2O_3 as-deposited films had an almost amorphous structure. Clearly, the intensity of the three peaks increased with temperature from 200 to 800 °C, with a particularly marked change at 31.3°, suggesting better crystallization of the structure with increasing temperature[5]. Furthermore, these peaks revealed a preferential orientation of the crystallites of the (400) plane of the hexagonal reflection corresponding to a peak at 31.3°. Notably, the position of this peak was barely shifted from that of the as-deposited sample even when the temperature was increased to 800 °C. Annealing was performed to improve densification and reduce the number of interfacial defects between the substrate and the oxide film. The La_2O_3 film, after annealing from 200 to 600 °C, was studied by XPS to analyze the structural and compositional properties. Figures 3(a) and 3(b) plot the orbit data of La3d and O1s, respectively. Figure 3(a) plots the intensity of the La3d peak as a function of annealing temperature. From this figure, the binding energy of the main peak $La3d_{5/2}$ is estimated to be approximately 835.6 eV, corresponding to La_2O_3 bonding up to 400 °C[6]. Additionally, the spectra revealed that the peak was slightly shifted toward a higher binding energy as the temperature increased to 600 °C,

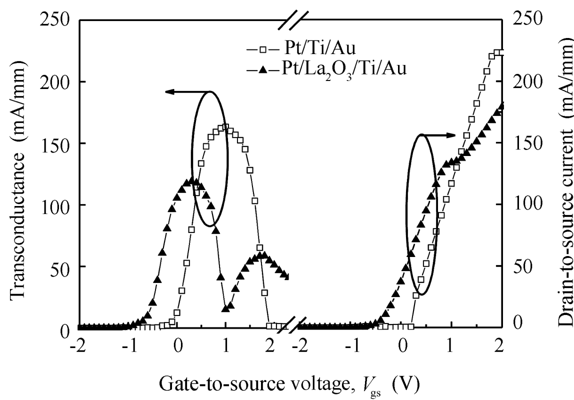

Fig. 4. g_m–V_{gs} and I_{ds}–V_{gs} characteristics of the La_2O_3 gate and the conventional gate.

with a binding energy shift of around 0.1 eV from the $La3d_{5/2}$ reference position. Figure 3(b) presents the orbit O 1s spectrum. The main peak of the binding energy in the as-deposited sample was at 528.6 eV, which was highly consistent with the typical O1s peak position of stoichiometric La_2O_3[5]. The measurements agree closely with the standard results in the XPS handbook. Interestingly, the La_2O_3 main peak is shifted by almost 1.5 eV at 600 °C, suggesting that the oxide film exhibited strong La–O bonding, even following annealing at higher temperatures. These phenomena demonstrate barely any change in the La or La–O bonding status, and confirm its superior thermal stability.

Figure 4 plots the DC characteristics of pHEMT with a gate length of 1 μm. The current–voltage (I_{ds}–V_{gs}) and transconductance–voltage (g_m–V_{gs}) curves with (Pt/La_2O_3/Ti/Au gate) and without La_2O_3 gate dielectric (Pt/Ti/Au gate) were obtained: the maximum I_{ds} and associated maximum g_m were 177 mA/mm and 118.76 mS/mm for the Pt/La_2O_3/Ti/Au gate pHEMT, and 221 mA/mm and 166.75 mS/mm for the Pt/Ti/Au gate pHEMT at a bias V_{ds} = 2.0 V. The standard Pt/Ti/Au HEMT yielded a higher peak g_m than the La_2O_3 gate, as the ability of the La_2O_3 HEMT architecture to modulate the gate-to-channel was suppressed by the insertion of a high-k insulator. Hence, the distance of the depletion region from the metal gate to the channel was increased, reducing the current in the modulation channel. Apparently, the conventional Pt/Ti/Au gate had a higher threshold voltage than the experimental Pt/La_2O_3/Ti/Au gate. The threshold voltage of the Pt/Ti/Au gate was 0.2 V for the E-mode. However, a D-mode p-HEMT with oxide as the dielectric layer was implemented using a Pt/La_2O_3/Ti/Au gate device, which yielded a pinch-off voltage of –0.6 V. The experimental results demonstrate that the E/D mode pHEMTs were formed on the same chip. Figure 5 plots the I_g–V_{gs} performance of the Schottky diodes. The I_g–V_{gs} curves show that the breakdown voltage (V_{BR}) was –20 V for the Pt/La_2O_3/Ti/Au gate and –9.4 V for the conventional Pt/Ti/Au gate, and the turn-on voltages (V_{on}) were 2 V and 0.7 V, respectively. The lager breakdown voltage was associated with the Pt/La_2O_3/Ti/Au gate because of the oxide layer had a high dielectric constant, which reduced the gate tunneling current at high voltage. As displayed in the

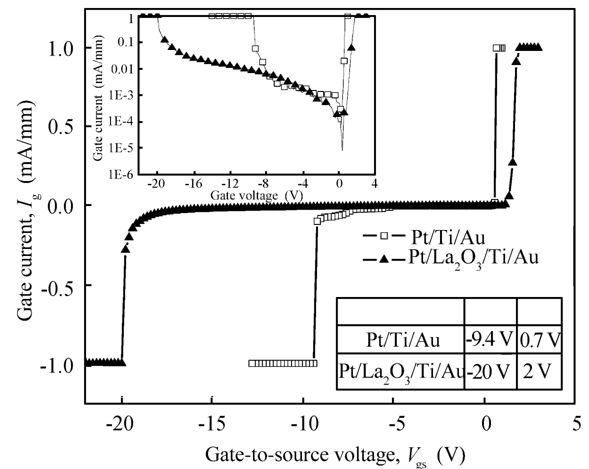

Fig. 5. Schottky diode characteristics of the La_2O_3 gate and the conventional gate.

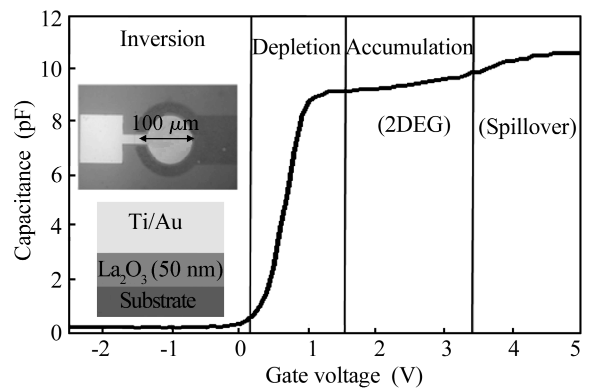

Fig. 6. C–V curve of La_2O_3 gate dielectrics of GaAs pHEMT measured at 1 MHz.

inset in Fig. 5, the leakage current of the La_2O_3 gate was significantly lower than that of the conventional gate, indicating that the former significantly reduced leakage. Therefore, the lower gate leakage current not only improved the device breakdown voltage but also increased the power-added efficiency (PAE) at a high-input-power swing.

The method for determining the dielectric constant of La_2O_3 was designed as follows. First, capacitance–voltage (C–V) measurements of the HEMT structure were made, with MOS-ring capacitors with diameters of 100 μm operated at 1 MHz, as displayed in Fig. 6. A La_2O_3 oxide layer with a thickness of about 50 nm was deposited by electron-beam evaporation. Hence, $C_{\mathrm{Dielectric}}$ could be easily calculated, using the following equation[7].

$$\frac{1}{C_{\mathrm{MAX}}} = \frac{1}{C_{\mathrm{Dielectric}}} + \frac{1}{C_{\mathrm{HEMT}}}. \quad (1)$$

Two-dimensional gas (2DEG) accumulated in the HEMT, and the maximum capacitance (C_{MAX}) was estimated to be around 9.5 pF, from Fig. 6. C_{HEMT} was calculated to be 30.33 pF ($\varepsilon_{\mathrm{GaAs}}$ = 12.9, $\varepsilon_{\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As}(x=0.24)}$ = 12.2148). Finally, Equation (1) yielded a capacitance of La_2O_3, $C_{\mathrm{Dielectric}}$, of 13.83 pF. Therefore, the dielectric constant of La_2O_3 was determined to be 9.95.

Figure 6 indicates a sharp transition from the depletion region to the 2DEG accumulation region. Accordingly, a weak

Table 1. Comparison of DC and RF characteristics of the different gate devices.

Characteristics of DC and RF	pHRMT of gate material	
	Pt/Ti/Au (E-mode)	Pt/La_2O_3/Ti/Au (D-mode)
V_{gs} @ drain-source current (I_{ds} = 0)	$V_{threshold}$ = 0.2 V	$V_{pinch\text{-}off}$ = –0.6 V
Maximum drain current, $I_{ds,max}$ (mA/mm)	221	177
Peak transconductance, $g_{m,max}$ (mS/mm)	166.75	118.76
Schottky turn-on voltage, V_{ON} (V)	0.7	2
Breakdown voltage, V_{BR} (V)	–9.4	–20
Cut-off frequency, f_T (GHz)	8	15.5
Maximum oscillation frequency, f_{max} (GHz)	19	21

pinning effect of the Fermi level at the GaAs/La_2O_3 interface was demonstrated, yielding a high-quality interface. Furthermore, an increase in the capacitance was observed at gate biases of beyond +3.45 V. This phenomenon might have been caused by the charge spillover effect in the 2DEG channel, which brought some of the carriers closer to the surface. Thus, the effective thickness of the barrier layer was decreased, and the capacitance was increased at gate biases of over +3.45 V.

Table 1 summarizes the DC and RF characteristics of the different gate devices. The current gain cut-off frequency (f_T) and the maximum oscillation gain cut-off frequency (f_{max}) were extracted using *S*-parameters, which were measured using a Vector Network Analyzer. The obtained f_T and f_{max} of the La_2O_3-gate were 15.5 GHz and 21 GHz, respectively, and those of the conventional gate were 8 GHz and 19 GHz, respectively. Moreover, the La_2O_3-gate obtained a high breakdown voltage, which could exceed that of the conventional gate. Accordingly, the measurements demonstrated that the La_2O_3-gate was suitable for RF and microwave circuit applications.

4. Conclusions

In this investigation, a high-k lanthanum oxide thin film (La_2O_3) was applied as a gate dielectric on GaAs pHEMTs. The thin La_2O_3 film characteristics of chemical composition and crystalline structure were determined using XRD and XPS after post-deposition annealing. The high-quality high-k La_2O_3 oxide layer was evaporated using an electron beam and a high oxygen flow rate to form the following gate-recess process, and then Ti/Au metals were deposited *in situ* in the same high-vacuum chamber. The experimental results indicated that binding energy slightly shifted as the temperature increased, suggesting that the La_2O_3 film was highly thermally stable. The La_2O_3 HEMT had a higher dielectric constant and so an E/D-mode pHEMT could be fabricated on one chip. Therefore, this technique was adopted to simplify the E/D-mode pHEMT process and improve the yield of wafers. The DC and *C–V* measurements demonstrated that the La_2O_3 HEMTs with a high-quality GaAs/La_2O_3interface, a surface state and a low gate leakage current have great potential for use in high-power, high-frequency, and high-temperature applications.

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