A Ka-band low-noise amplifier with a coplanar waveguide (CPW) structure with 0.15-μm GaAs pHEMT technology

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Abstract: This investigation explores a low-noise amplifier (LNA) with a coplanar waveguide (CPW) structure, in which a two-stage amplifier is associated with a cascade schematic circuit, implemented in 0.15-μm GaAs pseudomorphic high electron mobility transistor (pHEMT) technology in a Ka-band (26.5–40.0 GHz) microwave monolithic integrated circuit (MMIC). The experimental results demonstrate that the proposed LNA has a peak gain of 12.53 dB at 30 GHz and a minimum noise figure of 3.3 dB at 29.5 GHz, when biased at a V_{ds} of 2 V and a V_{gs} of –0.6 V with a drain current of 16 mA in the circuit. The results show that the millimeter-wave LNA with coplanar waveguide structure has a higher gain and wider bandwidth than a conventional circuit. Finally, the overall LNA characterization exhibits high gain and low noise, indicating that the LNA has a compact circuit and favorable RF characteristics. The strong RF character exhibited by the LNA circuit can be used in millimeter-wave circuit applications.

Key words: LNA; Ka-band; CPW; GaAs pHEMT; MMIC
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1. Introduction

In communication system applications, the millimeter-wave (MM-W) band has several significant advantages, including various communication channels, a wide bandwidth, and a high data transmission rate. Hence, it is extensively adopted in modern wireless communication systems. In the development of communication circuit technology, the coplanar waveguide (CPW) structure MMIC has been frequently utilized in transceiver communication systems[1−3]. Numerous researchers (Muraguchi *et al.*, 1984; Liu *et al.*, 2006) have reported that MMICs with CPW are applied in transmitter communication systems. The CPW structure is more easily fabricated than the microstrip-line, with no need to fabricate the back-side of the structure, good electronic isolation and a compact circuit layout[3]. Restated, the CPW MMIC not only reduces the chip size by eliminating discrete components, but also reduces the parasitic effect associated with wire-bonding[4].

The pHEMT performs excellently at high frequency, which is critical in MM-W applications. To fabricate the proposed CPW LNA, 0.15-μm GaAs pHEMT technology was adopted in a Ka-band circuit. Therefore, a Ka-band monolithic LNA using a CPW structure with a 0.15-μm GaAs pHEMT was employed in this work.

The circuit was designed as follows. First, the LNA utilizes a two-stage matching network, which was operated at high gain with low noise. To improve the noise characteristic, the proposed two-stage LNA with source inductor was designed in the first stage amplifier[5]. The S-parameters of the amplifier were designed and simulated using an advanced design system (ADS). The amplifier was designed to match fully the input and output impedance of 50 Ω without any external circuit. Each transmission line in the input stage was carefully chosen to optimize the gain, noise figure and return loss. Then, the amplifier was fabricated and S-parameters were measured using the vector network analyzer. Finally, the results indicated that the CPW LNA was an effective noise amplifier in MM-W integrated circuit applications.

2. Characterization of CPW structure

In recent years, coplanar waveguide (CPW) structures have gradually replaced microstrip-line technology in the design of microwave and millimeter wave circuits. Kuo *et al.* (2001) noted that the CPW structure benefited from its circuit layout, being insensitive to substrate thickness and having a high circuit density and low dispersion and low radiation losses, respectively[6].

The CPW gap is designed to be narrow, reducing the excitation waves in parallel-plate modes and eliminating the effect of microstrip discontinuity. In MMIC applications, the source and load impedances must be matched to the terminal characteristic impedance of 50 Ω. Accordingly, the dimensions of CPW are designed for such an impedance, with a width of 20 μm and a gap of 11 μm. Figure 1 presents a die photograph of a coplanar T-junction with a shorted stub connected to its third port, and the associated equivalent circuit model. The characteristic impedance of each line was designed to be 50 Ω, to minimize mis-matching losses. Figure 2 plots the simulated and measured return loss (S_{11}) results of the T-junction CPW structure. Figure 3 plots the simulated and measured insertion loss (S_{21}).

Figures 2 and 3 reveal that the EM simulation results are consistent with the measurements in the Ka-band region. Con-

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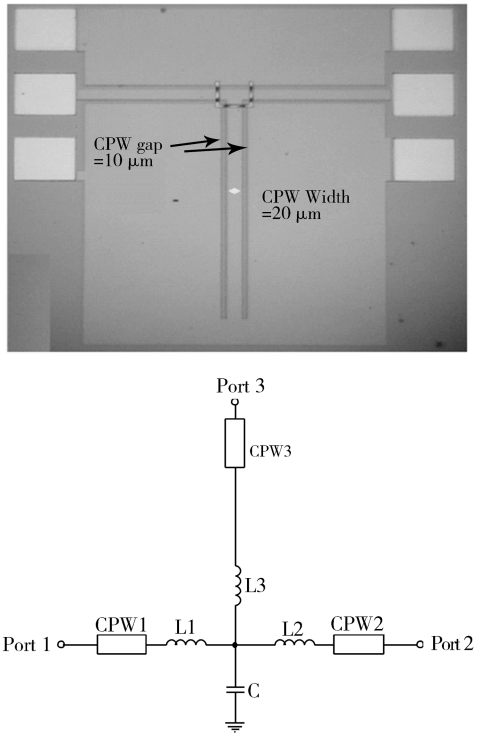

Fig. 1. T-junction CPW structure and its equivalent circuit model.

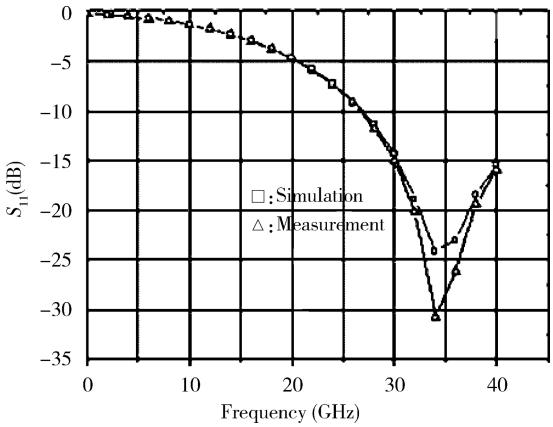

Fig. 2. Return loss (S_{11}) results of the EM simulated and measured in the CPW T-junction.

sequently, the CPW structure, with a width of 20 μm and a gap of 11 μm, is well designed for a characteristic impedance of 50 Ω, and is suitable as an amplifier in the MM-W IC.

3. Design and simulation of the LNA with CPW structure

In the designed MMIC, the lumped element was usually replaced by a distributed microstrip line, to reduce the parasitic effect. Hence, a transmission line was used as the passive inductor in this work. To achieve a favorable characteristic, the performance of the LNA circuit was simulated and the circuit layout with EM (electromagnetic) waves was verified using the advanced design system (ADS). The LNA MMIC used a cascade schematic which was carried out by the gate

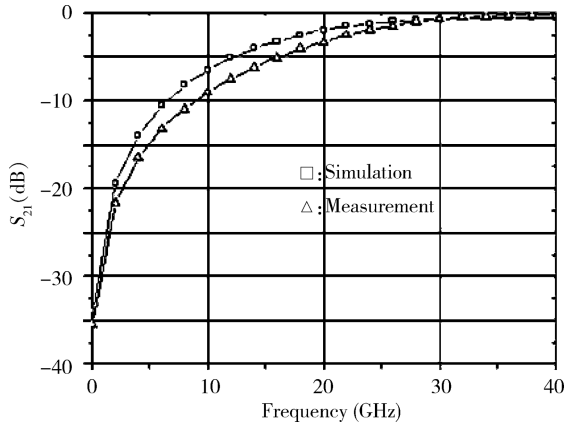

Fig. 3. Insertion loss (S_{21}) results of the EM simulated and measured in the CPW T-junction.

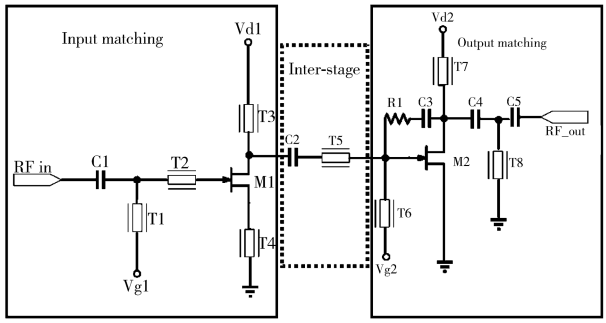

Fig. 4. LNA circuit cascade schematic of the Ka-band.

length 0.15 μm GaAs pHEMT with 2 × 50 μm channel width transistors at each stage. The matching circuits with matching impedance 50 Ω were realized as three-stage matching circuits, containing the input port, the inter-stage and the output port, as displayed in Fig. 4.

To optimize the LNA characteristic, the circuit was designed as follows. First, the input matching network was designed primarily to minimize the noise figure, by designing a two-stage LNA with inductor source degeneration. Then, the output stage was fully achieved to maximize gain, by implementing a high pass matching network. The pHEMT device was operated at a V_{ds} of 2 V and a V_{gs} of –0.6 V in this circuit, in which the FET could operate at high gain and low noise. Additionally, a degeneration inductance (T4) was directly connected to the source of the input pHEMT (M1), and used to tune the noise impedance matching of the pHEMT (M1). Selecting a suitable inductor (T2) enabled the real part of the input impedance pHEMT (M1) to match the 50 Ω. Therefore, an input matching network with a minimum noise figure was designed to improve impedance matching and ensure proper input return loss.

After the input matching stage of the matching circuit is the inter-stage, such that the output of the input stage was matched the input of the output stage. The inter-stage matching network was conjugate matched between the drain of the input pHEMT (M1) and the gate of the output pHEMT (M2), and was optimized to reduce the mismatch loss in the LNA circuit.

Next, the RF characteristics of the output stage were ver-

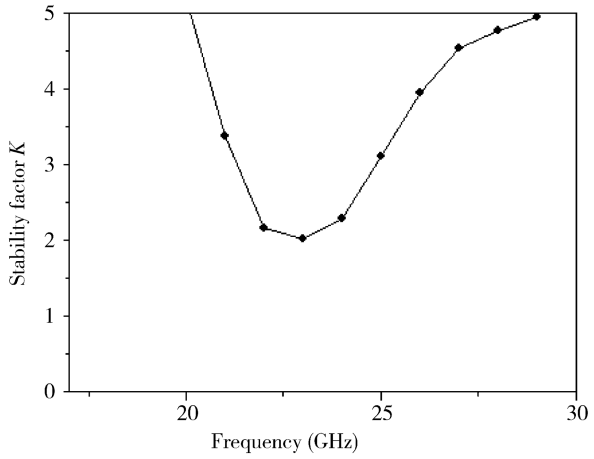

Fig. 5. Calculated stability factors K and B for the proposed LNA.

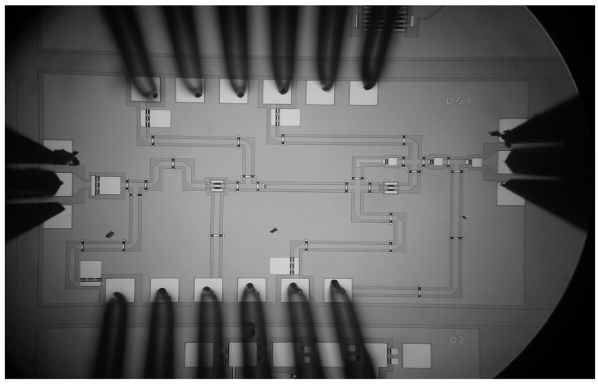

Fig. 6. Microphotograph with an LNA chip size of 1.6 × 0.9 mm^2.

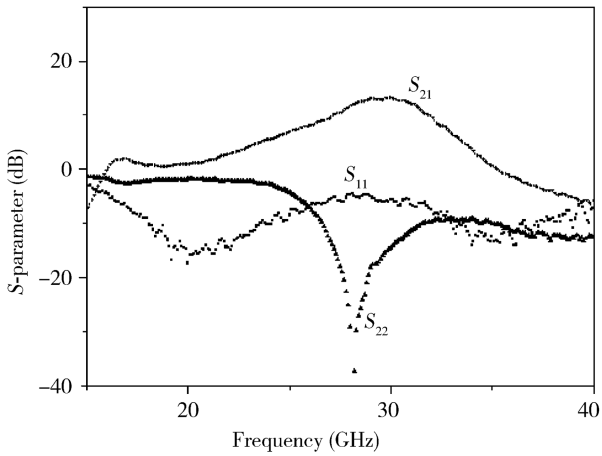

Fig. 7. Measured S-parameters of the proposed LNA.

ified using a feedback structure in the LNA circuit. The feedback resistance (R_1) as a shunt-feedback element was employed in the output stage to widen the bandwidth[7, 8], improve input/output matching, and increase stability[9]. Then, the capacitor (C_3) was used as in the ac coupling method[10], and the output of the second stage was loaded with a shunt inductor (T7). Thereafter, the output matching network was performed using a high-pass configuration of C_4, C_5, and T8, to maximize gain and impedance matching simultaneously. Furthermore, MIM capacitors (C_1, C_5) were installed at the RF input and output of the chip as DC blockers, and inductors (T1, T3) in the input matching network and (T6, T7) in the output matching network were used as the RF choke. Finally, the ports of the ground-signal-ground (GSG) structure were connected to the CPW, which acted as an input port and output port in the LNA circuit.

The stability of the amplifier circuit must be considered. Instability results from microstrip-line discontinuities and the electromagnetic (EM) effect, which is caused by coupling among various components at high frequency. All passive components were evaluated using an EM field simulator. A circuit stability analysis was performed for each stage to ensure the existence of a sufficient margin in the Ka-band. Figure 5 presents the simulation stability factor K for the proposed CPW LNA, indicating unconditional stability with $K > 1$ in the Ka-band region. Eventually, the stability of the amplifier was unconditionally stable in the Ka-band. Accordingly, circuit parameter optimization and EM simulation based on these essential matching networks were conducted, to yield the required circuit performance.

4. Measured results of CPW LNA MMIC

A two-stage noise amplifier MMIC was realized using 0.15-μm GaAs depletion mode pHEMT MMIC technology. Figure 6 presents a microphotograph of the two-stage CPW LNA MMIC with a chip area of 1.6 × 0.9 mm^2. This chip was measured on-wafer using RF 150-μm pitch-to-pitch with GSG probes, and the parasitic capacitances of the pads in the matching networks were considered. The S-parameters were measured using an Agilent 8510C vector network analyzer, as shown in Fig. 7. The measurements of the S-parameters revealed a small signal gain (S_{21}) with a peak of 12.53 dB at 30 GHz, with a bandwidth of 5.3 GHz from 27.3 to 32.6 GHz. The input return loss (S_{11}) was less than –10 dB, with a minimum of –16.66 dB at 34 GHz. The output return loss (S_{22}) was under –7.57 dB at 30 GHz.

The measurement of the S-parameters in Fig. 7 is limited: the S_{11} and S_{22} parameters were poor, perhaps because of variation in the fabrication and parasitic resistance. Fabrication variation resulted from the elimination of the polishing procedure and the formation of via holes during backside processing, worsening the power consumption of the chip. The matching circuit suffered from additional parasitic effects in the RF GSG probe pads, caused by parasitic resistances and capacitances, which generate thermal noise. The poor power consumption and parasitic effects substantially degraded the input and output return loss, and the return loss was directly related to the power gain and noise characteristics in the noise amplifier.

Figure 8 plots the noise figure: the minimum noise figure of 3.3 dB was obtained at 29.5 GHz. The noise performance in the Ka-band was excellent, and the S-parameters results show that the CPW LNA was well designed. The overall power gain (S_{21}) and noise figure (NF) demonstrate that this CPW LNA MMIC exhibits favorable RF characteristics in the Ka-band.

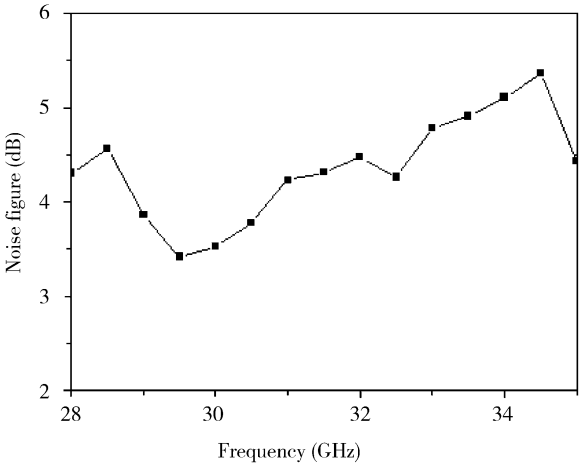

Fig. 8. Measured noise figure of the proposed LNA.

5. Conclusions

A two-stage MMIC LNA was implemented with a coplanar waveguide (CPW) topology, using 0.15μm D-mode pHEMT technology. Characterization of the LNA MMIC revealed a peak gain of 12.53 dB at 30 GHz, and a minimum noise figure of 3.3 dB at 29.5 GHz. Low noise was associated with high gain, and the RF characteristics were favorable. The MMIC LNA is thus very suitable for use in Ka-band noise amplifier MMIC applications.

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