A novel 2.95–3.65 GHz CMOS LC-VCO using tuning curve compensation*

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Abstract: This paper presents a new CMOS LC-VCO with a 2.95–3.65 GHz tuning range. The large tuning range is achieved by tuning curve compensation using a novel varactor configuration, which is mainly composed of four accumulation-mode MOS varactors (A-MOS) and two bias voltages. The proposed varactor has the advantages of optimizing quality factor and tuning range simultaneously, linearizing the effective capacitance and thus greatly reducing the amplitude-to-phase modulation (AM-PM) conversion. The circuit is validated by simulations and fabricated in a standard 0.18 μm 1P6M CMOS process. Measured phase noise is lower than –91 dBc at 100 kHz offset from a 3.15 GHz carrier while measured tuning range is 21.5% as the control voltage varies from 0 to 1.8 V. The VCO including buffers consumes 2.8 mA current from a 1.8 V supply.

Key words: CMOS; A-MOS; voltage-controlled oscillator; tuning curve compensation
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1. Introduction

Multi-mode and multi-band configurable transceivers have become more popular as the demands of multi-standard communication systems in a die increase. Many transceivers in the CMOS process merging two or several standards have been reported[1,2]. A wide tuning range LC-VCO is one of the key blocks in those issues, and it requires large tuning range for various standards, and low phase noise to achieve high performance. Additionally, low power consumption and small area cost are also important in mobile applications.

The most popular solutions to increase tuning range are switching LC tanks[3], capacitors[4] and inductors[5]. A switching LC tank is two separate resonators with different tuning ranges. Phase noise, tuning range and power consumption can be optimized separately, but a large area is required. A switched-capacitor array bank is widely used with a binary-weighted structure. However, because the phase noise of LC-VCOs depends on their quality factor Q, where Q is usually defined as energy stored/energy dissipated in the LC tank, they suffer Q degradation due to the switch-on resistors of the MOS switches, especially in the low frequency band. A switched-inductor is used only if the Q of the inductor is much larger than that of the capacitor varactor. So it is difficult to obtain reasonable phase noise when the operation frequency is below 10 GHz.

Two types of varactors are widely used in LC oscillators: pn-juction varactors[6] and accumulation mode MOS (A-MOS) varactors[7,8]. The pn-junction varactor has a monotonic capacitance–voltage (C–V) curve and its main drawback is low quality factor in higher GHz regions and small $C_{\max}/C_{\min}$ ratio[9]; another problem of junction varactors is that they can become forward biased by large-amplitude voltage swings[10]. An accumulation mode MOS varactor is superior to pn-junction varactors for many reasons. It achieves a higher quality factor and $C_{\max}/C_{\min}$ ratio. It can use either a single-ended or a differential control voltage. Furthermore, there is no amplitude clipping problem in the tank. Conventional LC-VCOs based on A-MOS[7,8] use two identical A-MOSs in parallel with an on-chip inductor. They have small control voltage range and large VCO gain $K_{\rm vco}$, which suffer from small tuning range and high noise sensitivity. The large-signal swing of the VCO output oscillation modulates the varactor capacitance due to a steep C–V curve, resulting in amplitude-to-phase modulation (AM-PM) conversion and degradation of the the phase noise[11,12].

In this paper, a novel A-MOS configuration composed of four A-MOSs is presented. It has wide tuning range using tuning curve compensation and AM-PM conversion is reduced. Furthermore, optimization of the varactor's Q and tuning range is discussed. The proposed LC-VCO has been applied to multi-mode multi-band global navigation satellite system (GNSS) receivers.

2. Proposed VCO design

2.1. A-MOS varactor

Usually a MOS varactor is implemented by connecting the drain, source, and bulk of an NMOS or PMOS together. Its capacitance depends on the voltage between gate and bulk and its tuning curve is non-monotonic[13,14]. An A-MOS varactor is similar to a conventional MOS varactor. Figure 1(a) illustrates the cross-section view of an A-MOS. The device is formed by placing an NMOS in an N-well[14,15], thereby

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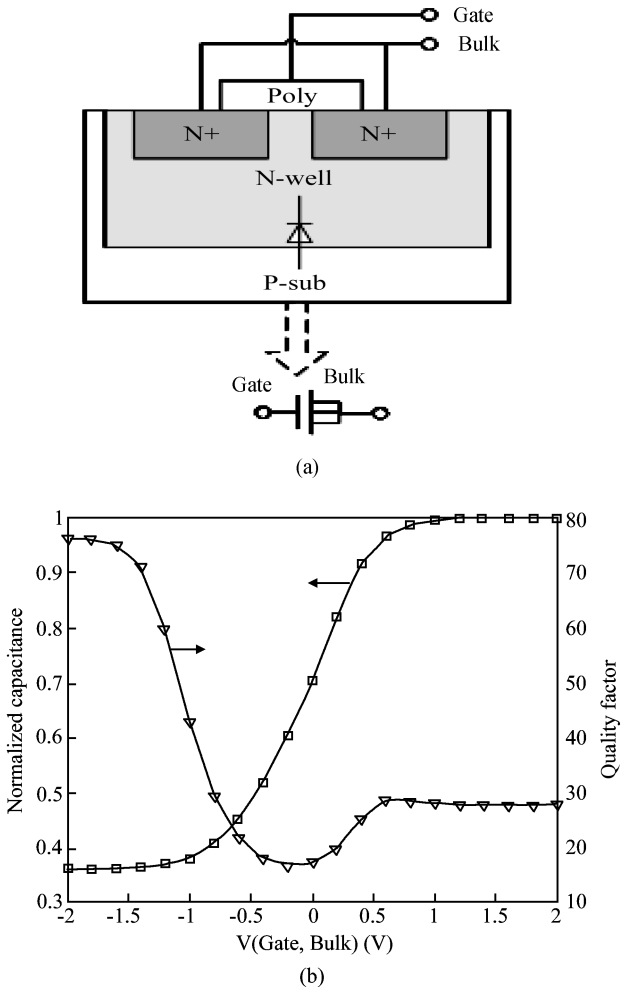

Fig. 1. (a) Cross-section view of an A-MOS; (b) Simulated *C*–*V* and *Q*–*V* curves of an A-MOS with large voltage swing at 3 GHz.

suppressing the injection of holes in the MOS channel in the strong, moderate, and weak inversion regions. It is noted that the P-type A-MOS is rarely used due to its low mobility. The tuning characteristics of the A-MOS varactor are shown in Fig. 1(b); it has a monotonic *C*–*V* curve and the capacitance is normalized by $C_{\max}$. The maximum capacitance $C_{\max}$ is approximated simply as $C_{\rm ox}$ due to a heavily doped poly-gate while $C_{\min}$ could be estimated as a series of $C_{\rm ox}$ and $C_{\rm dep}$, $C_{\min} = C_{\rm ox} \parallel C_{\rm dep}$, where $C_{\rm dep}$ is the minimum depletion capacitance. From Fig. 1(b), there is a tradeoff between tuning range and quality factor of the A-MOS. When the device is in weak inversion, $|V(\text{Gate, Bulk})| < 0.5$ V, and there is a steep capacitance variation, which is desirable for a wide tuning range when the quality factor reaches the smallest value in the *Q*–*V* curve, which corresponds to the degradation of phase noise. On the other hand, when the device is in accumulation or depletion, $|V(\text{Gate, Bulk})| > 0.5$ V, and the quality factor is much larger. However, its *C*–*V* curve is flat, which results in a small tuning range.

2.2. Tuning curve compensation of A-MOS varactors

The key to the compensation tuning curve is based on two series connected A-MOSs with offset DC bias voltage, which is shown in Fig. 2(a). $V_{\rm ctrl}$ is the control voltage and connects

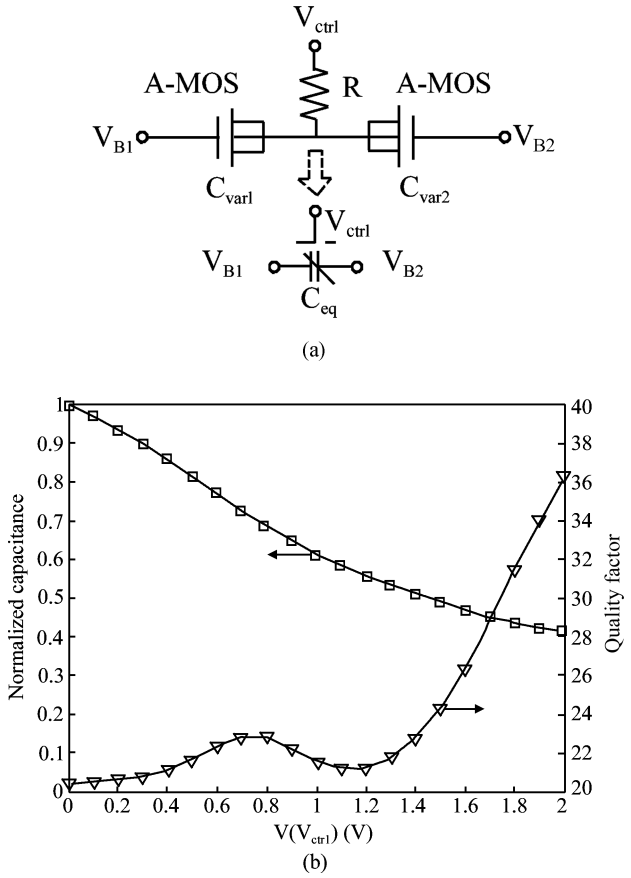

Fig. 2. (a) Proposed A-MOS varactors; (b) Simulated *C*–*V* and *Q*–*V* curves of the proposed varactor at 3 GHz.

to the bulk of the two A-MOSs by a resistor R. $V_{\rm B1}$ and $V_{\rm B2}$ are the DC bias of the gates. When $V_{\rm ctrl}$ varies from 0 to 1.8 V, the gate-bulk voltage of $C_{\rm var1}$ changes from $V_{\rm B1}$ to $V_{\rm B1} - 1.8$ V while that of $C_{\rm var2}$ is biased from $V_{\rm B2}$ to $V_{\rm B2} - 1.8$ V. The offset bias voltage is equal to $V_{\rm B1} - V_{\rm B2}$. The corresponding *C*–*V* curves between $C_{\rm var1}$ and $C_{\rm var2}$ are shifted by the same offset bias voltage. The equivalent capacitance is

$$C_{\rm eq}(V_{\rm ctrl}) = \frac{C_{\rm var1}(V_{\rm B1} - V_{\rm ctrl})C_{\rm var2}(V_{\rm B2} - V_{\rm ctrl})}{C_{\rm var1}(V_{\rm B1} - V_{\rm ctrl}) + C_{\rm var2}(V_{\rm B2} - V_{\rm ctrl})}. \quad (1)$$

Figure 2(b) shows the normalized *C*–*V* curve by the maximum capacitance and quality factor of the equivalent capacitor with 0.9 V offset bias voltage. The *C*–*V* curve is smooth when the control voltage $V_{\rm ctrl}$ varies from 0 to 2 V. The $C_{\max}/C_{\min}$ is equal to 2.5, which approaches the tuning ratio of a single A-MOS. Furthermore, there are two benefits for the proposed varactor. On the one hand, the equivalent quality factor of the A-MOS and tuning range would be optimized by the offset bias voltage. The quality factor $Q_{\rm var}$ of the A-MOS is defined as

$$Q_{\rm var} = \frac{1}{\omega C_{\rm var} R_{\rm var}}, \quad (2)$$

where $C_{\rm var}$ is the capacitance and $R_{\rm var}$ is effective series resistor; they can be modeled by a network analyzer using the *S*-parameter. The equivalent quality factor $Q_{\rm eq}$ of the proposed A-MOS varactor is

$$\frac{1}{Q_{\rm eq}} = \frac{1}{Q_{\rm var1}} + \frac{1}{Q_{\rm var2}}, \quad (3)$$

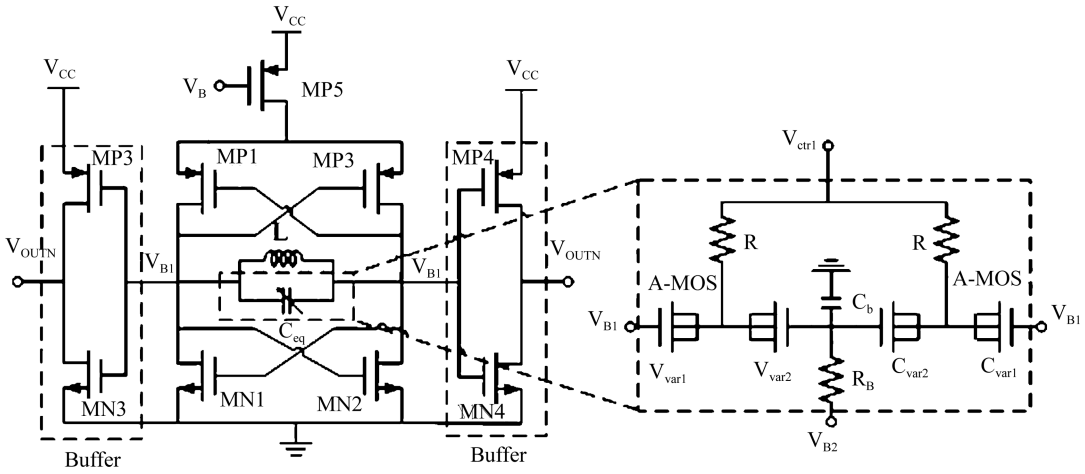

Fig. 3. Schematic of the proposed complementary –Gm CMOS LC VCO.

where Q_{var1} and Q_{var2} are the quality factors of C_{var1} and C_{var2} respectively. By adjusting the offset bias voltage and avoiding having the two A-MOSs work in weak inversion, a reasonable Q_{var1} and Q_{var2} can be realized. So a large equivalent quality factor Q_{eq} and wide tuning range are achieved simultaneously. On the other hand, the frequency of oscillation is specified by the effective capacitance of the varactor[11, 12]. The effective capacitance is measured with a large swing voltage in the tank. A large effective capacitance variation over the tuning range converts the amplitude modulation to phase modulation (AM-PM conversion). The proposed varactor with tuning curve compensation reduces the AM-PM conversion in two ways. The first is due to the smooth tuning curve. During one oscillation period, the time-average capacitance has a small fluctuation due to the linear C–V curve. So the gain of AM-PM conversion is reduced. The second is due to the fact that the voltage of each A-MOS decreases due to the series configuration. The small voltage of the A-MOS decreases the effective capacitance fluctuation, which results in a smaller AM-PM conversion.

2.3. Complete VCO design

The complementary –Gm LC VCO circuit employs a NMOS and PMOS cross-coupled pair in parallel to generate negative resistance. Because both the NMOS and PMOS generate –Gm, the negative resistance, –Gm is twice as large for the same power consumption compared with a single NMOS or PMOS oscillator. When oscillator is stable, the tank equivalent resistance is equal to –Gm. In other words, for the same tank, only the half power consumption is required. So, the complementary –Gm LC VCO is suitable for low power applications. Furthermore, there is much more symmetry voltage in the tank, which results in a lower $1/f$ noise up-conversion[23]. Additionally, the NMOS and PMOS cross-coupled pair could be used as bias for output buffers and varactors.

The proposed complementary –Gm LC VCO is shown in Fig. 3. MP1, MP2 and MN1, MN2 are the cross-coupled pairs, which generate negative resistance to compensate the equivalent resistance of the LC tank. MP5 is a tail current source. It provides a trade-off between phase noise and power dissipation. A large tail current results in a lower phase noise but a larger power dissipation. One disadvantage of the tail current source is that its $1/f$ noise is up-converted to the LC tank and degrades the phase noise. In this design, $1/f$ noise is reduced by large MP5.

An on-chip symmetry spiral inductor L is implemented by a top thick metal. A larger inductance of L is desirable for lower power consumption, but it limits the tuning range and results in a poor phase noise. L is optimized according to a specified tuning range and phase noise.

The varactor is the key feature of this design, which is illustrated in the right part of Fig. 3. Two symmetry tuning curve compensated A-MOSs are used as tank varactors, which is discussed in previous section. The two A-MOSs are configured in series. V_{B1} is directly connected to the cross-coupled pairs and is determined by the voltage between the gate and the source of MN1 and MN2. V_{B2} biases the varactor through a resistor R_B. V_{B2} can be generated by a resistance divider or diode-connected MOS. To reduce the noise induced by V_{B2}, a bypass capacitor C_b is adopted. The equivalent capacitance is specified by V_{B1}, V_{B2} and V_{ctrl}. By setting a proper offset voltage between V_{B1} and V_{B2}, a smooth tuning curve and reasonable quality factor can be obtained.

Two buffers composed of MN3, MP3 and MN4, MP4 are used to reduce the load effects and frequency variation. They are also biased by the cross-coupled pairs and their power consumptions are optimized according to the loads.

3. Experimental results

3.1. Measurement setup

The proposed complementary –Gm CMOS LC VCO has been manufactured in a standard 0.18 μm 1P6M CMOS process integrated with a low noise amplifier (LNA), down-mixer and IF driver, which is shown in Fig. 4. The output of the VCO is mixed with a very low phase noise RF signal, which is generated by a low phase noise RF signal generator and further amplified by the LNA. The down-converted IF signal is about

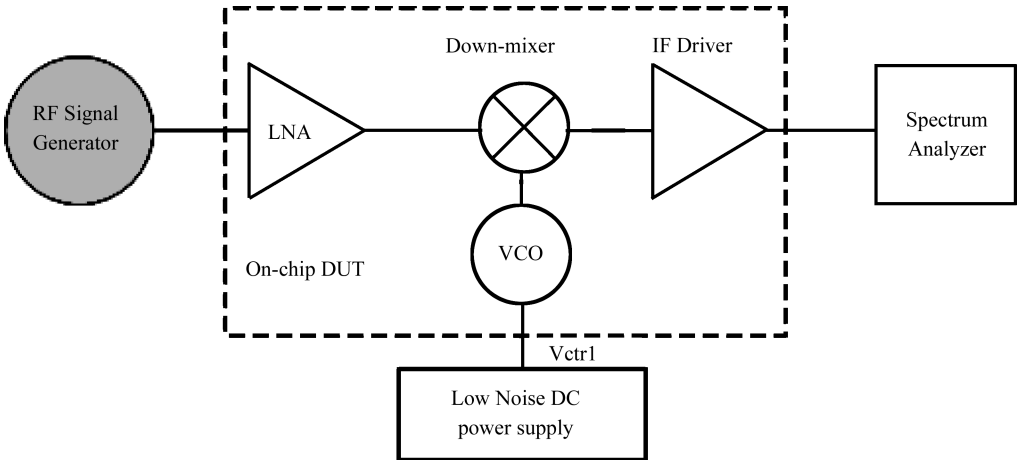

Fig. 4. Measurement setup.

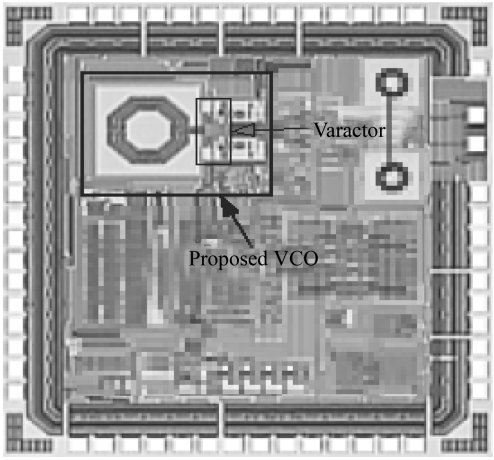

Fig. 5. Die microphoto.

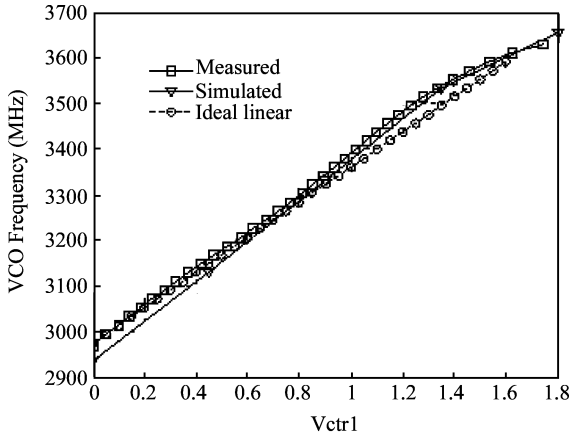

Fig. 6. Simulated and measured VCO tuning curve.

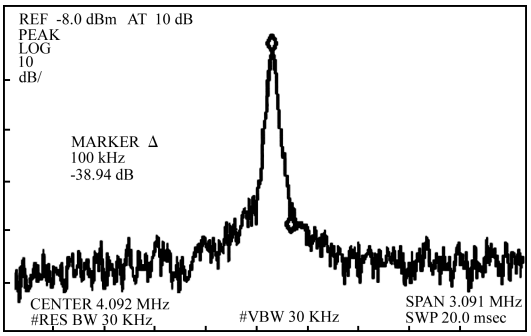

Fig. 7. Measured IF spectrum.

4 MHz and amplified by the IF driver. The spectrum is measured at the output of the IF driver. To reduce noise from the power supply and control voltage $V_{\rm ctrl}$, a low noise DC power supply is used for the measurement.

3.2. Measurement results

Figure 5 shows the chip micrograph of the proposed complementary –Gm CMOS LC VCO. The VCO occupies 600 × 400 μm^2. The frequency–voltage (f–V) curve is measured by fixing IF at about 4 MHz and the frequency of the RF signal changes as the tuning of the control voltage, $V_{\rm ctrl}$, which is illustrated in Fig. 6. The VCO output frequency is measured as $f_{\rm VCO} = f_{\rm RF} - f_{\rm IF}$, where $f_{\rm VCO}$ is the VCO output frequency, $f_{\rm RF}$ is the RF input frequency and $f_{\rm IF}$ is the frequency measured at the IF output. The frequency of the VCO changes from 2.95 to 3.65 GHz when $V_{\rm ctrl}$ is tuned from 0 to 1.8 V. The f–V curve of the proposed VCO is much more linear over the whole tuning range, especially when $V_{\rm ctrl}$ is below 1 V. The measured result is well in agreement with simulation. Over the whole tuning range, the proposed VCO consumes 2.8 mA from a 1.8 V power supply.

The phase noise of the proposed VCO is measured from the IF port. Figure 7 shows the measured IF spectrum, and the corresponding phase noise of the proposed VCO is better than –91 dBc at the 100 kHz offset. A performance comparison of the proposed VCO with other related LC-VCOs is listed in Table 1. The figure of merit (FOM) is represented as

$$\mathrm{FOM} = L(\Delta\omega) - 20\lg(\omega_0/\Delta\omega) + 10\lg(P/1\mathrm{mW}), \quad (4)$$

where ω_0 is the VCO oscillation frequency, $L(\Delta\omega)$ is the Leeson's phase noise equation at offset frequency $\Delta\omega$, and P is the power consumption in mW.

4. Conclusion

In this paper, A complementary –Gm CMOS LC VCO based on tuning curving compensation is presented. The quality factor of the varactor and tuning range are optimized simultaneously by adjusting the offset bias voltage, where its measured phase noise is as low as –91 dBc at 100 kHz, and

Table 1. Comparison of this work and related CMOS LC VCOs.

Parameter	This work (including buffers)	Ref. [17]	Ref. [18]	Ref. [4]
CMOS process (nm)	180	90	180	180
Center frequency (GHz)	3.3	13.73	5.6	4.65
Tuning range (%)	21.5	26.6	8.1	62
Power (mW)	5.04	2.81	5	12–81
Phase noise (dBc/Hz)	–91 @ 100 kHz	–108 to –104 @ 1 MHz	–118 @ 1 MHz	–95 to –101 @ 1 MHz
FOM (dBc/Hz)	–174.3	–182.2	–185.9	–157.5
Area (mm^2)	0.24	N/A	0.5	0.844

the tuning range is as large as 21.5%. The tuning curve is much more linear due to tuning curving compensation. The proposed VCO is suitable for multi-band multi-standard applications.

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