A 12-bit 100 MS/s pipelined ADC with digital background calibration

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Abstract: This paper presents a 12-bit 100 MS/s CMOS pipelined analog-to-digital converter (ADC) with digital background calibration. A large magnitude calibration signal is injected into the multiplying digital-to-analog converter (MDAC) while the architecture of the MDAC remains unchanged. When sampled at 100 MS/s, it takes only 2.8 s to calibrate the 12-bit prototype ADC and achieves a peak spurious-free dynamic range of 85 dB and a peak signal-to-noise plus distortion ratio of 66 dB with 2 MHz input. Integral nonlinearity is improved from 1.9 to 0.6 least significant bits after calibration. The chip is fabricated in a 0.18 μm CMOS process, occupies an active area of 2.3×1.6 mm^2, and consumes 205 mW at 1.8 V.

Key words: pipelined analog-to-digital converter; background calibration; digital calibration; capacitor mismatch; finite op-amp gain

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1. Introduction

Calibration techniques can be classified into two main types depending on their functionality: foreground calibration and background calibration. At the beginning of the 1990s, most of the schemes were foreground. Most of these converters were just calibrated only once during power up[1] or at the factory[2], but thermal drift and changing operating conditions can make these compensation methods ineffective or cause them to fail. Therefore, background schemes which can perform calibration continuously while the analog-to-digital (ADC) is in use are needed. Parallel structures can be used, but these techniques need additional stages[3] or additional ADCs[4], thus greatly increasing complexity, area and power of the whole ADC.

Another way is to directly inject a known signal into the stages, which will be added to the input signal and converted through stages in a similar way. In the digital domain, the injection will be detected, extracted and measured using a correlation-based or LMS-based method[5].

To make the calibration fast and accurate, the magnitude of the calibration signal needs to be large enough. Otherwise, with a large uncorrelated input signal present, it is difficult to detect and measure a small injection. But with a large injection, the input signal magnitude needs to be reduced so that the input signal plus injection may not exceed the full-scale range of the multiplying digital-to analog converter (MDAC). This leads to the reduction of the effective number of bits (ENOB).

Another problem is that in order to inject the calibration signal the sampling capacitor in the MDAC is usually split into several small capacitors[5–7]. But every capacitor has a different error and needs to be calibrated. It will take a much longer time to calibrate the mismatch errors caused by these capacitors, and the area and the power of the calibration logic will double at least.

In this paper, a digital background calibration scheme is proposed to overcome these problems. No additional capacitors are needed; the architecture of the MDAC is kept unchanged. The time for calibration can be very short and the area and the power of the digital logic can be small and low. Also, by injecting signals of different magnitudes, depending on the input signal level, whose equivalent magnitude is large, the time for calibration is further shortened while the dynamic range of the input signal does not need to be reduced. To demonstrate the scheme, a 12-bit 100 MS/s pipelined ADC with digital background calibration is implemented in 0.18 μm mixed-signal CMOS technology.

2. Theory of digital calibration

Figure 1 shows the amplifying phase of an MDAC of a conventional 1.5-bit stage in a pipelined ADC.

The amplified residue is affected by capacitor mismatch and finite op-amp gain, and becomes

$$V_{\mathrm{RES}} = (1+\delta)[(2+\alpha)V_{\mathrm{IN}} - (1+\alpha)DV_{\mathrm{REF}}]. \quad (1)$$

In the equation, $\alpha_{\mathrm{s}} = C_{\mathrm{s}}/C_{\mathrm{f}} - 1$, represents capacitor mismatch and $\delta = Af/(Af+1)$, represents finite op-amp gain. A is op-amp gain and f is feedback factor. D equals –1, 0, or 1, depending on the magnitude of the input signal.

Then the residue is digitized by the later ADC stages. Assuming the back-end ADC is also non-ideal with a gain of $1+\gamma$, in the digital domain, V_{RES} finally becomes

$$D(V_{\mathrm{RES}}) = (1+\gamma)(1+\delta)[(2+\alpha)V_{\mathrm{IN}} - (1+\alpha)D_{\mathrm{o}}V_{\mathrm{REF}}], \quad (2)$$

where D_{o} is the digital output of the stage.

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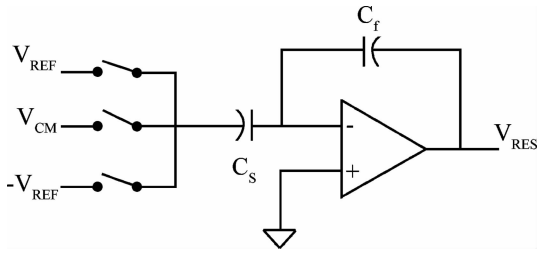

Fig. 1. Amplifying phase of a conventional 1.5-bit MDAC.

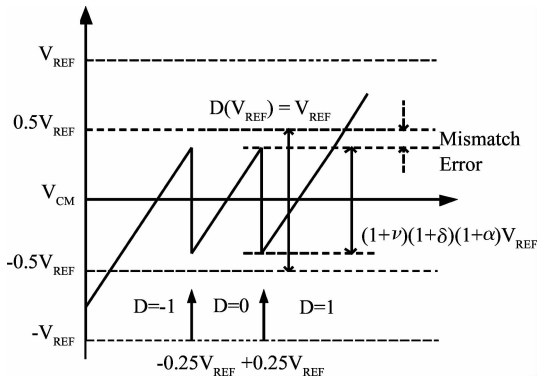

Fig. 2. Nonlinearity error in pipelined ADC.

Figure 2 shows how this mismatch affects the pipelined ADC's linearity. The non-ideal $(1 + \gamma)(1 + \delta)(1 + \alpha)V_{\mathrm{REF}}$ is subtracted in the analog domain, but the ideal $D(V_{\mathrm{REF}})$, which is V_{REF}, is added in the digital domain. As a result, a mismatch error occurs at the comparator threshold point, and is translated into the nonlinearity of the ADC.

The mismatch between $(1 + \gamma)(1 + \delta)(1 + \alpha)V_{\mathrm{REF}}$ and $D(V_{\mathrm{REF}})$ can be eliminated by either reducing the non-ideal factors in the analog domain or adjusting $D(V_{\mathrm{REF}})$ in the digital domain. For digital implementation, $(1 + \gamma)(1 + \delta)(1 + \alpha)V_{\mathrm{REF}}$ should be measured accurately with the back-end ADC to make $D(V_{\mathrm{REF}})$ match that value.

A PN-modulated signal which has a magnitude of V_{INJ} is injected into the stage and $D(V_{\mathrm{RES}})$ becomes

$$D(V_{\mathrm{RES}}) = (1 + \gamma)(1 + \delta)[(2 + \alpha)V_{\mathrm{IN}} - (1 + \alpha)DV_{\mathrm{REF}} - (1 + \alpha)\mathrm{PN} \times V_{\mathrm{INJ}}]. \quad (3)$$

PN is a pseudo-random noise (PN) pulse sequence of 1 and –1 with zero-mean. $\mathrm{PN} \times V_{\mathrm{INJ}}$ now has a gain of $(1 + \gamma)(1 + \delta)(1 + \alpha)$. Correlating PN with $D(V_{\mathrm{RES}})$ and accumulating in the digital domain, terms with V_{IN} and DV_{REF} will become noise since they are unrelated to PN. The only DC part is the sum of $(1 + \gamma)(1 + \delta)(1 + \alpha)V_{\mathrm{INJ}}$. Thus, the digital value of $(1 + \gamma)(1 + \delta)(1 + \alpha)$ is obtained.

3. A background calibration technique

Usually, injection is done by spliting the sampling capacitors into 2 or 4 or even more[6–8] small pieces. See Fig. 3 for an example[6]. Connect one of the capacitors with V_{CAL}, where V_{CAL} has a gain of $(1+\gamma)(1+\delta)(1+\alpha_1)$. Since there are four capacitors, four different errors should be measured and compensated. Additionally, it will take four times longer to calibrate the whole MDAC than if the capacitor were not split.

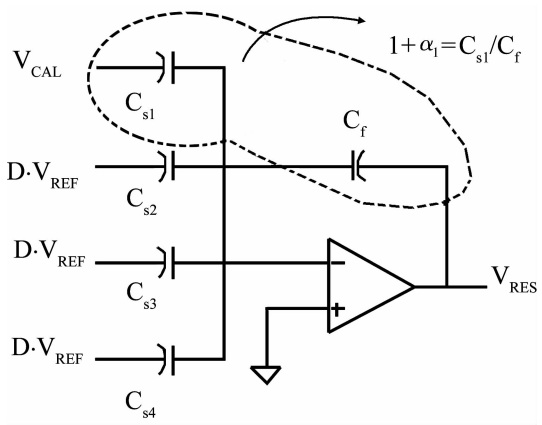

Fig. 3. Example of calibrating MDAC with split capacitors.

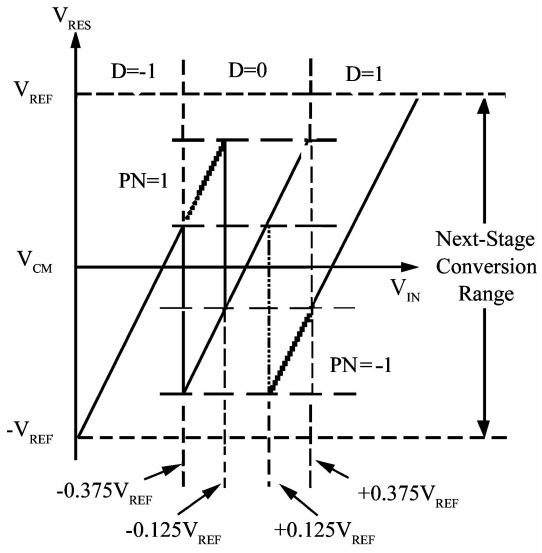

Fig. 4. Residue plot of the calibration scheme.

Also, the area of calibration logic will be four times larger and so will the digital power. Although some schemes[8] randomize the mismatch errors between capacitors to avoid increasing calibration time, randomization can only improve SFDR because in that case the distortion is translated into noise, but SNDR is always limited by these errors.

The scheme proposed here does not split the sampling capacitor. To make the injection possible, two additional comparators are used in the sub-ADC. Since the input capacitance of a comparator is quite small compared to the sampling capacitor, two additional comparators add only a little load to the front stage. Four comparators have thresholds at $-3/8V_{\mathrm{REF}}$, $-1/8V_{\mathrm{REF}}$, $+1/8V_{\mathrm{REF}}$, and $+3/8V_{\mathrm{REF}}$.

Calibration signals are injected between $-3/8V_{\mathrm{REF}}$ to $-1/8V_{\mathrm{REF}}$ and $+1/8V_{\mathrm{REF}}$ to $+3/8V_{\mathrm{REF}}$. See Fig. 4. When the input signal is between $+1/8V_{\mathrm{REF}}$ and $+3/8V_{\mathrm{REF}}$, no signal is injected if PN = 1, but a signal of $-V_{\mathrm{REF}}$ is injected if PN = −1, which means connecting the capacitor in Fig. 1 or Fig. 5 with V_{CM} not V_{REF} in the MDAC amplifying phase. Also, when the input signal is between $-3/8V_{\mathrm{REF}}$ and $-1/8V_{\mathrm{REF}}$, V_{REF} and 0 are injected if PN = 1 and PN = −1, respectively. As a result, the residue signal has a PN-modulated part with a large fixed-magnitude of $0.5V_{\mathrm{REF}}$, as shown in Eqs. (4)

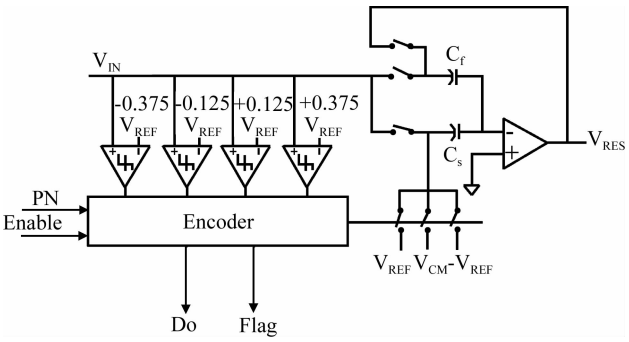

Fig. 5. A pipelined stage with digital background calibration.

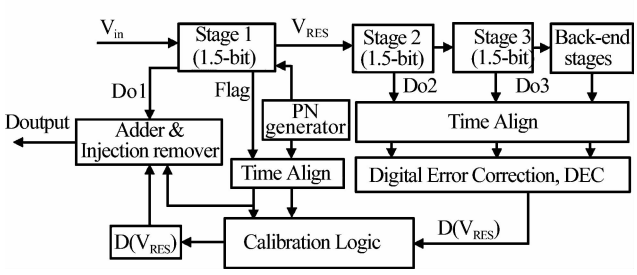

Fig. 6. A 1.5-bit/stage pipelined ADC with calibration.

and (5).

$$D(V_{\mathrm{RES}}) = (1+\gamma)(1+\delta)[(2+\alpha)V_{\mathrm{IN}} - (1+\alpha)\times 0.5V_{\mathrm{REF}} + (1+\alpha)\mathrm{PN}\times 0.5V_{\mathrm{REF}}], \quad (4)$$

$$D(V_{\mathrm{RES}}) = (1+\gamma)(1+\delta)[(2+\alpha)V_{\mathrm{IN}} + (1+\alpha)\times 0.5V_{\mathrm{REF}} + (1+\alpha)\mathrm{PN}\times 0.5V_{\mathrm{REF}}]. \quad (5)$$

Assuming a full-scale sine wave input signal, the possibility of occurrence of the signal between $-3/8V_{\mathrm{REF}} - -1/8V_{\mathrm{REF}}$ and $+1/8V_{\mathrm{REF}} - +3/8V_{\mathrm{REF}}$ is about 20%, thus it is about the same speed of calibrating one error in this scheme and in Ref. [6]. Since there are four errors in Ref. [6] and only one in this scheme, the calibration speed is about four times faster than that of Ref. [6] in calibrating an individual stage. Moreover, the injection has a large magnitude of $0.5V_{\mathrm{REF}}$, which also helps to make a fast convergence.

Figure 5 shows the architecture of a pipelined stage with digital background calibration. The encoder has two extra inputs, PN and Enable. Enable is used to turn on/off the calibration so we can test the ADC performance before and after calibration. D_{O} is the digital output of the stage and Flag is sent to the calibration logic to ensure correlation and accumulation right. The pipelined ADC with the proposed calibration scheme is illustrated in Fig. 6. Stage 1 is calibrated as an example. The PN generator is a linear feedback shifting register (LFSR), which generates a perfect pseudo-random noise sequence. After time alignment and digital error correction, $D(V_{\mathrm{RES}})$ is sent to the calibration logic. With the control of Flag, $D(V_{\mathrm{RES}})$ is correlated with PN. After accumulation and averaging, $D(V_{\mathrm{REF}})$ is obtained. Finally, adding $D(V_{\mathrm{RES}})$ to $D_{\mathrm{O1}} \times D(V_{\mathrm{REF}})$ and removing the PN injection signal, we get the calibrated digital output of the ADC. All the digital logic is implemented with adders and shifters. No multiplier is needed.

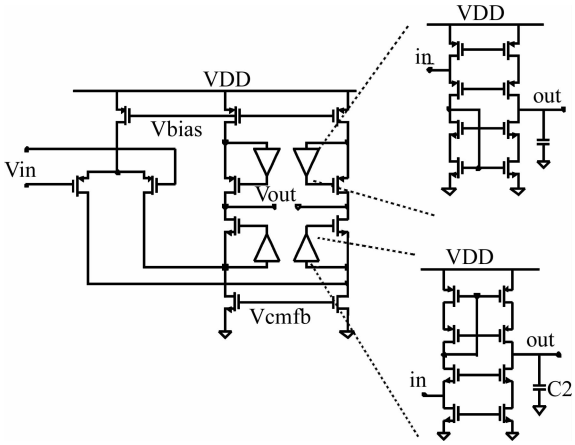

Fig. 7. Gain-boosted folded cascade op-amp.

In system simulations, including all circuit non-idealities such as capacitor mismatch, finite op-amp gain, and comparator and op-amp offsets, the calibration achieves an SNDR of 86 dB and an SFDR of 105 dB by averaging 2^{25} samples per stage.

4. Circuit implementation

The proposed ADC has one S/H, 13 1.5-bit stages, and a 2-bit flash. The digital output is 17 bits with redundant bits to reduce the digital truncation error. The digital encoding, digital correction, digital calibration, and also the PN sequence generator are all integrated in the digital logic.

While all gain errors in the signal path can be simultaneously calibrated with the proposed calibration method, to avoid introducing large nonlinear inter-stage errors[9, 10], the circuit implementation should ensure that all components are linear enough to achieve high SFDR. Single-stage folded cascade op-amp is used in SHA and other pipelined stages to obtain excellent bandwidth and output swing for low voltage application. As shown in Fig. 7, two gain-boosting feedback amplifiers are used to increase the output impedance of the folded cascade amplifier. The simulation results show that the op-amp has a DC gain of 95 dB and unity gain bandwidth of about 860 MHz with a 2 pF capacitance load.

Bootstrapped switches[11] are used in the S/H stage. In high-speed circuits, as switches gets larger, the amount of charge injection increases. The bootstrapped switch provides a lower and more linear on-resistance, and contributes to a smaller and more linear signal-dependent charge injection, which can be also calibrated along with the gain error.

5. Experimental results

The prototype chip is fabricated in a 0.18 μm CMOS process. The die photograph shown in Fig. 8 occupies an active area of 2.3×1.6 mm^2. The digital calibration algorithm is fully implemented on the prototype chip. The digital logic occupies 0.4×0.4 mm^2. Highly-linear differential sinusoidal input is obtained by using an Agilent E4438C signal generator followed by a band-pass filter and two single-ended-to-

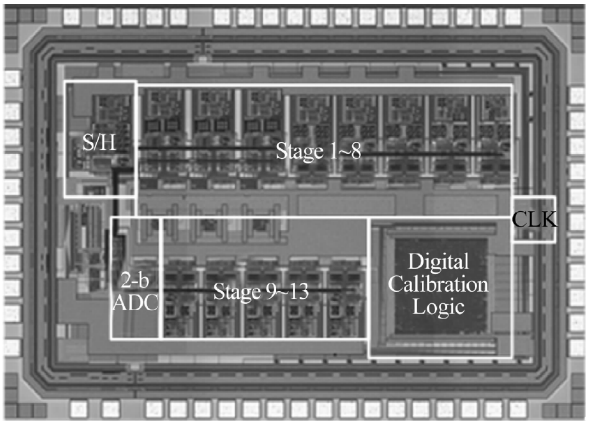

Fig. 8. Die photograph.

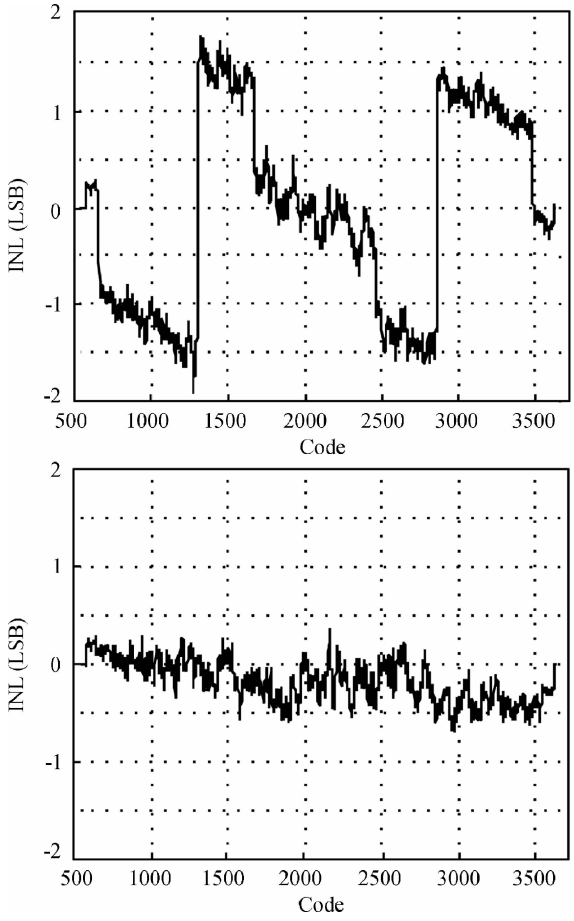

Fig. 9. Measured INL at 12-bit level before and after calibration.

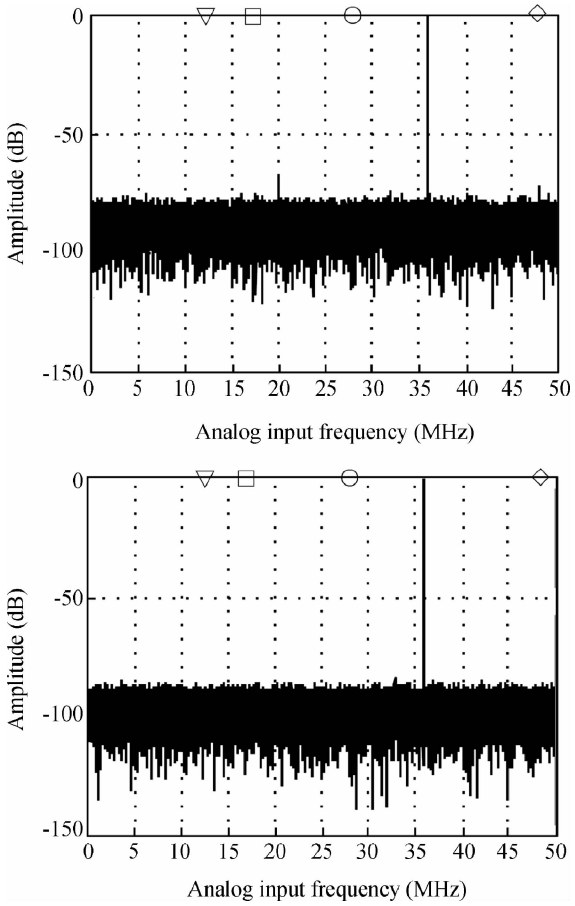

Fig. 10. Measured FFT spectra with 36 MHz input @ 100 MS/s before and after calibration.

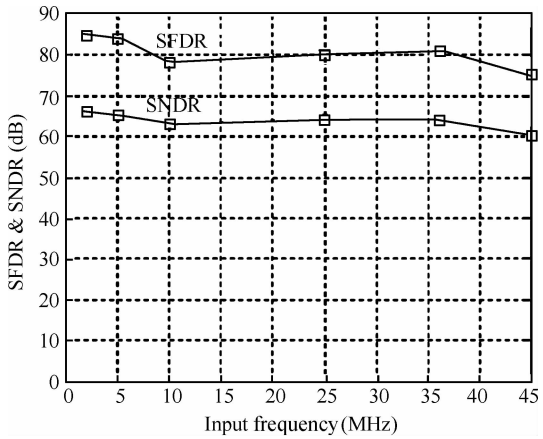

Fig. 11. Measured performances versus input frequency.

differential transformers.

To demonstrate the calibration algorithm, the capacitors in the first stage are slightly mismatched in layout by about 0.1%. In this way, the performance of the prototype ADC before calibration will degrade because of this mismatch.

Figure 9 shows the measured INL at a 12-bit level before and after calibration measured at 100 MS/s. The INL error jumps significantly at the comparator threshold points before calibration. The largest INL jump is from the first stage. After calibration, the INL errors are greatly reduced and improved from 1.9 LSB to 0.6 LSB.

Figure 10 shows the FFT spectrum of a 36 MHz input sampled at 100 MHz. The SFDR and SNR before calibration are 66 and 41 dB, respectively. After calibration, the SFDR and SNR are increased to 82 dB and 64 dB, respectively.

Figure 11 shows the ADC performance with varying input frequencies up to 45 MHz. The SFDR and SNDR stay constant at about 80 and 64 dB, respectively.

The measured performance is summarized in Table 1, which also lists performances of other converters with calibration schemes.

From Table 1, this work clearly has the smallest digital area and fastest calibration speed, and achieves a good INL and DNL. After calibration, the SFDR and SNDR of this 12-bit work approach the performances of some 15-bit works. Digital power is only 9 mW, much lower than that of most converters, even though the sampling rate is the second highest.

Table 1. Performance comparison with other ADCs.

ADC	Sampling rate (MS/s)	Calibration time (s)	INL (LSB)	DNL (LSB)	SFDR (dB)	SNDR (dB)	Area (Total/ Digital) (mm^2)	Power (Total/ Digital) (mW)
Ref. [5]	80	NM*	+0.5/−0.5	+0.3/–0.3	56.9	43.8	10.3/NM*	268/NM*
Ref. [6]	40	537	+3.4/−4	+0.34/–0.25	93	73	14/1.6	350/20
Ref. [7]	40	15	+1.2/−1.3	+0.25/–0.1	90	72	20/8	400/51
Ref. [8]	128	NM*	+0.4/−0.4	+0.05/–0.05	85	61	40/NM*	5700/NM*
This work	100	2.8	+0.4/−0.6	+0.1/–0.08	85	66	3.7/0.16	205/9

*not mentioned.

6. Conclusion

A 12-bit 100 MS/s pipelined ADC is designed and fabricated in 0.18 μm mixed signal CMOS technology with a fast digital background calibration scheme. Without reducing the signal range, this technique allows large magnitude injection while keeping the architecture of the MDAC unchanged. The proposed method calibrates all inter-stage gain errors resulting from capacitor mismatch, finite op-amp gain, and other sources with no strict requirements imposed on analog components.

References

[1] Karanicolas A N, Lee H S, Bacrania K L. A 15-b 1-Msample/s digitally self-calibrated pipeline ADC. IEEE J Solid-State Circuits, 1993, 28: 1207

[2] De Wit M, Tan K S, Hester R K. A low-power 12-b analog-to-digital converter with on-chip precision trimming. IEEE J Solid-State Circuits, 1993, 28: 455

[3] Ingino J, Wooley B. A continuously calibrated 12-b, 10-MS/s, 3.3-V A/D converter. IEEE J Solid-State Circuits, 1998, 33: 1920

[4] Chiu Y, Tsang C W, Nikolic B, et al. Least mean square adaptive digital background calibration of pipelined analog-to-digital converters. IEEE Trans Circuits Syst I, 2004, 51: 38

[5] Ming J, Lewis S H. An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration. IEEE J Solid-State Circuits, 2001, 36: 1489

[6] Liu H C, Lee Z M, Wu J T. A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration. IEEE J Solid-State Circuits, 2005, 40: 1047

[7] Siragursa E, Galton I. A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC. IEEE J Solid-State Circuits, 2004, 39: 2126

[8] Jewett R, Poulton K, Hsieh K C, et al. A 12-b 128-MSample/s ADC with 0.05 LSB DNL. IEEE ISSCC Dig Tech Papers, 1997: 138

[9] Keane J P, Hurst P J, Lewis S H. Background interstage gain calibration technique for pipelined ADCs. IEEE Trans Circuits Syst, 2005, 52: 32

[10] Daito M, Matsui H, Ueda M, et al. A 14-bit 20-MS/s pipelined ADC with digital distortion calibration. IEEE J Solid-State Circuits, 2006, 41: 2417

[11] Abo A, Gray P R. A 1.5 V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J Solid-State Circuits, 1999, 34: 599