Design of a DTCTGAL circuit and its application*

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Abstract: By research on the switch-signal theory for multiple-valued logic circuits, the theory of three essential elements and the principle of adiabatic circuits, a design scheme for a double power clock ternary clocked transmission gate adiabatic logic (DTCTGAL) circuit is presented. The energy injection and recovery can be conducted by the bootstrapped NMOSFET, which makes the circuit maintain the characteristics of energy recovery as well as multiple-valued input and output. An XOR/XNOR circuit based on DTCTGAL is also presented using this design scheme. Finally, using the parameters of a TSMC 0.25 μm CMOS device, PSPICE simulation results indicate that the proposed circuits have correct logic and significant low power characteristics.

Key words: multiple-valued logic; adiabatic; XOR/XNOR; low power; circuit design
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1. Introduction

At present, the development of large-scale integrated circuits is almost beyond Moore's Law; circuits that can be integrated on a chip will be larger and faster, and their power dissipation will also grow. Enormous power dissipation not only makes a variety of portable devices encounter problems with power supply, but also causes chip overheating, which could degrade the performance and reduce the life-time[1]. On the other hand, the area occupied by gate circuits on silicon has declined sharply with advances in semiconductor techniques, while there is more than 70% of the area for routing[2]. This has brought many problems in limiting circuit integration, increasing production costs, degrading circuit performance, and even causing unexpected running errors because of the electromagnetic effect between wires.

Multiple-valued logic circuits can not only increase the single-line capacity of information carrying and enhance the information density of integrated circuits, but they can also reduce the number of VLSI down-leads and pin-counts, which accordingly increase the space and time utilization of circuits and enhance the data-processing capacity[3,4]. However, binary components are used to realizing multiple-valued logic circuits at present, thus making the structure of circuits rather complex and the power dissipation enormous. Scholars from home and abroad have explored many fields to reduce the power dissipation of multiple-valued logic circuits; for example, Reference [5] presented a new type of multiple-valued logic circuit by using neuron MOS transistors. The neuron MOS transistors can flexibly operate the threshold and easily obtain the sum calculation of floating gate signals. Nevertheless, the modeling of neuron MOS transistors is complex and difficult to achieve with the conventional CMOS process. Reference [6] presented a design for a double-edge multiple-valued flip-flop, which adopts the redundancy-restraining techniques of sequential logic circuits and effectively uses the originally redundant edge triggered characteristics, which improves the system speed and reduces the circuit dissipation, but redundancy-restraining techniques still adopt the way that the DC power supply charges traditional CMOS circuits, and the energy is always irreversibly transformed from electric energy to heat. Although popular approaches to reduce power dissipation are to reduce the supply voltage, node capacitances and switching activity, the energy saving is still limited.

Adiabatic (energy recovery) circuits[7,8] use AC power supplies; in this way, the resonant tank is formed by the inductor in the power supply and the node capacitances in the circuits, so the charge on the node of the circuits can be recycled effectively to achieve energy recovery, and irreversible energy conversion from electric energy to heat caused by dissipative elements, i.e. resistance, can be largely reduced or avoided, hence the adiabatic circuits can achieve very low power consumption. Therefore, according to switch-signal theory and the theory of three essential elements (signal, network, load)[9], this paper takes the ternary logic circuit as an example, presents a novel double power clock ternary clocked transmission gate adiabatic logic (DTCTGAL) circuit based on the binary clocked transmission gate adiabatic logic (CTGAL) circuit[10], and further applies it to the design of a ternary adiabatic XOR/XNOR circuit. Finally, PSPICE simulation verifies that the circuits proposed have a correct logic function and obvious low-power characteristics.

2. Switch-signal theory and the theory of three essential elements

The high-threshold and low-threshold comparative operations of switch signal theory[11] are introduced first to de-

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scribe the interaction between switch and input signal; their expressions can be defined as follows:

High-threshold comparative operation:

$$a_{\mathrm{H}}^{m} = {}^{t}a = \begin{cases} \text{turn-on}, & a > t, \\ \text{turn-off}, & a < t. \end{cases} \tag{1}$$

Low-threshold comparative operation:

$$a_{\mathrm{L}}^{m} = a^{t} = \begin{cases} \text{turn-on}, & a < t, \\ \text{turn-off}, & a > t. \end{cases} \tag{2}$$

The two expressions represent the switching characteristics of NMOS transistors (high-threshold comparative operation) and PMOS transistors (low-threshold comparative operation) respectively; $t \in \{0.5, 1.5\}$ is the detection threshold of the input signal; $a \in \{0, 1, 2\}$ is the input signal; $m \in \{0.5, 1.5\}$, for NMOS transistors, m is the turn-on threshold and $m = t$; for PMOS transistors, $-m$ is the turn-on threshold; $2 - m = t$ and $1 - m = t$ when logic 2 and logic 1 are transmitted respectively. In ternary adiabatic circuits, logic 2 and logic 1 correspond to AC power Φ and Φ_1. The ternary not operation can be defined as follows:

$$\overline{x} = \begin{cases} 2, & x = 0, \\ 1, & x = 1, \\ 0, & x = 2. \end{cases} \tag{3}$$

According to the definitions above, the expressions can be deduced as follows:

$$\begin{cases} {}^{t}a = \overline{a}^{\overline{t}}, \\ a^{t} = {}^{\overline{t}}\overline{a}, \end{cases} \tag{4}$$

$$\begin{cases} {}^{t}(a \cdot b) = {}^{t}a \cdot {}^{t}b, \\ {}^{t}(a + b) = {}^{t}a + {}^{t}b, \end{cases} \tag{5}$$

$$\begin{cases} (a \cdot b)^{t} = a^{t} + b^{t}, \\ (a + b)^{t} = a^{t} \cdot b^{t}. \end{cases} \tag{6}$$

According to the theory of three essential elements (signal, network, load)[9], the four-valued algebra is proposed and used as a tool to research ternary circuits.

Definition 1. $\langle\!\langle \mathrm{H}, +, \cdot, -, \uparrow, \delta, 0, *, 1, 2 \rangle\!\rangle$ are four-valued algebra; the basic operations are $+$, $\cdot$, $-$, $\uparrow$ and δ, and must satisfy $\forall x, y \in \mathrm{H}$,

(1) $x + y = \max(x, y)$, $x \cdot y = \min(x, y)$, $0 < 1 < * < 2$,

(2) $y^{x} = y \uparrow x = \begin{cases} y, & x = *, \\ x, & \text{else}, \end{cases}$ $\overline{x} = \begin{cases} *, & x = *, \\ 2 - x, & \text{else}, \end{cases}$

$$y_{\delta} = \begin{cases} 2, & x = y, \\ 0, & \text{else}. \end{cases}$$

The exponential operation $\uparrow$, with the form of ${}_{x}\!<f>$, describes the transmission of the source signal x across switch $<f>$, and ε is the type of load.

$$<f> = *f + \varepsilon\overline{f}, \text{ switch control signal } f \in \{0, 2\}. \tag{7}$$

The binary character of the switch shows that the switch control signal f is a Boolean function and has two basic formats: $f = a \cdot b$ and $f = a + b$; when applied to Eq. (7), the series operation $\uparrow$ and parallel operation $\|$ can be induced and are given by:

$$<a \cdot b> = <a> \uparrow <b>, \ <a + b> = <a> \,\|\, <b>. \tag{8}$$

Assume that the NMOS switch N_1 is controlled by a, Φ is the source signal, and the NMOS switch N_2 is controlled by b. When N_1 and N_2 are connected in series, this can be written as ${}_{\Phi}\!<{}^{t}a> \uparrow <{}^{t}b> = {}_{\Phi}\!<a_{\mathrm{H}}^{m}> \uparrow <b_{\mathrm{H}}^{m}>$. Only when N_1 and N_2 are turned on at the same time, can Φ be sent to the output, and the relationships are given as follows:

$$\begin{aligned} {}_{\Phi}\!<{}^{t}a> \uparrow <{}^{t}b> &= {}_{\Phi}\!<a_{\mathrm{H}}^{m}> \uparrow <b_{\mathrm{H}}^{m}> \\ &= \begin{cases} \Phi, & a > m \text{ and } b > m, \\ \varepsilon, & \text{else}. \end{cases} \end{aligned} \tag{9}$$

This can be analyzed in the same way when PMOS transistors are connected in series.

Except for the sole-source signal, the "parallel connection" operation $|$ should be adopted for multiple-source signals x_i, where $i \in K = \{1, 2, \ldots, k\}$.

Definition 2.

$$\Big|_{i \in k}{}_{x_i}\!<f_i> = \sum_{i \in k} x_i f_i + \varepsilon\overline{\sum_{i \in k} f_i},$$

$$\forall i, j \in k; \text{ if } x_i \neq x_j, \text{ then } f_i \cdot f_j = 0.$$

Theorem 1. (Operation conversion theorem)

$$\begin{aligned} &<F(a, b, c, \ldots, +, \cdot, 2, 0)> \\ &\quad = F(<a>, <b>, <c>, \ldots, \|, \uparrow, *, \varepsilon). \end{aligned}$$

Theorem 2. (Network conversion theorem)

$$\begin{aligned} &\Big|_{i \in k}{}_{x_i} F_i(<a>, <b>, <c>, \cdots, \|, \uparrow, *, \varepsilon) \\ &\quad = \sum_{i \in k} x_i F_i(a, b, c, \cdots, +, \cdot, 2, 0) + \\ &\qquad \varepsilon\overline{\sum_{i \in k} F_i(a, b, c, \cdots, +, \cdot, 2, 0)}, \end{aligned}$$

$\forall i, j \in K$, if $x_i \neq x_j$, then $F_i \cdot F_j = 0$.

Since outputs of the circuits always connect with capacitive loads ($\varepsilon = QQ$), a formula can be obtained from theorem 2:

$$QQ^{+} = \Big|_{i \in k}{}_{x_i}\!<F_i>|_{\varepsilon = QQ} = \sum_{i \in k} x_i F_i + QQ\overline{\sum_{i \in k} F_i}. \tag{10}$$

Theorem 1 describes the conversion relation between Boolean operation and switch operation, and theorem 2 describes the conversion relation between gate levels and component levels.

3. Design of the DTCTGAL circuit

Based on the binary CTGAL circuit[10], a novel design for a DTCTGAL circuit is proposed. The operation is divided into two steps: (1) clocked NMOS transistors, which are controlled by a clock $\overline{\Phi}$, finish sampling the input signals, and $\overline{\Phi}$ controls the work rhythm of the input sampling so as to make the phase of input signals equivalent to $\overline{\Phi}$; (2) under the

work rhythm of the other two power clocks Φ_1 and Φ, the input sampled values and the CMOS-latch structure are used to finish charging the output loads and recovering the charge on the output loads. Φ_1 and Φ have the same phase but different amplitudes: the amplitude values of Φ_1 and Φ are $V_{DD}/2$ and V_{DD}, which correspond to logic 1 and logic 2 respectively; their phase difference with $\overline{\Phi}$ is 180° (the output phase is the same as Φ_1 and Φ). To eliminate the floating output, complementary output signals are used.

Suppose in, inb to be the complementary input signals, x the sampled value of in, y the sampled value of inb, out, outb complementary output signals, and the initial values of out, outb to be zero. According to the switch-signal theory, theorems 1, 2 and Eq. (10), structural formulas for this circuit can be obtained.

In the first operational step:

in sampled value:

$$x^+ = \text{in} \cdot {}^{0.5}\overline{\Phi} + x \cdot \overline{{}^{0.5}\overline{\Phi}}. \tag{11}$$

The first item of the above equation shows that the NMOS transistor controlled by $\overline{\Phi}$ finishes sampling the input signal; the second item shows that the sampled value keeps its original value when this NMOS transistor is turned off. According to Eq. (1), this equation can be further expressed as follows:

$$\begin{aligned} x^+ &= \text{in} \cdot {}^{0.5}\overline{\Phi} + \varepsilon \cdot \overline{{}^{0.5}\overline{\Phi}} \\ &= \text{in} \cdot \overline{\Phi}_{\text{H}}^{0.5} + \varepsilon \cdot \overline{\overline{\Phi}_{\text{H}}^{0.5}} = {}_{\text{in}}\langle \overline{\Phi}_{\text{H}}^{0.5} \rangle|_{\varepsilon = x}. \end{aligned} \tag{12}$$

The function expression of y can be obtained in the same way:

$$\begin{aligned} y^+ &= \text{inb} \cdot {}^{0.5}\overline{\Phi} + y \cdot \overline{{}^{0.5}\overline{\Phi}} = \text{inb} \cdot {}^{0.5}\overline{\Phi} + \varepsilon \cdot \overline{{}^{0.5}\overline{\Phi}} \\ &= \text{inb} \cdot \overline{\Phi}_{\text{H}}^{0.5} + \varepsilon \cdot \overline{\overline{\Phi}_{\text{H}}^{0.5}} = {}_{\text{inb}}\langle \overline{\Phi}_{\text{H}}^{0.5} \rangle|_{\varepsilon = y}. \end{aligned} \tag{13}$$

It is necessary to point out that the input signals in, inb are complementary, so $y = \overline{x}$ after sampling.

In the second operational step:

$$\text{out}^+ = \Phi[{}^{1.5}x + \text{outb}^{0.5}] + \Phi_1 \cdot {}^{0.5}(y \cdot x) + 0 \cdot {}^{1.5}\text{outb}. \tag{14}$$

The first and third items of the above equation show that the input sampled value controls Φ and Φ_1 to charge the output load and recover the charge on the output load respectively; the second item shows that the complement of the output signal controls the evaluation and energy recovery of this output by feedback; the fourth item shows that outb eliminates the float of out when out does not follow Φ or Φ_1 to change. The above equation can be further expressed as follows:

$$\begin{aligned} \text{out}^+ &= \Phi(x_{\text{H}}^{1.5} + \text{outb}_{\text{L}}^{1.5}) + \Phi_1(y_{\text{H}}^{0.5} \cdot x_{\text{H}}^{0.5}) + 0 \cdot \text{outb}_{\text{H}}^{1.5} \\ &= {}_{\Phi}\langle x_{\text{H}}^{1.5} \rangle \| \langle \text{outb}_{\text{L}}^{1.5} \rangle |_{\Phi_1} \langle y_{\text{H}}^{0.5} \rangle \\ &\quad \uparrow \langle x_{\text{H}}^{0.5} \rangle |_0 \langle \text{outb}_{\text{H}}^{1.5} \rangle |_{\varepsilon = \text{out}}. \end{aligned} \tag{15}$$

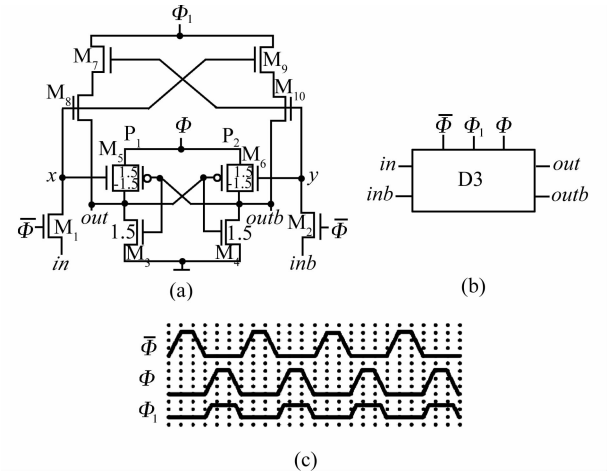

Fig. 1. DTCTGAL circuit: (a) Schematic; (b) Symbol; (c) Clock.

The function expression of outb can be obtained in the same way:

$$\begin{aligned} \text{outb}^+ &= \Phi[{}^{1.5}y + \text{out}^{0.5}] + \Phi_1 \cdot {}^{0.5}(y \cdot x) + 0 \cdot {}^{1.5}\text{out} \\ &= \Phi(y_{\text{H}}^{1.5} + \text{out}_{\text{L}}^{1.5}) + \Phi_1(y_{\text{H}}^{0.5} \cdot x_{\text{H}}^{0.5}) + 0 \cdot \text{out}_{\text{H}}^{1.5} \\ &= {}_{\Phi}\langle y_{\text{H}}^{1.5} \rangle \| \langle \text{out}_{\text{L}}^{1.5} \rangle |_{\Phi_1} \langle y_{\text{H}}^{0.5} \rangle \\ &\quad \uparrow \langle x_{\text{H}}^{0.5} \rangle |_0 \langle \text{out}_{\text{H}}^{1.5} \rangle |_{\varepsilon = \text{outb}}. \end{aligned} \tag{16}$$

According to Eqs. (11)–(16), a corresponding DTCTGAL circuit can be drawn, as shown in Fig. 1(a).

The circuit above combines ternary logic with an adiabatic CTGAL circuit, and makes use of double power clock to charge and discharge the loads, so it can be termed double power clock ternary clocked transmission gate adiabatic logic (DTCTGAL) circuit.

Figure 2 shows the simulation waveforms of the DTCTGAL circuit, where the input signal in is "201021…". As shown in Fig. 2, the power clock have six cycles: the inputs in, inb of the first and fifth cycles are 2, 0; the inputs in, inb of the second and fourth cycles are 0, 2; the inputs in, inb of the third and sixth cycles are 1, 1. Because of the symmetrical structure of DTCTGAL shown in Fig. 1, the working characteristics of the circuit when inputs in, inb are 0, 2 are the same as that when inputs in, inb are 2, 0. The working characteristics of the DTCTGAL circuit are analyzed next (taking the first and third cycles as examples respectively). The two cycles of the power clock are divided into six equal periods respectively, i.e. $T_1, \ldots, T_6$ and $T_1', \ldots, T_6'$.

The first cycle:

During period T_1, the voltages of the input in and the clock $\overline{\Phi}$ go high, but the voltages of the input inb and the power clock Φ_1, Φ are low. Therefore, M1 is turned on, and the voltage of the node x is charged to about $V_{DD} - V_{TN}$ where V_{TN} is the threshold voltage of the NMOS transistor M1; at the same time, M2 is turned on so as to make the voltage of the node y 0 V. M5 is turned on and M6 is turned off, while both branches M7, M8 and M9, M10 are turned off. Since both the voltages of the power clock Φ_1, Φ are 0 V, the output voltages of out, outb remain at 0 V. During this period, the input signals are sampled by clock $\overline{\Phi}$.

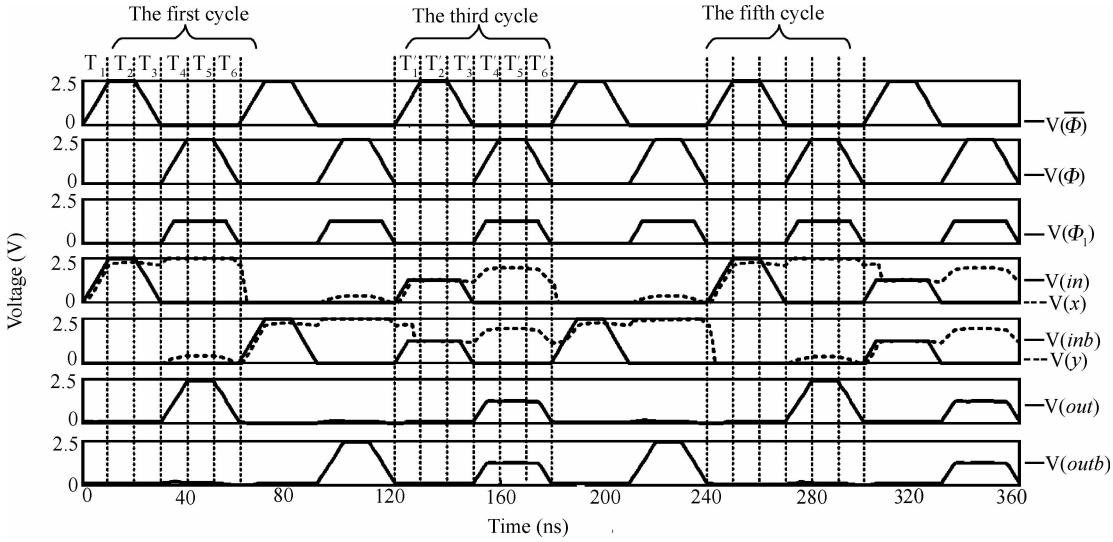

Fig. 2. Simulation waveforms of DTCTGAL.

During period T_2, the nodes x, y keep the value of input sampled signals.

During period T_3, the voltage of clock $\overline{\Phi}$ descends so that M1 is turned off and the voltage of node x stays at the sampled voltage level.

Therefore, period T_1–T_3 can be termed the sampling period when the input signals are sampled.

During period T_4 (the logic evaluation period), the voltage of $\overline{\Phi}$ is 0 V, but the voltages of Φ_1, Φ begin to rise; at this time, both M1 and M2 are turned off so as to make node x the floating high-voltage node and y the floating low-voltage node. Due to the parasitic capacitances among x and Φ_1, Φ, the voltage of node x can be bootstrapped to a higher level than $V_{DD} - V_{TN}$. M5 has been turned on, and power clock Φ charges the output out through M5 at the low voltage level, without threshold loss. When the voltage of out rises above the threshold of M4, M4 is turned on and outb is clamped to the ground (0). When the voltage of Φ rises above $|V_{TP}|$, where V_{TP} is the threshold voltage of the PMOS transistor P_1, P_1 is turned on, so power clock Φ charges output out at the high voltage level, without threshold loss. Hence out is clamped to Φ through the complementary transmission gate composed of M5 and P_1.

During period T_5 (the holding period), the voltage of out stays at V_{DD} which is the peak level of power clock Φ, and outb is clamped at 0 V.

During period T_6 (the energy recovery period), nodes x, y retain the original floating state, out follows Φ to drop to 0 V through the transmission gate composed of M5 and P_1.

The third cycle:

During period T_1', both nodes x, y are charged to $V_{DD}/2$ by inputs in, inb, M7, M 8 and M 9, M 10 are all turned on, and the branches M5, M6 connected to Φ are turned off. The working characteristics between periods T_2' and T_3' are equal to the first cycle, that is, nodes x, y retain the sampled value.

During period T_4' (the logic evaluation period), the power clock Φ_1 charges out through M7, M8 and charges outb through M9, M10 respectively, making out, outb follow Φ_1 to rise and clamped to Φ_1; at this time, M3 and M4 are turned off. The voltages of nodes x, y can be bootstrapped to a higher level than $V_{DD}/2$.

Table 1. Truth table of a ternary XOR/XNOR circuit.

Signal	Value								
A	0	0	0	1	1	1	2	2	2
B	0	1	2	0	1	2	0	1	2
$A \oplus B = A\overline{B} + \overline{A}B$	0	1	2	1	1	1	2	1	0
$A \odot B = \overline{A}\overline{B} + AB$	2	1	0	1	1	1	0	1	2

During period T_5' (the holding period), both out and outb are kept at $V_{DD}/2$.

During period T_6' (the energy recovery period), out follows Φ_1 to drop to 0 V through M7, M8 and outb follows Φ_1 to drop to 0 V through M9, M10.

By using bootstrapped NMOS transistors and the CMOS-latch structure, the DTCTGAL circuit ensures that the output always follows the power clock Φ_1 and Φ to change, eliminating the non-adiabatic energy consumption generated at the beginning of the evaluation period and the end of the energy recovery period, thereby reducing the energy consumption effectively.

3. Application of the DTCTGAL circuit

"XOR" and "XNOR" are important in Boolean logic, and their gate circuits are basic units in digital circuit design. The ternary XOR/XNOR truth table is shown in Table 1[12].

Suppose $\overline{\Phi}$ to be the clock-controlled clock, Φ_1 and Φ the power clocks, A, B the input signals, $\overline{A}$, $\overline{B}$ the complementary signals of A, B, ax, bx the sampled values of A, B, ay, by the sampled values of $\overline{A}$, $\overline{B}$ respectively. According to Eqs. (11)–(13), the function expressions of each sampled value can be obtained:

$$ax^+ = {}_A\langle\overline{\Phi}_H^{0.5}\rangle|_{\varepsilon=ax}, \tag{17}$$

$$bx^+ = {}_B\langle\overline{\Phi}_H^{0.5}\rangle|_{\varepsilon=bx}, \tag{18}$$

$$ay^+ = {}_{\overline{A}}\langle\overline{\Phi}_H^{0.5}\rangle|_{\varepsilon=ay}, \tag{19}$$

$$by^{+} = {}_{\overline{B}}\langle \overline{\Phi}_{\mathrm{H}}^{0.5} \rangle|_{\varepsilon = by}. \tag{20}$$

According to the switch-signal theory, the theory of three essential elements and table 1, the function expression of $A \oplus B$ can be obtained:

$$\begin{aligned}
\mathrm{out}^{+} &= A \oplus B = 2 \cdot ({}^{1.5}A \cdot B^{0.5} + A^{0.5} \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot A^{1.5} \\
&\quad + {}^{0.5}B \cdot B^{1.5}) + 0 \cdot (A^{0.5} \cdot B^{0.5} + {}^{1.5}A \cdot {}^{1.5}B) \\
&= 2 \cdot ({}^{1.5}A \cdot {}^{1.5}\overline{B} + {}^{1.5}\overline{A} \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} \\
&\quad + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot ({}^{1.5}\overline{A} \cdot {}^{1.5}\overline{B} + {}^{1.5}A \cdot {}^{1.5}B) \\
&= 2 \cdot ({}^{1.5}A \cdot {}^{1.5}\overline{B} + {}^{1.5}\overline{A} \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} \\
&\quad + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot {}^{1.5}(\overline{A} \cdot \overline{B} + A \cdot B).
\end{aligned} \tag{21}$$

Noting $\overline{A}\overline{B} + AB = A \odot B = \mathrm{outb}$ in the above equation, according to the characteristics of the DTCTGAL circuit, the complementary output signal is used to control the injection and recovery of energy by feedback, using Φ_1, Φ to substitute logic 1 and logic 2 respectively, Equation (21) can be expressed as follows:

$$\begin{aligned}
\mathrm{out}^{+} &= A \oplus B = \Phi \cdot ({}^{1.5}A \cdot {}^{1.5}\overline{B} + {}^{1.5}\overline{A} \cdot {}^{1.5}B + \mathrm{outb}^{0.5}) \\
&\quad + \Phi_1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot {}^{1.5}\mathrm{outb} \\
&= \Phi \cdot \left[{}^{1.5}(ax \cdot by) + {}^{1.5}(ay \cdot bx) + outb^{0.5}\right] + \Phi_1 \\
&\quad \cdot \left[{}^{0.5}(ax \cdot ay) + {}^{0.5}(bx \cdot by)\right] + 0 \cdot {}^{1.5}\mathrm{outb}.
\end{aligned} \tag{22}$$

The first, second, fourth, and fifth items of Eq. (22) show that the input sampled values *ax*, *ay*, *bx*, *by* are used to control Φ and Φ_1 to inject energy into the output and recover energy from the output; the third item shows that the complementary signal of the output signal is used to eliminate the high threshold loss when logic 2 is transmitted so as to reduce the energy consumption further; the sixth item shows that outb eliminates the float of out when out does not follow the power clock to change. Equation (22) can be expressed as follows:

$$\begin{aligned}
\mathrm{out}^{+} &= \Phi \cdot \left[(ax \cdot by)_{\mathrm{H}}^{1.5} + (ay \cdot bx)_{\mathrm{H}}^{1.5} + \mathrm{outb}_{\mathrm{L}}^{1.5}\right] \\
&\quad + \Phi_1 \cdot \left[(ax \cdot ay)_{\mathrm{H}}^{0.5} + (bx \cdot by)_{\mathrm{H}}^{0.5}\right] + 0 \cdot \mathrm{outb}_{\mathrm{H}}^{1.5} \\
&= {}_{\Phi}\langle ay_{\mathrm{H}}^{1.5} \rangle \uparrow \langle bx_{\mathrm{H}}^{1.5} \rangle \parallel \langle ax_{\mathrm{H}}^{1.5} \rangle \uparrow \langle by_{\mathrm{H}}^{1.5} \rangle \\
&\quad \parallel \langle outb_{\mathrm{L}}^{1.5} \rangle |_{\Phi_1} \langle ax_{\mathrm{H}}^{0.5} \rangle \uparrow \langle ay_{\mathrm{H}}^{0.5} \rangle \parallel \langle bx_{\mathrm{H}}^{0.5} \rangle \\
&\quad \uparrow \langle by_{\mathrm{H}}^{0.5} \rangle |_0 \langle \mathrm{outb}_{\mathrm{H}}^{1.5} \rangle |_{\varepsilon = \mathrm{out}}.
\end{aligned} \tag{23}$$

Using the same methods, the function expression of $A \odot B$ can be obtained:

$$\begin{aligned}
\mathrm{outb}^{+} &= A \odot B = 2 \cdot (A^{0.5} \cdot B^{0.5} + {}^{1.5}A \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot A^{1.5} \\
&\quad + {}^{0.5}B \cdot B^{1.5}) + 0 \cdot (A^{0.5} \cdot {}^{1.5}B + {}^{1.5}A \cdot B^{0.5}) \\
&= 2 \cdot ({}^{1.5}\overline{A} \cdot {}^{1.5}\overline{B} + {}^{1.5}A \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} \\
&\quad + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot ({}^{1.5}\overline{A} \cdot {}^{1.5}B + {}^{1.5}A \cdot {}^{1.5}\overline{B}) \\
&= 2 \cdot ({}^{1.5}\overline{A} \cdot {}^{1.5}\overline{B} + {}^{1.5}A \cdot {}^{1.5}B) + 1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} \\
&\quad + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot {}^{1.5}(\overline{A} \cdot B + A \cdot \overline{B}).
\end{aligned} \tag{24}$$

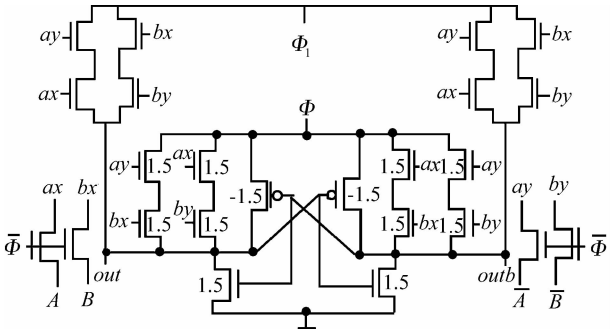

Fig. 3. XOR/XNOR circuit based on DTCTGAL.

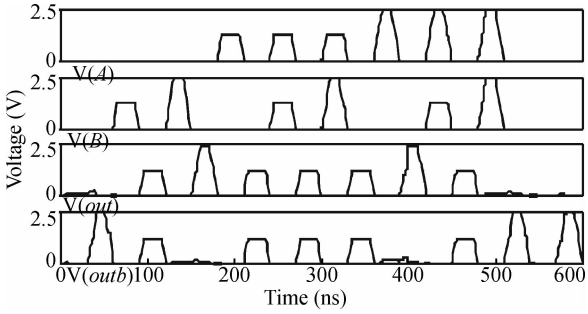

Fig. 4. Simulation waveforms of the XOR/XNOR circuit based on DTCTGAL.

Because $\overline{A}B + A\overline{B} = A \oplus B = \mathrm{out}$, the above equation can be further expressed as follows:

$$\begin{aligned}
\mathrm{outb}^{+} &= \Phi \cdot ({}^{1.5}\overline{A} \cdot {}^{1.5}\overline{B} + {}^{1.5}A \cdot {}^{1.5}B + \mathrm{out}^{0.5}) + \\
&\quad \Phi_1 \cdot ({}^{0.5}A \cdot {}^{0.5}\overline{A} + {}^{0.5}B \cdot {}^{0.5}\overline{B}) + 0 \cdot {}^{1.5}\mathrm{out} \\
&= \Phi \cdot [{}^{1.5}(ay \cdot by) + {}^{1.5}(ax \cdot bx) + \mathrm{out}^{0.5}] + \\
&\quad \Phi_1 \cdot [{}^{0.5}(ax \cdot ay) + {}^{0.5}(bx \cdot by)] + 0 \cdot {}^{1.5}\mathrm{out} \\
&= \Phi \cdot [(ay \cdot by)_{\mathrm{H}}^{1.5} + (ax \cdot bx)_{\mathrm{H}}^{1.5} + \mathrm{out}_{\mathrm{L}}^{1.5}] + \\
&\quad \Phi_1 \cdot [(ax \cdot ay)_{\mathrm{H}}^{0.5} + (bx \cdot by)_{\mathrm{H}}^{0.5}] + 0 \cdot \mathrm{out}_{\mathrm{H}}^{1.5} \\
&= {}_{\Phi}\langle ay_{\mathrm{H}}^{1.5} \rangle \uparrow \langle by_{\mathrm{H}}^{1.5} \rangle \parallel \langle ax_{\mathrm{H}}^{1.5} \rangle \uparrow \langle bx_{\mathrm{H}}^{1.5} \rangle \\
&\quad \parallel \langle \mathrm{out}_{\mathrm{L}}^{1.5} \rangle |_{\Phi_1} \langle ax_{\mathrm{H}}^{0.5} \rangle \uparrow \langle ay_{\mathrm{H}}^{0.5} \rangle \parallel \langle bx_{\mathrm{H}}^{0.5} \rangle \\
&\quad \uparrow \langle by_{\mathrm{H}}^{0.5} \rangle |_0 \langle \mathrm{out}_{\mathrm{H}}^{1.5} \rangle |_{\varepsilon = \mathrm{outb}}.
\end{aligned} \tag{25}$$

According to Eqs. (17)–(25), the corresponding XOR/XNOR circuit based on the DTCTGAL circuit can be drawn, as shown in Fig. 3.

4. Computer simulation and conclusion

Using the parameters of the TSMC 0.25 μm CMOS device, the DTCTGAL circuit and the XOR/XNOR circuit based on DTCTGAL designed above are simulated, where the amplitude voltages of the power clock Φ, Φ_1 correspond to 2.5 V, 1.25 V, and the device sizes of the NMOS and PMOS transistors are taken with $W/L = 0.36\ \mu$m/0.24 μm and $W/L = 0.72\ \mu$m/0.24 μm respectively. The simulation waveforms of the XOR/XNOR circuit based on DTCTGAL is shown in Fig. 4, where *A*, *B* are the input signals, and out, outb are the dual-rail complementary output signals. As shown in Fig. 4, the output

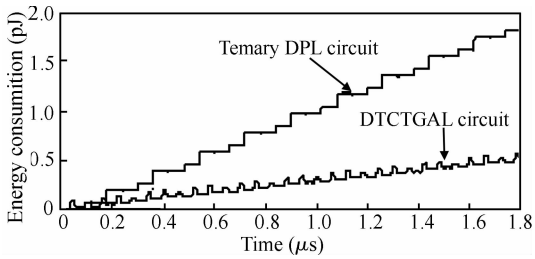

Fig. 5. Transient energy consumption comparison between DTCTGAL and ternary DPL.

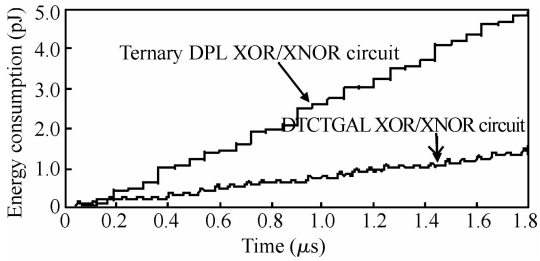

Fig. 6. Transient energy consumption comparison between DTCTGAL XOR/XNOR circuit and ternary DPL XOR/XNOR circuit.

signals are delayed by half a clock cycle compared to input signals, which is consistent with the characteristics of DTCTGAL circuits. When AB = 00, then out = 0, outb = 2; when AB = 01, then out = 1, outb = 1; when AB = 02, then out = 2, outb = 0; when AB = 10, then out = 1, outb = 1; . . . ; the rest can be followed by analysis of Fig. 4. The simulation results are consistent with Table 1, verifying the valid functionality of the XOR/XNOR circuit based on DTCTGAL.

Figure 5 gives a transient energy consumption comparison between the DTCTGAL and ternary DPL[11] (double pass-transistor logic) circuits, where the input in is "210210. . . ". The ascending parts of the curves indicate that the power clocks charge the circuit, while the descending parts denote energy recovery from the circuit to the power clock; the gradual rise of the concave bottoms in the curves shows the energy consumption of the circuit. The energy consumption of the ternary DPL circuit is 1.82 pJ in 1.8 μs while the energy consumption of the DTCTGAL circuit is 0.5 pJ, which shows an energy saving of 72%. Similarly, in Fig. 6, the energy consumption of the ternary DPL XOR/XNOR circuit is 4.83 pJ in 1.8 μs while the energy consumption of the DTCTGAL XOR/XNOR circuit is 1.14 pJ, which shows an energy saving of 76%. As can be seen from the analysis above, the circuits proposed in this paper have predominant characteristics of low power dissipation.

According to the energy recovery of low power character in adiabatic circuits and the high space utilization character of multiple-valued logic circuits, this paper has proposed a novel design for DTCTGAL circuits. The design achieves ternary input and output in an adiabatic circuit by using MOS transistors with different thresholds, and further extends it to the design of a ternary XOR/XNOR circuit. The scheme proposed in this paper can be further applied to design higher-radix multiple-valued circuits, so as to promote the development of multiple-valued logic circuits.

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