An 11 mW 79 dB DR ΔΣ modulator for ADSL applications*

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Abstract: This paper shows the design of a second-order multi-bit ΔΣ modulator with hybrid structure for ADSL applications. A modified two phase non-overlapping clock generator is designed to let PH2 borrow 12% of the time from PH1, which relaxes the speed of OTAs, comparators and the DEM block. The clock feed through problem of the passive adder is solved by revising the timing of the comparators and the adder. The chip is designed and fabricated in UMC 0.18 μm CMOS technology. Measurement results show that with an oversampling ratio of 32 and a clock rate of 80 MHz, the modulator can achieve 79 dB dynamic range, 71.3 dB SNDR, 11 mW power consumption from a 1.8 V power supply. The FOM is 1.47 pJ/step.

Key words: ΔΣ modulator; ΔΣ A/D; low power

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1. Introduction

Owing to the booming development of CMOS technology, the traditional opinion that ΔΣA/Ds only fit well in low speed high resolution applications has changed. ΔΣA/Ds used in data receivers are popular today, since they only need very simple anti-aliased filters and are compatible with today's VLSI technology. The signal bandwidth of discrete time ΔΣ modulators can now achieve 10 MHz[1] and that of continuous time ones can even reach 20 MHz[2]. ΔΣA/Ds can be used in many standard receivers such as ADSL[3], ISDB-T/DVB-T[4], and 802.11 n/WiMax[5]. High speed low power ΔΣ modulators have been a hot topic in recent research.

This work designs a 1.25 MHz signal bandwidth, 80 dB SNDR ΔΣ modulator with second-order multi-bit hybrid structure for ADSL applications. A modified two phase non-overlapping clock generator is designed to let PH2 borrow 12% of the time from PH1, which can relax the speed requirement for OTAs, comparators and DEM. The clock feed through problem of the passive adder is solved by revising the timing of the comparators and the adder. The modulator is designed and fabricated in 0.18 μm UMC 1P6M CMOS technology with 1.8 V power supply. Measurement shows that the modulator can achieve 79 dB dynamic range, 71.3 dB SNDR with an oversampling ratio of 32 and 80 MHz clock frequency. The FOM is 1.47 pJ/step.

2. Architecture

The feed forward structure of the ΔΣ modulator presented in Ref. [6] not only realizes the same transfer function as the traditional feedback structure, but also makes the outputs of the integrators consist of quantization noise only. Compared with the traditional feedback structure, the output range of the integrators can be reduced a lot. Thus, the specifications of output swing and gain linearity for OTA design can be greatly relaxed. However, the traditional feed forward structure needs a broad band amplifier after the passive adder to compensate the gain compress of the adder. Such an amplifier consumes a lot of power. In this design, a hybrid second-order structure which has two feed forward paths and two feedback paths is adopted[5]. A linear model is shown in Fig. 1. There are only two paths to be added before the quantizer. If both paths have the same gain, the compression factor will be 0.5. So the compression can be compensated by halving the reference voltage of the comparators. Thus, the comparison range is halved, making the input transistors of the comparators easier to keep in the saturation region. Besides, by choosing suitable coefficients, the output range of the integrators can consist of quantization noise only, which retains the advantage of the traditional feed forward structure.

For the quantizer, although multi-bit quantizers suffer from a linearity problem and need more comparators than single-bit quantizers, they can offer much better performance. First, they can greatly reduce the quantization noise and the output swing of each integrator. Second, they can reduce the OSR to get the same SNDR. Thus, the clock frequency can be set lower and power is saved. Third, they makes the structure more stable so that the overload (OL) level can become higher,

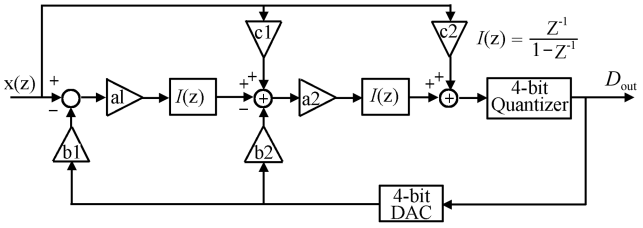

Fig. 1. Linear model of the second-order hybrid structure.

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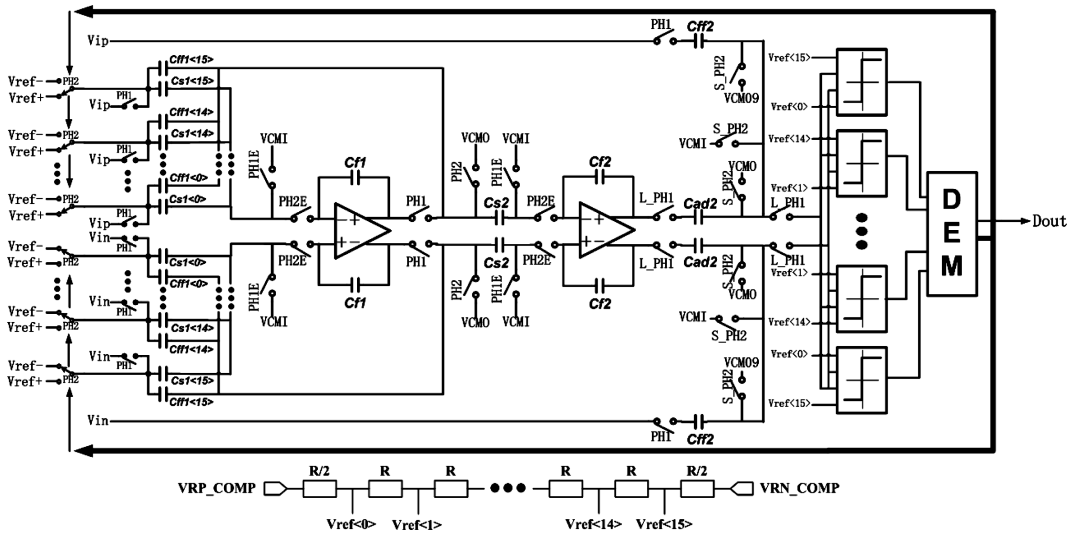

Fig. 2. Fully differential implementation of the ΔΣ modulator.

increasing the input dynamic range. In this work, a 4-bit quantizer with 16 comparators is chosen.

A larger oversampling ratio eases the design of the anti-aliasing filter preceding the modulator. However, a larger OSR needs a higher clock frequency, which leads to more digital power consumption. As a tradeoff, the OSR is chosen to be 32.

To find suitable coefficients for the structure, the signal transfer function (STF) is calculated by

$$\mathrm{STF}(z) = \frac{c_2 z^2 + (a_2 c_1 - 2c_2)z - a_2 c_1 + a_2 a_1 + c_2}{z^2 + (b_2 a_2 - 2)z - b_2 a_2 + a_1 b_1 a_2 + 1}. \quad (1)$$

Making STF equal 1 constrains the choice for the coefficients in the following way:

$$c_2 = 1, \;\; c_1 = b_2, \;\; b_1 = 1. \quad (2)$$

MATLAB is used for searching for suitable coefficients. The searching requirements are set to be: OL > 0.9, SNDR > 85 dB and output swing < 0.6. Since there are 16 comparators, for matching considerations, the coefficients are chosen to be:

$$a_1 = a_2 = 1, \;\; b_2 = c_1 = 1.6, \;\; b_1 = 1, c_2 = 1. \quad (3)$$

The simulation results show that the structure using the coefficients above can ideally reach 88 dB SNDR with 4 bit quantizer, OSR = 32 and OL = 0.9.

3. Circuit design

The circuit of the second-order discrete time modulator is depicted in Fig. 2. It is fully differential and consists of two switched-capacitor integrators, sixteen comparators, one DEM block, one two phase non-overlapping clock generator and one distributed 4 bit D/A converter. The sampling and feedback capacitors are shared. The realization of the coefficients a_1, b_1 and b_2, c_2 shares the switches since the switches all sample the input signal in the sampling phase and feed back the same V_{ref} in the integrating phase. Sharing the switches and capacitors makes the layout much simpler. The detailed concern of each circuit block is shown next in this section.

3.1. Sampling capacitors

There are four major kind of noise which should be considered when choosing the sampling capacitors. They are the thermal noise caused by the switches in the sampling phase and in the integrating phase, the thermal noise caused by the OTA and finally, the reference noise caused by the reference voltage sources. For this design, the sum of the noise above is about 5 kT/C_{s}[8], where k is Boltzmann constant, T is the temperature in Kelvin and C_{s} is the sampling capacitance. The SNR for the sum of the four noise sources is set to be 94 dB, which is 6 dB high than the peak SNDR of the quantization noise of the ideal structure. Thus, C_{s} of the first stage is chosen to be 103 fF × 16. Since the noise of the second stage can be reshaped by the loop transfer function, C_{s} of the second stage is chosen to be 51 fF × 10.

3.2. Switches

The non-zero sampling switch resistance and the sampling capacitor not only form a time constant which slows down the charge transfer, but also reduces the dominant closed-loop pole of the OTA[9]. Moreover, the non-linear sampling switch resistance will cause non-linearity of the modulator which leads to harmonic distortion and inter-modulation. The way to solve this problem is to make the switch resistance small or to use bootstrapping switches. In this paper, both ways are adopted. The sampling switches in the parallel branches are just CMOS switches and the resistances are chosen to be under 200 Ω, since each switch only needs to drive 1/16 of the total C_{s}. The sampling switches after the integrator output are chosen to be CMOS switches, too. Because the integrator output swing is small. The resistances are about 30 Ω. The bootstrapping switches are only used for the sampling switches in the feed forward path. The reason for this is that the voltage being sampled covers the full range from 0 to V_{dd}. CMOS

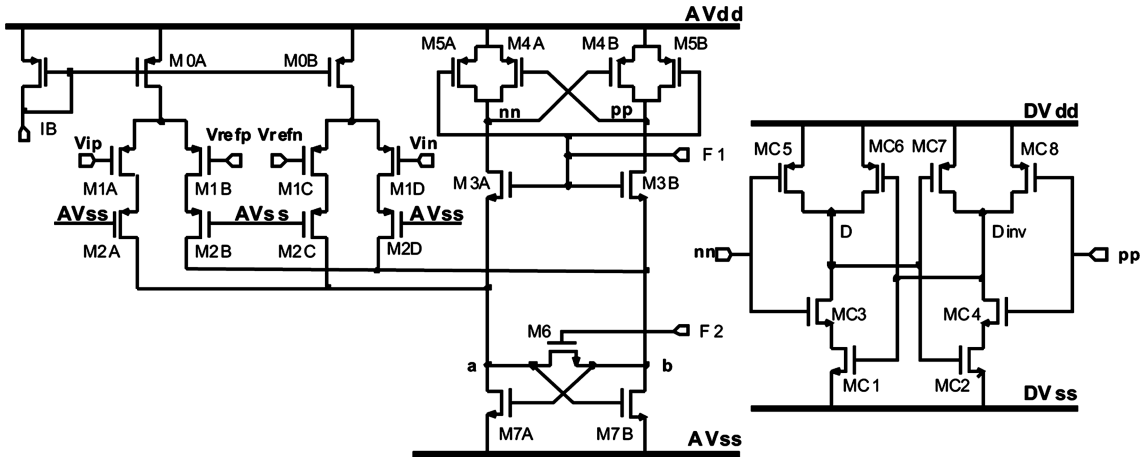

Fig. 3. Schematic of the comparator.

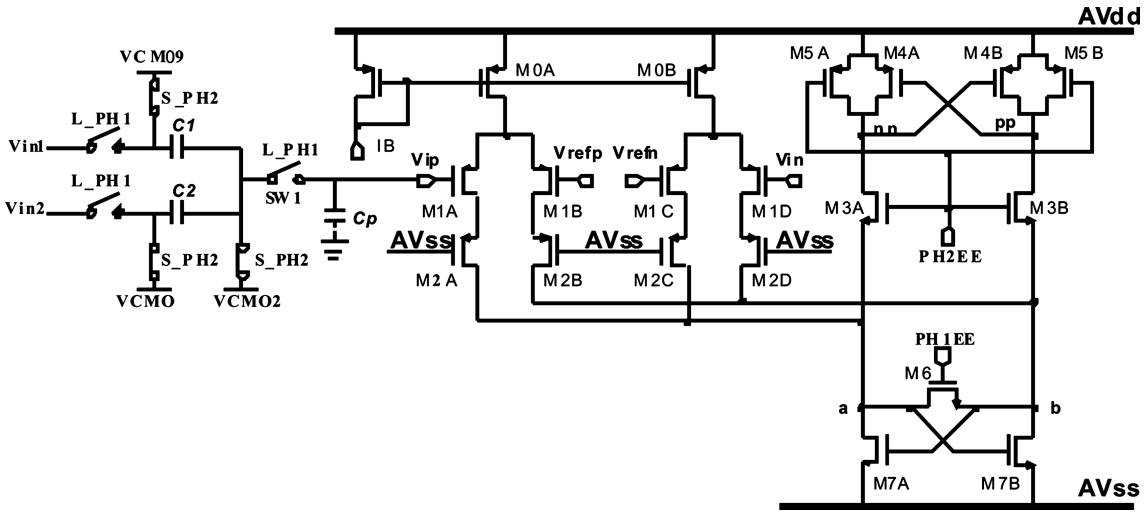

Fig. 4. Schematic of the adder and the comparator.

switches cannot reach good linearity over such a wide range.

3.3. OTA

The structure of the modulator requires the OTA gain to be moderate. The specifications of OTA output swing and gain linearity are quite relaxed; the reason for this is shown in section 2. Therefore, a telescopic OTA is the most suitable type. It has high power efficiency as well as low input noise. Since the OTA consumes most of the analog power, saving OTA power can greatly help to save the overall power consumption.

3.4. Comparator

The comparator schematic is shown in Fig. 3. It works in two non-overlapping phases and has two stages to regenerate. The comparison should be finished in less than 1/5 of the PH2 time after PH2 begins. The input capacitance of the comparators should be as low as possible to make the addition of the adder accurate while the Cff2 remains small. Therefore, the input transistor sizes are chosen to be 0.18 μm in length. Compared with the comparator shown in Ref. [10], the M2A, M2B, M2C, M2D are added to reduce the influence to the input nodes Vip and Vin by the voltage changing of nodes a and b. The static current of each comparator is only 11.25 μA, and the power is 20.25 μW. 16 comparators consume 324 μW in all, which is very low.

The biggest problem of the comparators is the clock feed through effect of the input node. The input node is the output of the passive adder, as shown in Fig. 4. In PH1, the adder does the addition and the comparators reset themselves. In PH2, the adder resets itself and the comparators work. During PH2, SW1 is open, so Vin and Vip are dynamic nodes during the comparison. At the falling edge of L_PH1, the voltage of Vin and Vip suddenly drops and cannot resume during the comparison. In this paper, a pair of early clocks PH1EE and PH2EE is designed to control the comparator and a pair of mended clocks L_PH1 (which is longer than PH1) and S_PH2 (which is shorter than PH2) is designed to control the passive adder. The timing diagram is shown in Fig. 5. The comparison starts earlier and the switches are turned off later than usual. So when clock feed through occurs, the comparison is almost done. Since in PH2 the adder resets itself, the side effect of PH2_S can be compensated by reducing the on-resistance of the switches, which does the reset.

3.5. Clock generator

A schematic and a timing diagram of the clock generator

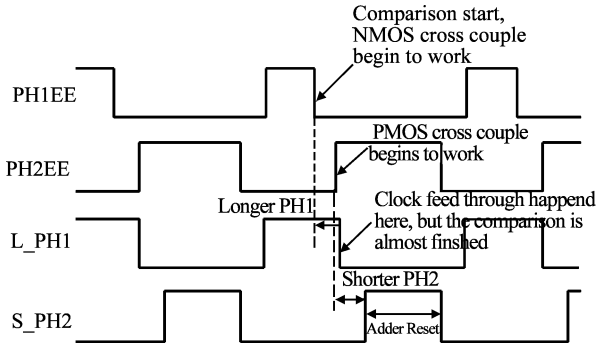

Fig. 5. Timing diagram of the comparator.

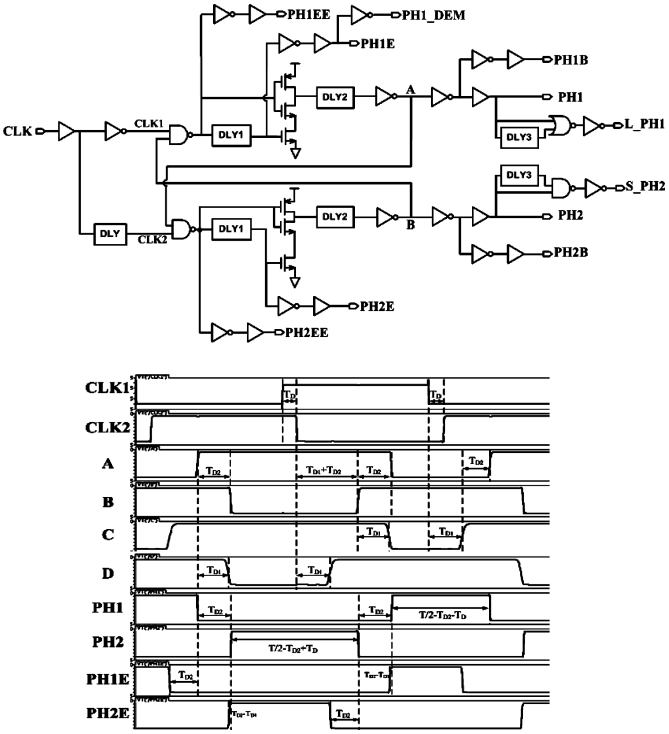

Fig. 6. Schematic and timing diagram of the clock generator.

are depicted in Fig. 6. Compared with a traditional two phase non-overlapping clock generator, another DLY unit is put in front of CLK2. This unit can change the pulse width of the two clock phases independently. The pulse width of PH1 now becomes $T/2-T_{\mathrm{DLY2}}-T_{\mathrm{DLY}}$ while PH2 becomes $T/2-T_{\mathrm{DLY2}}+T_{\mathrm{DLY}}$. In the feed forward structure, the operations of integration, comparison, and DEM all work in PH2 and only the sampling operation works in PH1. The time budget is quite tight for PH2 using an equal pulse width clock. However, if PH2 borrows some time from PH1, the speed requirements of the OTAs, comparators and DEM can be relaxed and the power consumption can be lowered. In this design, about 12% of PH1's pulse width is given to PH2. Since only the sampling operation works in PH1, reducing the sampling resistance can compensate the side effect of reducing the time of PH1.

The clock generator also generates PH1EE, PH2EE to control the comparator, and L_PH1 and S_PH2 to control the passive adder as mentioned in section 3.4.

3.6. DEM

Multi-bit ΔΣ modulators suffer from capacitance mismatch in D/A. Such an effect will cause deterioration of the SNDR of the modulator. One way to solve this problem is to use the dynamic element matching (DEM) technique[9]. In this design, data weighted averaging (DWA) is chosen for the DEM block. The block diagram is shown in Fig. 7. It consists of a Temperature to Binary encoder, a 4-bit adder and a shifter. The clock to control this block is the inverter of PH1E, which is PH1_DEM in Fig. 6.

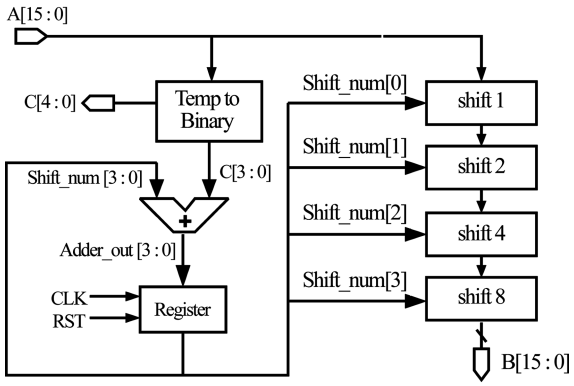

Fig. 7. Block diagram of DWA logic block.

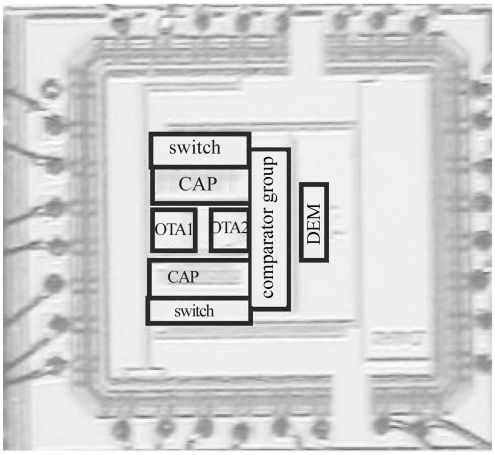

Fig. 8. Die photograph of the second-order ΔΣ

4. Experimental results

The second-order ΔΣ modulator has been fabricated in 0.18 μm 1P6M CMOS technology. The die photograph is shown in Fig. 8. The total die area including pads is 1.3 × 1.3 mm^2.

The performance of the modulator is evaluated by driving its input with a differential sinusoidal signal generated by a DS360 Ultralow Distortion Function Generator. The output 4-b digital signal is captured by an Agilent logic analyzer. The clock frequency is 80 MHz using crystal and the power supply is 1.8 V generated by LT3024. The peak SNDR measurement of the modulator is shown in Fig. 9. The peak SNDR can achieve 71.3 dB and SFDR can reach 79.2 dB with 80 kHz in put signal. The peak SNDR is 9 dB lower than the post simulation. There are many harmonics shown in the spectrum, which is mainly due to mismatch of the comparators. The THD is 72.1 dB, so the SNDR is mainly limited by the harmonic distortion. Figure 10 shows the input level versus SNDR. With a

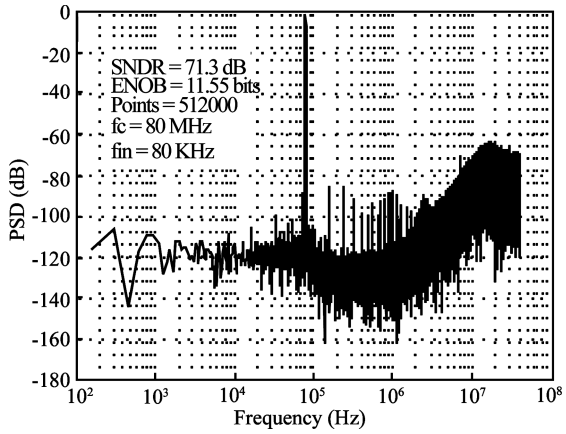

Fig. 9. Peak SNDR measurement.

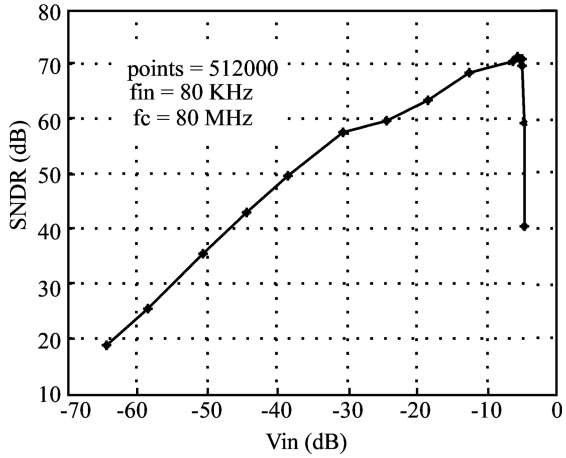

Fig. 10. Input level versus SNDR.

low input level, the SNDR is proportional to the input signal power in dB. However, with a high input level, such a relationship changes because of the harmonics. The dynamic range of the modulator is 79 dB. A summary of the measured performance is shown in Table 1.

5. Conclusion and future work

In this paper, a complete design for a second-order multi-bit hybrid structure switched-capacitor ΔΣ modulator is presented. A modified two phase non-overlapping clock generator is designed to let PH2 borrow 12% of the time from PH1, which relaxes the design of the OTAs, comparators and DEM. The clock feed through problem of the passive adder is solved by revising the timing of the comparators and the adder. The modulator can achieve 79 dB DR and 71.3 dB peak SNDR in measurements with 1.8 V power supply, 1.25 MHz signal bandwidth and 80 MHz clock rate. The power consumption is 11 mW and the FOM is 1.47 pJ/step.

Table 1. Measured performance summary of the ΔΣ modulator.

Parameter	Value
Peak SNDR	71.3 dB
Dynamic range	79 dB
Peak SFDR	79.2 dB
Sampling rate	80 MHz
Oversampling ratio	32
Signal band	20–1.25 MHz
Supply voltage	1.8 V
Total power consumption	11.07 mW
Analog power consumption	2.62 mA × 1.8 V = 4.716 mW
Digital power consumption	3.53 mA × 1.8 V = 6.354 mW
FOM	1.47 pJ/step
Total area	1.3 × 1.3 mm^2
Technology	UMC 0.18 μm 1P6M CMOS

To get better SFDR, the mismatch of the comparators should be considered in future design. Since digital circuits consume more power than analog circuits, more advanced technology could be used to reduce the digital power.

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