A four-channel microelectronic system for neural signal regeneration*

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Abstract: This paper presents a microelectronic system which is capable of making a signal record and functional electric stimulation of an injured spinal cord. As a requirement of implantable engineering for the regeneration microelectronic system, the system is of low noise, low power, small size and high performance. A front-end circuit and two high performance OPAs (operational amplifiers) have been designed for the system with different functions, and the two OPAs are a low-noise low-power two-stage OPA and a constant-g_m RTR input and output OPA. The system has been realized in CSMC 0.5-μm CMOS technology. The test results show that the system satisfies the demands of neuron signal regeneration.

Key words: implanted; neuronal signal; regeneration; detecting; stimulating

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1. Introduction

It is well known that the nerves in the spinal cord are hard to regenerate if crushed or injured.

With the rapid development of semiconductors, microelectronics is being applied more and more in the study of neuronal signal recording and nerve stimulation. Many research results have been reported all over the world[1–4]. Our research group has realized a bridging system for the spinal cord function recovery, and undertaken further research on the microscopic study of neuronal population by means of a monolithic integrated MEA (microelectrode array). In general, the bridging system contains interfaces, front-end circuits, a neuronal signal amplifier, a neuronal signal processor, FES (function electric stimulation), and a power supply module.

The bridging system for the injured nerve bundle can be formed by two microelectrode arrays of the cuff-type, Utah-type and so on, which can form multi signal channels, and a microelectronic circuit, which has bidirectional signal regeneration channels[4, 5].

The electrode contacts of the two microelectrode arrays are interfaced with two stumps of the broken nerve bundle. Some contacts are used for neural signal detection, and connected with the signal input of the channel on one direction in the microelectronic circuit. The remaining contacts are used for neural function electrical stimulation and connected with the signal output of the channel on the other direction in the microelectronic circuit. Thus a bidirectional neural signal channel bridge is formed. The neural signals will be regenerated in the up- and down-directions, and the neural function can be rebuilt.

The fundamental concept of nerve function rebuilding should be based on some research, minimally invasive surgery, implant surgery, compatibility of implanted devices, high performance microelectronic systems, method of power supply, study of long-term effect and so on. The function of the microelectronic system should include nerve signal detection and electric function stimulation.

A common detecting circuit in bio-potential measurements is a DC-coupled fully differential amplifier followed by a differential amplifier, as in the classical three op-amp instrumentation amplifier. The environment of the implanted microelectronics can be complicated. The nerve action potential coupled from a microelectrode array should be in the magnitude of microvolts, with the frequency below 10 kHz. The input resistance of the equivalent voltage source will be 5–30 kΩ. The ECG (electrocardiogram) signal and EMG (electromyogram) signal will also be coupled into the detecting circuit if not considered carefully. The interface between the microelectrode and the organism can have a large DC offset, which can influence the work of the detecting circuit. The input stage should therefore be AC coupled, and the lowest frequency could be at about 1 Hz. One thing that should be considered carefully is the power dissipation, because the organism is sensitive to temperature and the power supply is a piece of hard engineering[6].

The basic requirements for implanted devices in the body should be small size, low-voltage and low-power working, and ability to implant without any external connections[7–9]. For consideration of implantation for spinal cord signal

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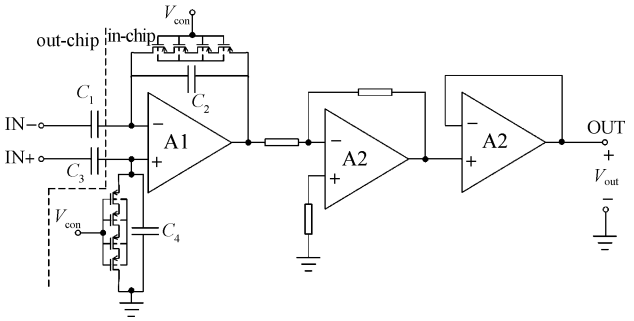


Fig. 1. Three-stage voltage stimulating regeneration system.

recording and stimulation, the regeneration microelectronic system should be designed with a low-noise, high precision, and ac-coupled amplifier and a voltage stimulating circuit with a low inner resistance or a current stimulating circuit with a high inner resistance.

In this paper, a neuronal signal regeneration system designed in a standard 0.5 μm CMOS process (CSMC, Wuxi, China) is presented. In the following sections, the system architecture, the circuit and layout design, and the test result will be discussed.

2. System design

The regeneration system contains several modules with different functions. The neuronal signal detected by a microelectrode is very weak, several to hundreds of microvolts. It should be amplified to a high enough amplitude at first. Then, it is supplied to another microelectrode to stimulate a spinal nerve.

According to the consideration of system demands, a three-stage voltage stimulating regeneration system was designed[10–12]. Figure 1 shows the schematic of the system. It contains a detecting circuit, a gain circuit, and a stimulating circuit. The ac-coupled input stage was implemented by a MOS-resistance in parallel with a capacitance. As the basic cell of the circuits, two OPAs (operational amplifiers) were designed with low power, low noise, small size, high gain, and high CMRR. In Fig. 1, A1 is a low-power and low-noise two-stage OPA, and A2 is a constant-g_m, rail-to-rail input and output OPA. They were used in different modules.

3. Circuit techniques

From Fig. 1, it is known that the basic cells of both the detecting and stimulating circuits are OPAs. Therefore, the key part of the circuit is the design of high performance OPAs. In addition, the front-end of the system is important for ac-coupling. The biasing circuit and start-up circuit used by two OPAs are also discussed.

3.1. Front-end circuit

Figure 2 shows the front-end circuit, with $C_1 = C_3$, $C_2 = C_4$, $R_{mos1} = R_{mos2} = R_{mos}$. In this design the circuit has two functions: to realize ac-coupling by means of a blocking

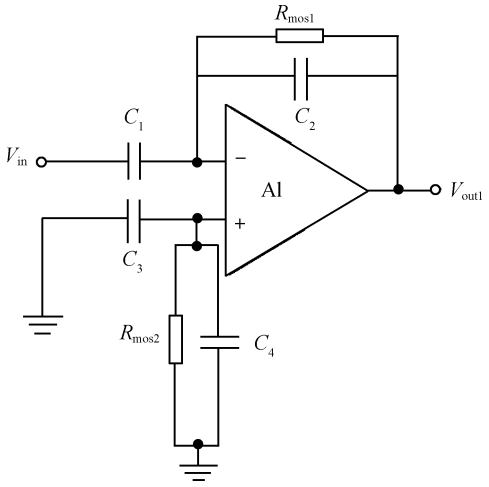


Fig. 2. Front-end circuit.

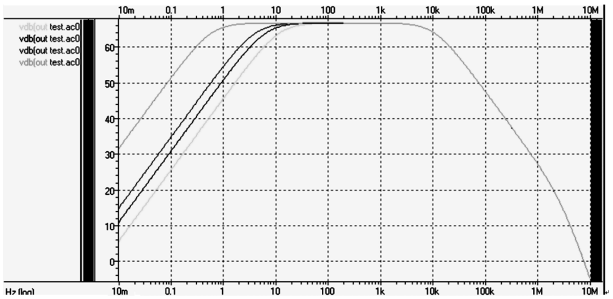


Fig. 3. Simulated amplitude–frequency curves of the system: the curve represents the gain, from top to bottom, V_{CON} = –1.5, –1.8, –2, –2.5 V.

capacitance, and to define the gain of the preamplifier.

$$A_{VPRE} = -C_1/C_2. \tag{1}$$

Because the on-chip capacitance will be in the pico-farad magnitude, the low frequency components will be hard to pass. Therefore, series of MOSFETS are used to realize ultrahigh resistances. The MOSFETs work in a linear area by means of V_{GS} control. The resistance R_{mos} can be expressed as

$$R_{mos} = \frac{1}{\mu C_{ox}(V_{GS} - V_T)W/L}, \tag{2}$$

and the −3 dB frequency is:

$$f_{-3dB} = \frac{1}{2\pi R_{mos} C_2}. \tag{3}$$

Figure 3 is the simulated amplitude–frequency curves of the system, with V_{GS} = –1.5, –1.8, –2, –2.5 V. The curves show that the pass-band is from 1 Hz to 10 kHz, when V_{con} is –1.5 V.

3.2. Low-noise low-power two-stage OPA

Figure 4 shows the schematic of the low-noise low-power two-stage OPA. According to the cascade noise formula, the noise of the first-stage differential input transistor is critical for the system. In our design, PMOS were adopted as an input pair for their lower noise coefficient than that of their NMOS counterpart. Further, an NMOS inverter with current-mirror load

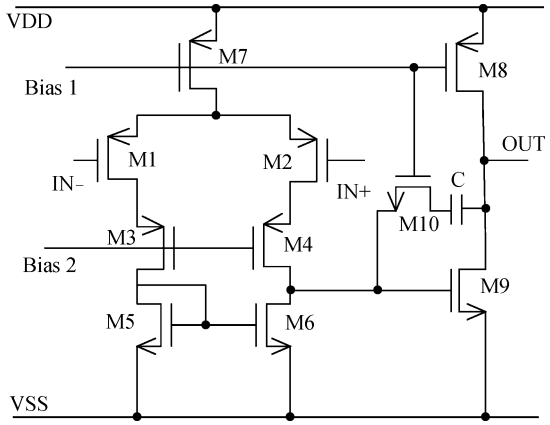


Fig. 4. Circuit schematic of the low-noise low-power two-stage OPA.

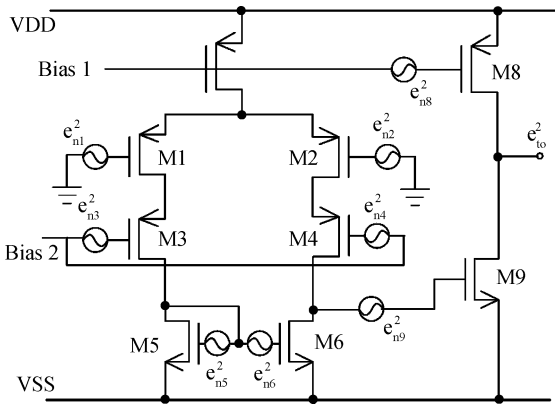


Fig. 5. Noise module of the amplifying circuit.

was adopted as the output stage. Functionally, the input stage provides high gain and the output stage ensures large output voltage swing. The open-loop OPA has a gain of

$$A_{\mathrm{V}} = \{-g_{\mathrm{m1}}\left[(g_{\mathrm{m3}}r_{\mathrm{ds3}}r_{\mathrm{ds1}}) \parallel r_{\mathrm{ds6}}\right]\} \parallel [-g_{\mathrm{m9}}\,(r_{\mathrm{ds8}} \parallel r_{\mathrm{ds9}})]. \quad (4)$$

The equivalent input noise can be deduced as follows.

Figure 5 shows the noise module of the amplifying subcircuit. First, neglecting the DC source noise, the equivalent output noise spectral density e_{to}^2 is:

$$e_{\mathrm{to}}^2 = g_{\mathrm{m9}}R_{\mathrm{II}}^2\left[e_{\mathrm{n8}}^2 + e_{\mathrm{n9}}^2 + R_{\mathrm{I}}^2\left(g_{\mathrm{m1}}^2e_{\mathrm{n1}}^2 + g_{\mathrm{m2}}^2e_{\mathrm{n2}}^2 + g_{\mathrm{m5}}^2e_{\mathrm{n5}}^2 + g_{\mathrm{m6}}^2e_{\mathrm{n6}}^2 + \frac{e_{\mathrm{n3}}^2}{r_{\mathrm{ds1}}^2} + \frac{e_{\mathrm{n4}}^2}{r_{\mathrm{ds2}}^2}\right)\right]. \quad (5)$$

Differential gain is $g_{\mathrm{m1}}R_{\mathrm{I}}g_{\mathrm{m9}}R_{\mathrm{II}}$; the equivalent input noise e_{eq}^2 is:

$$e_{\mathrm{eq}}^2 = \frac{e_{\mathrm{to}}^2}{g_{\mathrm{m1}}g_{\mathrm{m9}}R_{\mathrm{I}}R_{\mathrm{II}}} = \frac{2e_{\mathrm{n9}}^2}{g_{\mathrm{m1}}^2R_{\mathrm{I}}^2} + 2e_{\mathrm{n1}}^2\left[1 + \frac{g_{\mathrm{m5}}^2}{g_{\mathrm{m1}}^2}\left\|\left(\frac{e_{\mathrm{n5}}^2}{e_{\mathrm{n1}}^2}\right)^2 + \frac{e_{\mathrm{n3}}^2}{g_{\mathrm{m1}}^2r_{\mathrm{ds1}}^2e_{\mathrm{n1}}^2}\right.\right] \quad (6)$$

and $e_{\mathrm{n1}}^2 = e_{\mathrm{n2}}^2$, $e_{\mathrm{n3}}^2 = e_{\mathrm{n4}}^2$, $e_{\mathrm{n5}}^2 = e_{\mathrm{n6}}^2$. From the equation, the noise of the second stage can be neglected, because it is divided by the gain of the first stage. The noise of cascade transistors m3 and m4 also can be neglected, because it is divided by $(g_{\mathrm{m1}}r_{\mathrm{ds1}})^2$. So the equivalent input noise e_{eq}^2 can be

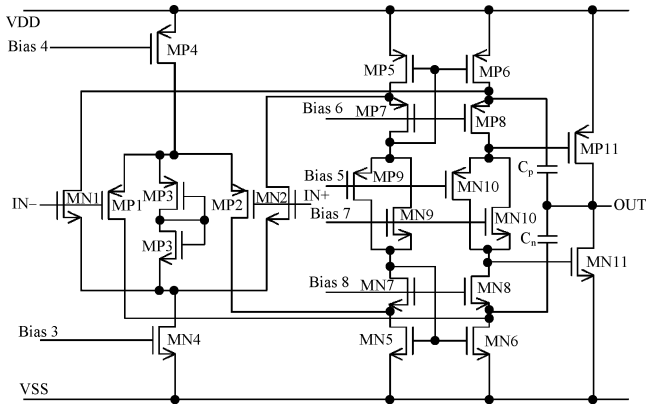


Fig. 6. Circuit schematic of the constant-g_m rail-to-rail input and output OPA.

expressed as

$$e_{\mathrm{eq}}^2 \approx 2e_{\mathrm{n1}}^2\left[1 + \left(\frac{g_{\mathrm{m5}}}{g_{\mathrm{m1}}}\right)^2\left(\frac{e_{\mathrm{n5}}^2}{e_{\mathrm{n1}}^2}\right)\right]. \quad (7)$$

The $1/f$ noise module of the MOSFET is:

$$e_{\mathrm{ni}}^2 = \frac{KF}{2fC_{\mathrm{ox}}W_{\mathrm{i}}L_{\mathrm{i}}K'} = \frac{B}{fW_{\mathrm{i}}L_{\mathrm{i}}}. \quad (8)$$

and the transconductance is:

$$g_{\mathrm{mi}} = \sqrt{\left(2K'\frac{W_{\mathrm{i}}}{L_{\mathrm{i}}}\right)|I_{\mathrm{D}}|}. \quad (9)$$

So Equation (7) can be expressed as:

$$e_{\mathrm{eq1}/f}^2 = 2e_{\mathrm{n1}}^2\left[1 + \left(\frac{K_{\mathrm{N}}'B_{\mathrm{N}}}{K_{\mathrm{P}}'B_{\mathrm{P}}}\right)\left(\frac{L_1}{L_5}\right)^2\right]. \quad (10)$$

From Eq. (10), the product of W_1 and L_1 should be large enough. So e_{n1}^2 can be minimized. The minimum value of the equivalent input noise should be $2e_{\mathrm{n1}}^2$, adjusting the ratio of L_1 to L_5.

The thermal noise module of the MOSFET is:

$$e_{\mathrm{ni}}^2 \approx \frac{8kT}{3g_{\mathrm{m}}},$$

$$e_{\mathrm{eqthermal}}^2 = 2e_{\mathrm{n1}}^2\left[1 + \frac{g_{\mathrm{m5}}}{g_{\mathrm{m1}}}\left(\frac{e_{\mathrm{n5}}^2}{e_{\mathrm{n1}}^2}\right)\right] = 2e_{\mathrm{n1}}^2\left[1 + \sqrt{\frac{K_{\mathrm{N}}'W_3L_1}{K_{\mathrm{P}}'W_1L_3}}\right], \quad (11)$$

where $K' = \mu C_{\mathrm{ox}}$, and k is the Boltzmann constant. Equation (11) shows that the method for reducing $1/f$ noise also reduces thermal noise.

3.3. Constant-g_{m} rail-to-rail input and output OPA

Figure 6 shows the schematic of the constant-g_{m} rail-to-rail input and output OPA. The OPA is designed for the demands of low voltage and full swing of input and output range. In this design, a kind of feed-forward input stage for constant conductance and gain is adopted. The conductance g_{m} is kept unchanged within the dynamic rail-to-rail range.

Figure 7 shows the feed-forward input-stage of the OPA[13]. MP1 and MP2 build up a PMOS different input pair,

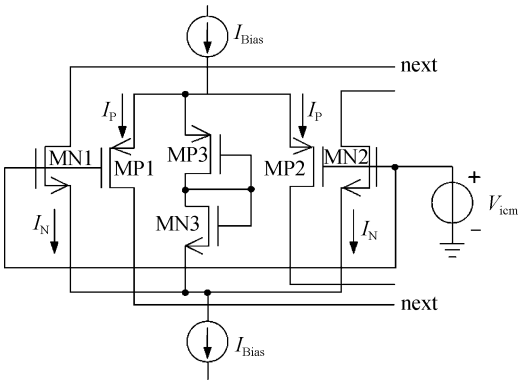


Fig. 7. Circuit schematic of the feed-forward input stage.

MN1 and MN2 build up an NMOS different input pair, MP3 and MN3 form a diode. MP1, MN1, MP3, and MN3 form a feed-forward close-loop. The constraint relation is:

$$\begin{aligned} &V_{GS(MP1)} + V_{GS(MN1)} = V_{GS(MP3)} + V_{GS(MN3)}, \\ &V_{GS} - V_T = \sqrt{\frac{I_D}{\mu C_{ox}(W/L)}}. \end{aligned} \tag{12}$$

Define the four input transistors MP1, MN1, MP2, MN2 to have the same value of $K = K_N^{'} W_{N1}/2L_{N1} = K_N^{'} W_{N2}/2L_{N2} = K_P^{'} W_{P1}/2L_{P1} = K_P^{'} W_{P2}/2L_{P2}$, and MP3, MN3 to have a value of $6K$. The equation can be expressed as

$$\sqrt{\frac{I_P}{K}} + \sqrt{\frac{I_N}{K}} = \sqrt{\frac{I_{Bias} - 2I_N}{6K}} + \sqrt{\frac{I_{Bias} - 2I_P}{6K}}, \tag{13}$$

where $I_N = I_P = I_{Bias}/8$. A MOSFET has a transconductance of $g_m = \sqrt{(2K^{'}W/L)|I_D|(1 + \lambda V_{DS})}$, so we have

$$g_m = g_{mN} + g_{mP} = \sqrt{4KI_N} + \sqrt{4KI_P} = \sqrt{2KI_{Bias}}. \tag{14}$$

So, the W/L of each MOSFET can be adjusted for the constant g_m. The gain is also kept approximately constant. The OPA has a gain of

$$\begin{aligned} A_V = &\left(g_{mn1} + g_{mp1}\right)\left\{\left[g_{mp8} r_{op8}\left(r_{op6} \parallel r_{on1}\right)\right] \parallel \right. \\ &\left.\left[g_{mn8} r_{on8}\left(r_{on6} \parallel r_{op1}\right)\right]\right\}\left(g_{mn11} + g_{mp11}\right)\left(r_{op11} \parallel r_{on11}\right) \\ = &\sqrt{2KI_{Bias}}\left\{\left[g_{mp8} r_{op8}\left(r_{op6} \parallel r_{on1}\right)\right] \parallel \left[g_{mn8} r_{on8}\left(r_{on6} \parallel \right.\right.\right. \\ &\left.\left.\left. r_{op1}\right)\right]\right\}\left(g_{mn11} + g_{mp11}\right)\left(r_{op11} \parallel r_{on11}\right). \end{aligned} \tag{15}$$

The function of the feed-forward circuit is to extract part of the input bias current I_{Bias} from MP3 and MN3 in a timely manner. When the input differential pair is worked in a saturation region, the bias current of the pair is $I_{Bias}/4$. The feed-forward circuit is $3I_{Bias}/4$. Equation (14) is met. When the input common-mode voltage is high, the PMOS pair is shut down, and the common-source terminal of NMOS is elevated by the input common-mode voltage. So the feed-forward circuit cannot conduct and the current extracted from I_{Bias} is zero. Then $I_N = I_{Bias}$, so Equation (14) is met again. Similar, when the input common-mode voltage is low, $I_P = I_{Bias}$. So Equation (14) is met when the input common-mode voltage changes.

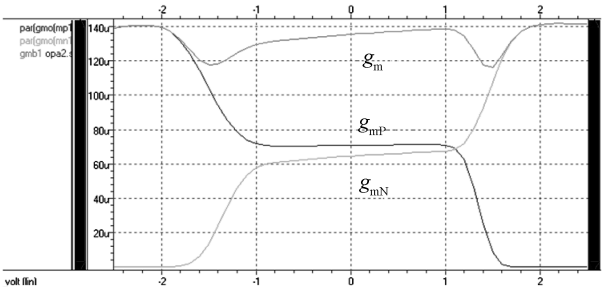


Fig. 8. Simulation curve of g_{mN}, g_{mP} and g_m.

Figure 8 shows the simulation curve of g_{mN}, g_{mP}, and g_m. The result shows that g_m is nearly constant within the common-mode voltage V_{icm} from rail-to-rail. The variation of g_m is within 9.2%.

To make efficient use of the supply voltage and current, the OPA requires class-AB biased output transistors connected in a common-source configuration. As can be seen from Fig. 6, the class-AB output stage consists of two common-source connected output transistors, which are directly driven by two in-phase signal currents. Floating current sources are adopted in the summing circuit stage.

Ignoring the noise of the biasing current source, the equivalent input noise of the input NMOS pair and PMOS pair are e_{ninn}^2 and e_{ninp}^2, respectively:

$$\begin{aligned} e_{ninn}^2 &= e_{nn1}^2 + e_{nn2}^2 + \frac{g_{mn5}^2 e_{nn5}^2 + g_{mn6}^2 e_{nn6}^2 + g_{mp5}^2 e_{np5}^2 + g_{mp7}^2 e_{np7}^2}{g_{mn1}^2}, \\ e_{ninp}^2 &= e_{np1}^2 + e_{np2}^2 + \frac{g_{mp5}^2 e_{np5}^2 + g_{mp6}^2 e_{np6}^2 + g_{mn5}^2 e_{nn5}^2 + g_{mn7}^2 e_{nn7}^2}{g_{mp1}^2}. \end{aligned} \tag{16}$$

Therefore, according to the $1/f$ and thermal noise modules, the L of MN5, MN6, MP5, MP6 and the W of MN1, MN2, MP1, MP2 should be designed with a large size and the decreased noise.

3.4. Biasing circuit and start-up circuit

The robustness of the biasing sub-circuit is very important in the design of an OPA. By analysis and simulation, the biasing output in this design is stable with variations of power, temperature and process corners. In order to solve the idle-state problem of the biasing and amplifying sub-circuit, a start-up sub-circuit was designed. Figure 9 shows the schematic of the biasing sub-circuit and start-up sub-circuit.

4. Chip design and simulation

The four-channel regeneration system has been realized in a 0.5-μm CMOS process of CSMC (Wuxi, China). The NMOS transistors and the PMOS transistors with short channel have target threshold voltages of 0.87 and 0.97 V, respectively. The layout of the one-channel system is shown in Fig. 10. The BIAS is the layout of the biasing circuit and start-up circuit, A1 is the layout of the low-noise low-power two-stage OPA, and A2 is the layout of the constant-g_m rail-to-rail

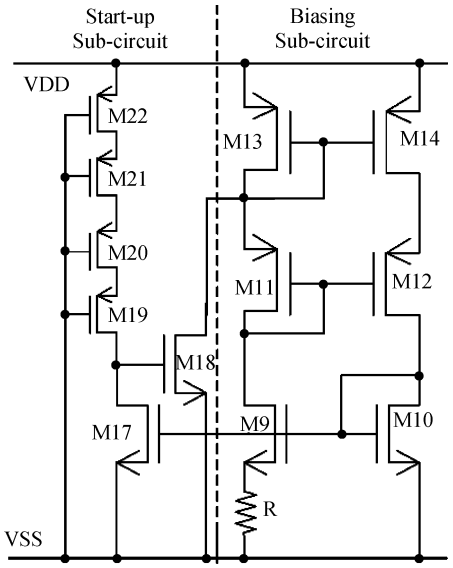


Fig. 9. Circuit schematic of the biasing sub-circuit and start-up sub-circuit.

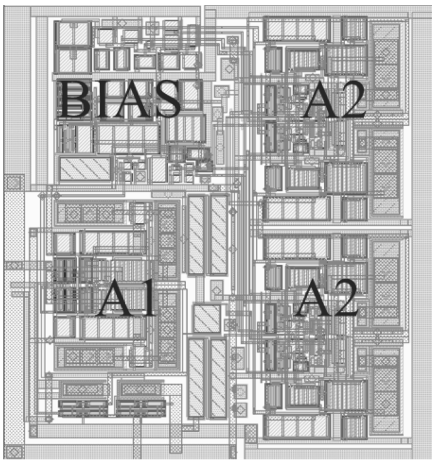


Fig. 10. Layout of the one-channel generation system. Area: 324 × 344 μm^2.

Table 1. Simulation results of one of the four-channel regeneration systems.

Parameter	Value
Supply voltage	±2.5 V
Output range	−2.5 to +2.5 V
Power	4.1146 mW
Equivalent input noise (not including $1/f$ noise) @ 100 Hz	19.3 nV/$\sqrt{\text{Hz}}$
Area	0.324 × 0.344 mm^2

input and output OPA.

Table 1 shows the simulation results of the one-channel regeneration system. Because the technology library does not include $1/f$ noise parameters, the simulation result of the equivalent input noise does not include $1/f$ noise.

The layouts and simulation results show that the designed system is of low power, low noise and small size. A micrograph of the realized four-channel regeneration system is shown in Fig. 11. The chip area is 1.21 × 1.286 mm^2. All four channels were tested, with the same test condition. All of them work well. Figure 12(a) shows the output signal with a gain of 67.9 dB and a rail-to-rail amplitude, and the input signal is of ECG pulse form with V_{in} = 2 mV and f = 10 Hz. Figure 12(b) shows the output signal with a gain of 65.7 dB, and the input signal is of a sine waveform with V_{in} = 2 mV, and f = 1 kHz. Because the waveform generator used for the test is Agilent 33220, the minimum signal amplitude is 20 mV, and a 20-dB attenuator was used to attenuate the signal to 2 mV, thus giving

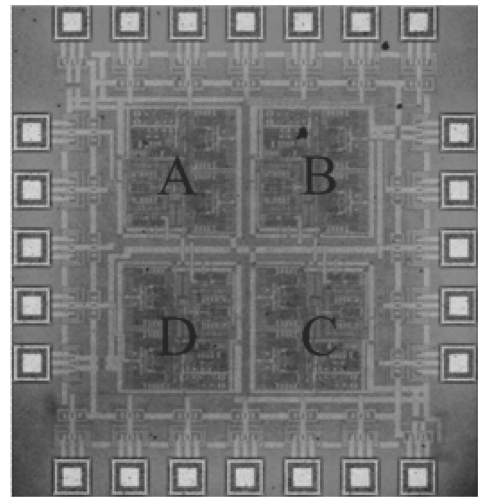
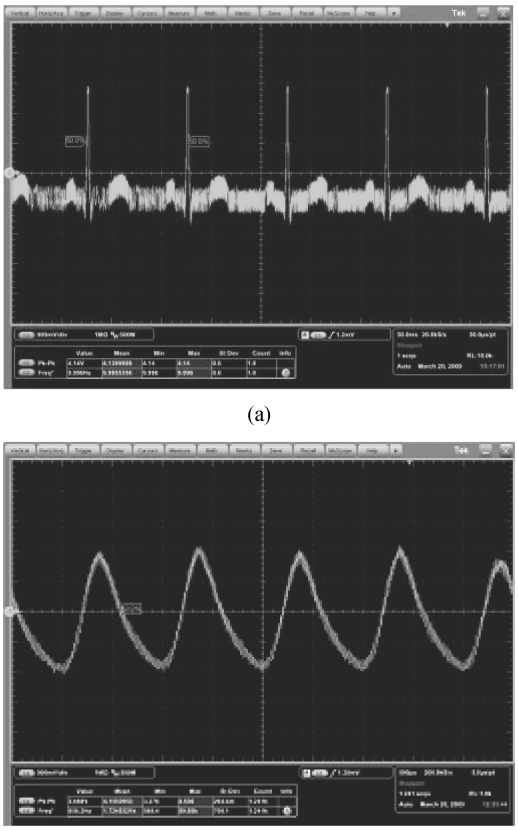


Fig. 11. Micrograph of the four-channel regeneration system. Area: 1.21 × 1.286 mm^2.



(a)

(b)

Fig. 12. Waveform graphs of the four-channel regeneration system test: (a) Input signal is ECG with V_{in} = 2 mV, f = 10 Hz; (b) Input signal is sine signal with V_{in} = 2 mV, f = 1 kHz.

a high noise level. If attenuated more, the noise becomes larger than the signal and cannot be recognized by the oscilloscope. The test results show that the regeneration system satisfies the demand of neuronal signal detecting.

5. Summary

A microelectronics system has been designed for the signal regeneration of injured spinal cord. As the basic cells, two OPAs were designed basically with low noise and low power and were used for different functions. The chip has been realized in CSMC 0.5-μm CMOS technology. The test results show that the chip works well.

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