Rotary traveling-wave oscillator design using 0.18 μm CMOS

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Abstract: A rotary traveling-wave oscillator (RTWO) targeted at 5.8 GHz band operation is designed and fabricated using standard 0.18 μm CMOS technology. Both simulation and measurement results are presented. The chip size including pads is 1.5×1.5 mm^2. The measured output power at a frequency of 5.285 GHz is 6.68 dBm, with a phase noise of −102 dBc/Hz at 1 MHz offset from the carrier.

Key words: rotary traveling-wave oscillators; multiphase oscillators; CMOS
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1. Introduction

The design of clock networks has become one of the most important parts that constrain chip performance. With the decrease of feature size in the CMOS process and the increase of operation frequency on chip, the transmission line effects of interconnects become more obvious and cannot be neglected, which seriously affects the performance of clock distribution networks. For this purpose, rotary traveling-wave oscillators (RTWOs) were recently proposed as a new transmission line approach for multi-gigahertz clock generation[1]. Further research has shown that compared to more conventional H-tree based clocking topology, clock network design with much lower power consumption can be achieved employing RTWOs[2,3].

On the other hand, the RTWO has also found applications in voltage controlled oscillator (VCO) design[4, 5]. One remarkable feature of RTWO-based VCO design is that differential multiphase (360°) waves with uniform amplitude can be obtained with ease, which provides great flexibility in the choosing of architecture for successive circuit blocks. Moreover, by employing the geometric programming based optimization design methodology proposed in Ref. [3], extreme power saving (up to 85%) compared to the original power-unaware RTWO design is possible.

In this paper, an RTWO targeted at 5.8 GHz band operation is designed and fabricated using SMIC 0.18 μm CMOS technology. The theory of RTWO structure and modeling is presented. The detailed design of the fabricated RTWO, along with the simulated results, is given.

2. Theory of rotary traveling-wave oscillator

2.1. Fundamentals and structures

The basic structure of the RTWO is a rotary ring composed of a differential transmission line as shown in Fig. 1(a). The transmission line is cross-connected at point "A" and works in odd mode to ensure a reversed feedback such that signal inversion occurs after each one round delay of τ. Assuming a lossless transmission line, once started, oscillation will continue with a period of 2τ forever. Square waves with known relative phases can be obtained simply by tapping into the transmission line, either single-endedly or differentially. Practically, multiple cross-coupled inverter pairs are distributed along the transmission line to compensate for any possible energy losses. The inverter pairs also enforce the odd mode operation for the differential line and sustain the phase locking.

One of the proposed applications for the RTWO is to interconnect multiple RTWOs into rotary oscillator arrays[1], which offer a scalable architecture with the potential for low-power low-skew global clock distribution over an arbitrary chip area. As shown in Fig. 1(b), all the individual RTWOs oscillate at the same frequency, while synchronization is achieved by hard wiring between abutting rings which forces phase locking. Clock signals are obtained from the nearest RTWO for further local distribution.

2.2. Equivalent distributed circuit model

For the efficient analysis of RTWO, the transmission line is modeled as multiple RLC segments each loaded by one inverter pair. Figure 2(a) shows the lumped equivalent model of one segment of length Δl with all significant high frequency components and parasitics, where R_0, L_0, C_{11}, C_{22}, and C_{12} are per-unit-length resistance, inductance, self capacitances and mutual capacitance, respectively.

Accordingly, the equivalent capacitance per unit length is:

$$C_0 = C_{\text{tran\_perlen}} + C_{\text{inv\_perlen}} = C_{11} + 2C_{12} + 2C_{\text{inv}}/\Delta l, \quad (1)$$

where C_{inv} is the equivalent capacitance of one inverter pair. With the help of an equivalent capacitance circuit for the loaded differential transmission line segment as shown in Fig. 2(b), we can obtain the expression for C_{inv}:

$$\begin{aligned} C_{\text{inv}} &= \left(C_{\text{gsP2}} + C_{\text{dsP1}}\right) \parallel \left(C_{\text{gsP1}} + C_{\text{dsP2}}\right) + \left(C_{\text{gsN2}} + C_{\text{dsN1}}\right) \\ &\quad \parallel \left(C_{\text{gsN1}} + C_{\text{dsN2}}\right) + C_{\text{dgN1}} + C_{\text{dgP1}} + C_{\text{dgP2}} + C_{\text{dgN2}} \\ &= \left(C_{\text{gsP1}} + C_{\text{dsP1}} + C_{\text{gsP2}} + C_{\text{dsP2}} \right. \\ &\quad \left. + C_{\text{gsN2}} + C_{\text{dsN1}} + C_{\text{gsN1}} + C_{\text{dsN2}}\right)/4 \\ &\quad + C_{\text{dgN1}} + C_{\text{dgP1}} + C_{\text{dgP2}} + C_{\text{dgN2}}, \end{aligned} \quad (2)$$

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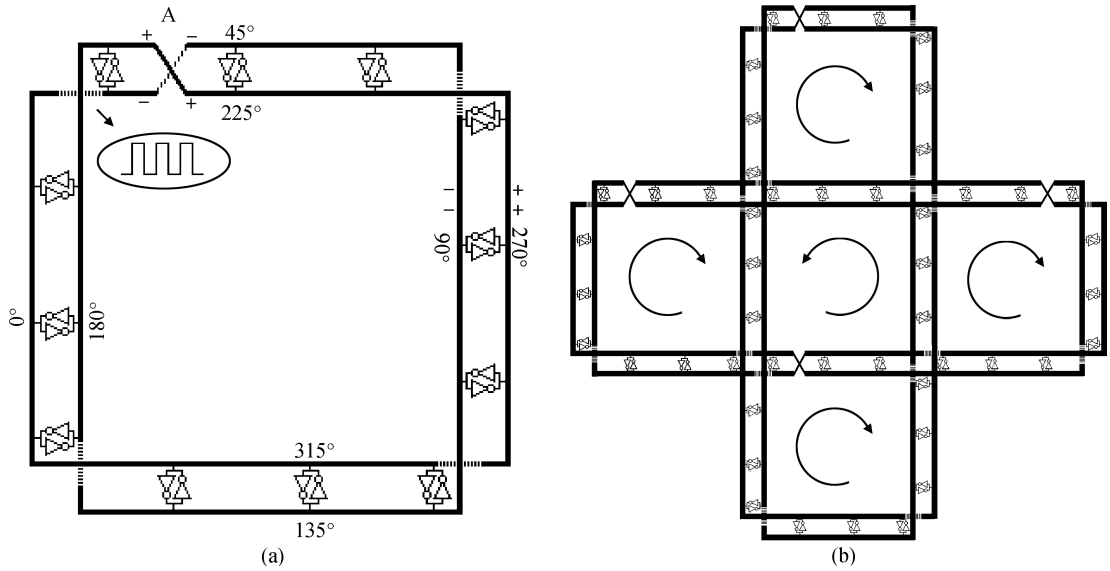

Fig. 1. (a) Rotary traveling-wave oscillator structure. (b) Rotary oscillator arrays.

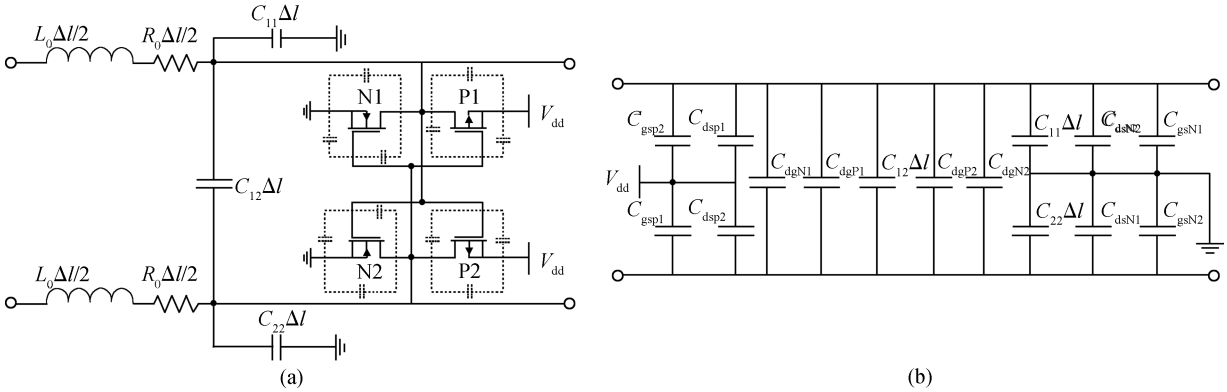

Fig. 2. (a) Lumped RLC model for one short transmission line segment of length Δl. (b) Equivalent capacitance circuit.

where C_{dg} is the gate overlap and Miller-effect feedback capacitance, C_{gs} is the total channel capacitance, and C_{ds} is the drain depletion capacitance to bulk (substrate). Note that the /4 factor is used to convert the in-parallel "to ground" capacitance value into an in-series differential value[1].

The per-unit-length differential inductance L_0 is calculated using the analytic expression from[6]:

$$L_0 = \frac{\mu_0}{\pi} \ln\left(\frac{\pi \times s}{w + T_c} + 1\right), \tag{3}$$

where s is the conductor separation, w is the conductor width, and T_c is the conductor thickness which is a constant of 2.17 μm for the SMIC 0.18 μm process.

Thus for a low-loss transmission line working in odd mode, the characteristic impedance Z_{odd} and propagation coefficient γ can be derived as follows:

$$Z_{odd} = \sqrt{L_0/C_0}, \quad \gamma = j\omega\sqrt{L_0 C_0}. \tag{4}$$

2.3. Oscillation frequency and power dissipation

With the phase velocity of the traveling wave being

$$v_p = \frac{1}{\sqrt{L_0 C_0}}, \tag{5}$$

the oscillation frequency f_{osc} is given approximately by:

$$f_{osc} = \frac{v_p}{2l} = \frac{1}{2l\sqrt{L_0 C_0}} = \frac{1}{2N\Delta l\sqrt{L_0 C_0}}, \tag{6}$$

where l is the total length of the differential transmission line and N is the number of inverter pairs. The $\times 2$ factor arises from the traveling wave requiring two complete rotations for a cycle.

Once the oscillation is established, the majority of power dissipation is due to the energy losses on the transmission line, which is shown to contribute to more than 80% of the total power consumption[2]. This can be explained by the fact that unlike a ring oscillator, the energy that goes into charging and discharging MOS gate capacitance becomes transmission line energy and is recirculated. As losses on the transmission line are related to I^2R instead of CV^2f, potential power saving is possible. Thus the power dissipation of an RTWO is governed by:

$$P_r = \frac{V_{dd}^2}{Z_{odd}^2} R_{loop}, \tag{7}$$

where R_{loop} is the series loop resistance of the RTWO ring. It is obvious that maximizing Z_{odd} and minimizing R_{loop} are of

Table 1. Design parameters of the proposed RTWO.

Design parameter		Value
Transmission line	Conductor width (w)	10 μm
	Conductor separation (s)	15 μm
	Loop length (l)	3500 μm
Inverter pair	NMOS channel width (w_n)	3 μm
	PMOS channel width (w_p)	9 μm
	NMOS and PMOS channel length	0.18 μm
	NMOS and PMOS finger number (f_n)	10
	Number of inverter pairs (N)	12

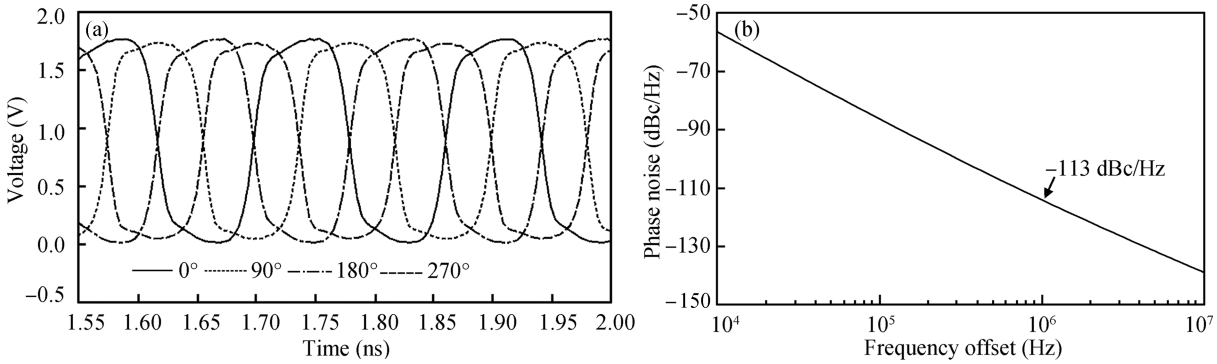

Fig. 3. (a) Simulated output waveforms. (b) Simulated phase noise performance.

the utmost importance for power reduction.

3. RTWO design

3.1. Design parameters and simulation

In this paper, an RTWO is designed with a targeted operation frequency band of 5.8 GHz. As shown in Fig. 1(a), there are twelve cross-coupled inverter pairs distributed along the RTWO ring. Table 1 shows the detailed parameters, which have been obtained using a similar methodology to that introduced in Ref. [3].

Figure 3(a) shows the simulated output waveforms taken from four symmetrical positions on the RTWO ring, whose relative phases range from 0° to 270°, with a phase difference of 90°. Just as mentioned above, multiphase output waveforms with uniform amplitude can be generated with ease using an RTWO. The oscillation frequency simulated is 5.68 GHz. The phase noise performance results as shown in Fig. 3(b) read that phase noise at 1 MHz offset from the carrier is –114 dBc/Hz.

3.2. Layout considerations

The proposed RTWO is implemented in standard 1P6M 0.18 μm CMOS technology with a 2.17 μm Al top metal layer. Figure 4 shows a microphotograph of the fabricated circuit. The total chip size including pads is 1.5 × 1.5 mm^2, which has been mainly constrained by the length of the RTWO ring. The transmission line is realized using microstrip structure with a metal-6 layer on top of a metal-1 layer to eliminate the non-ideal effects of the substrate. The conductors are relatively wide in order to minimize resistive losses of the rather thin metal-6 layer to reduce power consumption. To minimize the MOS gate resistance, all inverter pairs are multifinger structures. Finally, the whole structure is protected by a guardring.

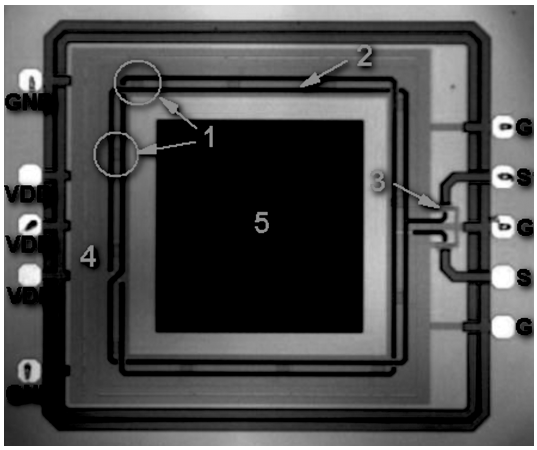

Fig. 4. Microphotograph of the fabricated RTWO. 1: Inverter pairs; 2: Transmission line (metal-6); 3: Output buffer; 4: VDD net (metal-2) GND net (metal-1); 5: Dummy.

4. Experimental results

To characterize the performance of the proposed RTWO, on-wafer probing using DC and differential HF-probes was performed. The output power spectrum was measured with an Agilent E4440A spectrum analyzer. As shown in Fig. 5, the RTWO oscillates at a frequency of 5.285 GHz with an output power of 6.68 dBm. The deviation in the oscillating frequency from the simulated result is caused mainly by the excess capacitive parasitic loading effect from the inverter pairs which the simulation models have failed to account for accurately. The results also show that the single side band phase noise at 1 MHz offset from the 5.285 GHz carrier is –102 dBc/Hz, which is 11 dBc/Hz higher than that predicted by simulation.

Table 2. Performance summary of the high-frequency RTWOs.

Parameter	This work	Ref. [1]	Ref. [4]	Ref. [5]
Process	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Frequency (GHz)	5.285	3.38	18	32
V_{DD} (V)	1.8	2.5	1	1.2
DC power (mW)	129	210	14.4	54
Phase noise @ 1-MHz (dBc/Hz)	–102	–	–117.3	–108
Output power (dBm)	6.68	–	–10.7	–9.1

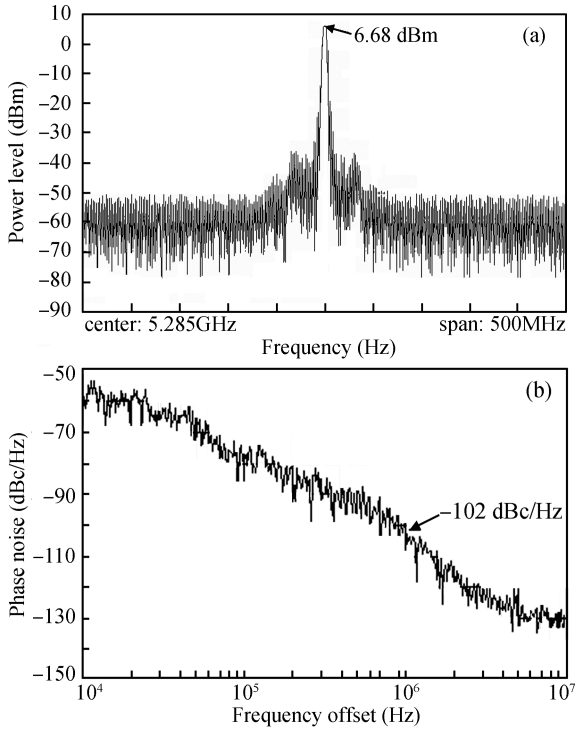

Fig. 5. (a) Measured output power spectrum. (b) Measured phase noise.

The same measurement was performed on five samples of the fabricated chips. The results show that the oscillation frequencies can range from 5.285 to 5.366 GHz, with a maximum relative difference of 1.5%. While this diversity of oscillation frequencies can be explained mainly by process variation, an on-chip frequency tuning mechanism could have been employed to counteract this effect. For this purpose, multiple MOS varactors in parallel with the inverter pairs can be used.

Table 2 lists the performance summary of the proposed circuit along with results from state-of-the-art RTWOs for comparison. The experimental results also indicate that if V_{DD} of 1.2 V is used, the DC current can be reduced from 72 to 25 mA, resulting in a DC power of 45 mW.

5. Conclusion

In this paper, an RTWO targeted at 5.8 GHz band operation is successfully implemented using standard 0.18 μm CMOS technology. While the feasibility of RTWO design at this frequency band using standard CMOS technology is proved, it should be noted that an RTWO-based circuit will be more advantageous for higher frequencies applications. With the increase in oscillating frequency, the length of the RTWO ring is decreased, which improves the efficiency. Our simulation results for an 11.8 GHz RTWO design have shown that a phase noise of about –120 dBc/Hz at 600 kHz offset can be achieved. Finally, the chip size will be much smaller.

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