

A variable step-down conversion ratio switched capacitor DC–DC converter for energy harvesting systems working in intermittent mode

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Abstract: Energy harvesting systems stimulate the development of power management for low power consumption applications. Improving the converter efficiency of power management circuits has become a significant issue in energy harvesting system design. This paper presents a variable step-down conversion ratio switched capacitor (SC) DC–DC converter to advance the converter efficiency of charge on the stored capacitor in a wireless monitoring system of orthopedic implants. The converter is designed to work at 1 MHz switching frequency and achieves 15 to 2 V conversion. Measurement results show that the converter efficiency can reach 42% including all circuit power consumption, which is much higher than previous work.

Key words: energy harvesting system; switched-capacitor DC–DC converter; piezoelectric elements

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1. Introduction

As the power requirements of microelectronics continue to decrease, it is possible to supply systems by harvesting energy from ambient environments. The micro energy harvesting system has been widely used in low power applications, including smart medical micro systems and wireless sensor network nodes.

In wireless monitoring systems of orthopedic implants, charge generated by piezoelectric (PZT) elements is used to supply energy^[1], in which the PZT elements are also used as sensors to detect abnormal high amounts of force, and other conditions of the orthopedic implants. Due to poor source characteristics (high voltage, low current, high impedance) of the PZT elements, the requirements of power management circuit are critical.

To store energy on capacitors is widely used in energy harvesting system designs. To advance charge efficiency of the stored capacitor can evidently improve the converter efficiency of the whole system. A linear voltage regulator is used in Ref. [2] to make the electrical energy in the stored capacitor into a usable power supply, whose efficiencies are 19%. Reference [3] uses forward-switching to regulate the electrical energy, and the power converter efficiency is about 17.6%, which is still not high enough.

In order to make full use of the power generated by the PZT elements and to improve converter efficiency, a variable step-down conversion ratio switched capacitor DC–DC converter circuit working in intermittent mode is proposed, which minimizes the number of off-chip components and is well suited for monolithic integration. The proposed circuit has a higher conversion efficiency than linear regulators over the entire supply voltage range. Furthermore, by reducing the switching (clock) frequency, the total power losses can be re-

duced down to zero, while preserving a good no-load output voltage regulation. The DC–DC converter is controlled with a voltage monitor system to automatically adjust working mode or standby mode. When the voltage on the stored capacitor is not high enough to drive the system, the converter goes into standby mode to save energy until the voltage across the capacitor is high enough. Then, invalid energy loss is decreased in intermittent working mode, which is ideally suited for power management circuits in energy harvesting systems.

We also describe the system-level design of the power management units and provide concrete circuit details of the DC–DC converter system. Design issues associated with the converter efficiency of the system are described in detail.

2. Power converter system architecture

The proposed circuit structure of the DC–DC converter is shown in Fig. 1. It consists of several functional blocks, a bandgap reference (BGR), a variable step-down conversion ratio switched-capacitor (SC) converter, a voltage ratio controller, an oscillator, a clock controller and an output voltage monitor supplied by V_{IN} , which is the voltage across the storage capacitor.

The PZT electronic power stored on a big storage capacitor (C -store) is regulated by the proposed power converter after being rectified by a full-wave bridge rectifier. The voltage ratio controller, which is composed of resistances, comparators and logic circuits, is used to monitor the input voltage value to set the step-down conversion ratio. The variable step-down conversion ratio SC converter dynamically scales according to the voltage across the storage capacitor. The output voltage monitor serves as a voltage detector by sending a signal to enable or disable clock signal in order to confine output voltage. The oscillator and the driver circuits generate the non-overlapping

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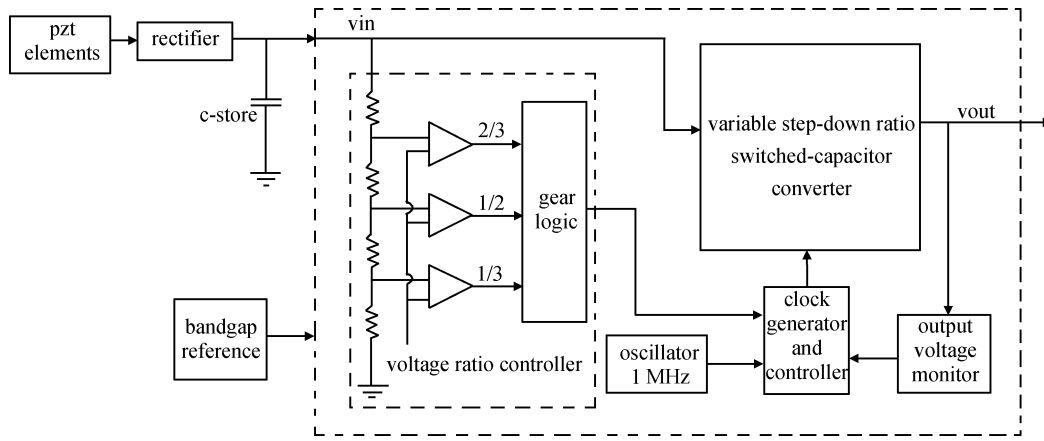


Fig. 1. Circuit structure of the DC-DC converter.

stacked clocks used in the SC converter. The BGR provides precise bias current and reference voltage for the other circuits.

Compared to power converters with both inductive and capacitive energy storage, SC DC-DC converters have several advantageous properties. First, without magnetic components, they are well suited for monolithic integration. Second, operation down to zero-load is possible with no need for dummy loads or complex control techniques. When completely unloaded, the SC converter output voltage assumes a value uniquely determined by the converter topology.

However, it is difficult to ensure output voltage regulation in the presence of wide load variations, especially on the condition of input voltage variations. Continuous voltage regulation can be achieved, at the expense of degrading the converter efficiency. For a single step-down conversion ratio topology, the SC converter limits the maximum efficiency that can be achieved to $\eta_{lin} = (1 - V_o/V_{nl})$, where V_{nl} is the no-load voltage for this topology. The bigger difference between V_o and V_{nl} , the smaller the maximum efficiency that can be achieved by this topology. This is a fundamental problem with switching capacitor DC-DC converters. Thus, in order to improve efficiency, it is necessary to switch in different topologies (different step-down conversion ratios) whose no-load output voltage is closer to the output voltage desired. The variable step-down conversion ratio SC topologies will be discussed in detail in the next section.

The proposed SC converter works in intermittent mode. The threshold voltage of the power converter system is set to be 5 V. When the voltage across the stored capacitor is lower than 5 V, the power converter will be in standby mode until the piezoelectric elements charges the stored capacitor above the threshold voltage. Otherwise, when the output voltage across the stored capacitor is higher than 5 V, when necessary, the power converter begins to work.

3. Circuit design

3.1. Charge pump DC-DC circuit

The switched capacitor (SC) converter in this design is used to dynamically scale the charged capacitor supply from 5–15 to 2 V. As shown in Fig. 2, flying capacitors (C1, C2) are

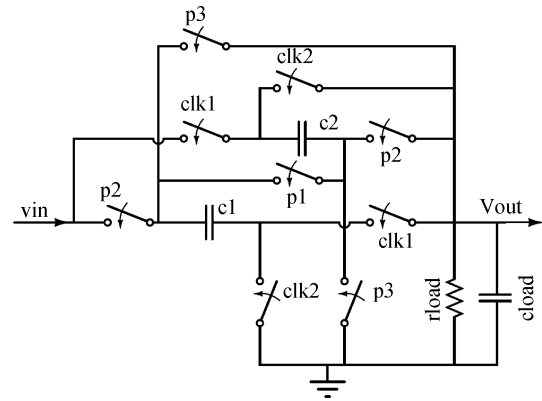


Fig. 2. Circuit structure of SC converter.

Table 1. Relation between control signals and step-down conversion ratio.

| V_{DD}/V_{out} | 1/3 | 1/2 | 2/3 |
|------------------|-----|-----|-----|
| A | 0 | 1 | 1 |
| B | 1 | 2 | 0 |

equal in value and they transfer charge from the storage capacitor to the load. The SC converter can work on several ratios of step-down functions, 2/3, 1/2 and 1/3. All of these different functions use the same capacitor topology, which will be set to different topologies according to different clock sequence combinations. The circuit topology of the SC converter is discussed in Ref. [4] in detail; two logic-level signals A and B are generated by the voltage ratio controller to select different step-down conversion ratios. p1, p2 and p3 are the logic combinations of A, B, clk1 and clk2, as illustrated in Table 1.

Equation (2) depicts the relationship between p1, p2, p3 and other signals:

$$\begin{aligned}
 p1 &= \text{clk1} \cdot \bar{A} + \text{clk2} \cdot \bar{B}, \\
 p2 &= \text{clk1} \cdot A, \\
 p3 &= \text{clk2} \cdot B.
 \end{aligned}
 \tag{2}$$

With a non-zero load at the output of an SC converter, the steady-state output voltage (in absolute value) is lower than the ideal unloaded value, which reduces converter efficiency. In a steady state, all capacitors in the converter are periodically charged and discharged in order to supply the output current

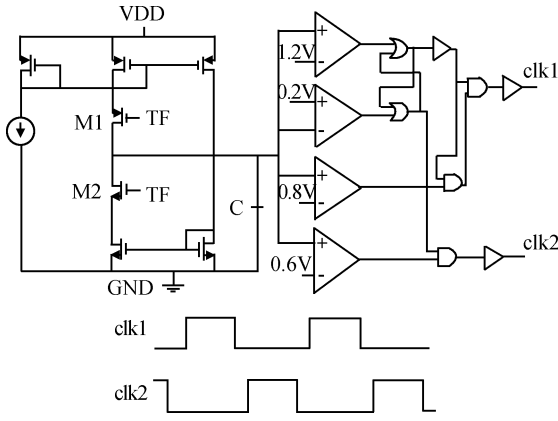


Fig. 3. Circuit structure of oscillator^[5].

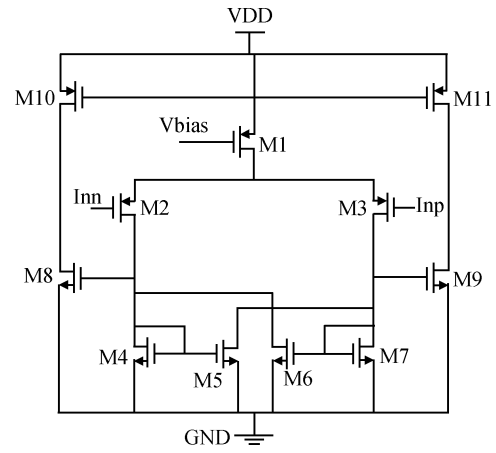


Fig. 4. Hysteresis comparator circuit.

to load. As a result, capacitor voltages now have an ac ripple component. Energy is lost on the capacitor and the switch on-resistances during each charge transfer to or from a capacitor. Furthermore, when the ac components in capacitor voltages are large enough, the drain voltage or source voltage of the transistors used as switches would be higher than the supply voltage, and the parasitic pn junction will be forward biased, which will lead to the possibility of leaking current. To set a small charge-transfer capacitor is an effectual approach to minimize the ac components. This approach will reduce the ripple output voltage. However, the minimum value of charge-transfer capacitor is also limited by the maximum load current. So properly setting the capacitor values is important in the design of a switched-capacitor DC–DC converter.

3.2. Stacked clock generator

Proper clock sequences are helpful to suppress the leakage current. An oscillator circuit generates the complex clock sequence used in the SC converter as shown in Fig. 3. The four input levels of those four hysteresis comparators are generated by the bandgap reference. Several logic operations of hysteresis comparator outputs are used to implement the clock scheme. TF, which is generated by non-overlapping clocks (ck1 and ck2) and the outputs of comparators after several specific logic operations, is the signal to control turning on or off of M1 and M2, changing the charge stored in capacitor C and forming an oscillator. One of the advantages of this oscillator is that this scheme automatically realizes the controlled clock. When the output voltage of SC is lower than the settled value, by the control of TF signal, it will be convenient to achieve the enablement of clock, and then restart the SC converter. In contrast, when the output of SC is higher than the settled value, the clock will be disabled through the control of the TF signal^[5].

The hysteresis comparator is applied to reduce the DC offset and noise in the oscillator, which is shown in Fig. 4. M4, M7 and M5, M6 are cross-coupled bi-stable current sources as load. The ratios of width to length of M5 and M6 are larger than those of M4 and M7. M8–M11 consists of the second stage, which acts as two inverters to increase drive capacity. In the voltage ratio controller and the output voltage monitor, the same hysteresis comparators are used to detect voltage values.

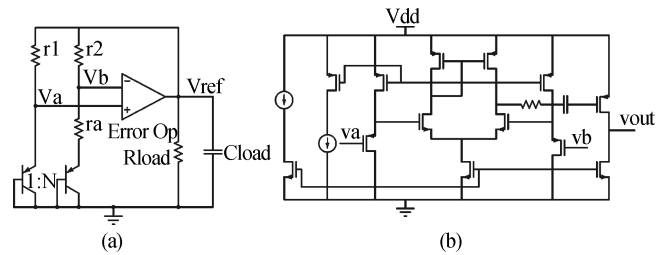


Fig. 5. Concrete circuit of (a) BGR and (b) error operational amplifier.

3.3. BGR circuit

The BGR circuit is a basic and very important component in analog and mixed signal circuits. It provides precise bias current and reference voltage in order to make the oscillator of the SC and voltage monitors work correctly. As mentioned before, the converter is working in the high-voltage region. Compared with devices working in the low-voltage region, the same supply current consumes more power. So an ultra-low supply current of the BGR is preferred here. Figure 5 shows the concrete circuit of the BGR and the error operational amplifier used in the BGR.

In the BGR, the resistors r_1, r_2 enforce branch currents equal to proportional-to-absolute-temperature (PTAT), which is generated by Q_1, Q_2 and r_a when $V_a = V_b$ is enforced by an operational amplifier. Thus, the reference voltage V_{ref} is given by

$$V_{ref} = V_{BE} + (r_1/r_a) \ln N \cdot V_t. \tag{1}$$

V_{ref} with a low temperature coefficient can be easily obtained by optimizing temperature-independent circuit parameters $r_1/r_2, N$.

The op-amp with an nMOS differential pair and pMOS followers includes an R–C compensation network for achieving a sufficient stability margin, which allows the input common-mode voltage to be as low as 0 V, thus simplifying the design of the startup circuit. The bias current may be derived from the bandgap reference itself. This provides a lower sensitivity to the supply voltage, leading to a higher supply rejection, but it also leads to a very small voltage gain in the undesired bias point. Furthermore, the input transistors should be designed with a large gate area and non-minimum gate length in order to keep the offset low. Indeed, the spread of the refer-

Table 2. Measurement results of the DC–DC converter.

| Symbol | Parameter | Condition | Min | Typ | Max |
|---------------|--|---|-----|-----|-----|
| V_{supply} | Supply voltage (V) | $T = +27\text{ }^\circ\text{C}$ | 5 | 9.5 | 14 |
| V_{out} | Output voltage (V) | $R_{load} = 3.85\text{ k}\Omega$ | 2.0 | | 2.5 |
| I_{out} | Supply current (μA) | $5.5\text{ V} < V_{in} < 7.5\text{ V}, R_{load} = 3.85\text{ k}\Omega$ | 560 | | |
| | | $7.5\text{ V} < V_{in} < 11.5\text{ V}, R_{load} = 3.85\text{ k}\Omega$ | 580 | | |
| | | $11.5\text{ V} < V_{in} < 14\text{ V}, R_{load} = 3.85\text{ k}\Omega$ | 660 | | |
| I_{CC} | Quiescent supply current (μA) | $I_{out} = 0\text{ mA}$ | 143 | | 240 |
| f_{osc} | Oscillator frequency (MHz) | | | 1 | 1.3 |
| μ_{trans} | Total power efficiency (%) | $T = +27\text{ }^\circ\text{C}$ | 49 | | 61 |
| μ_{power} | Total power efficiency (%) | $T = +27\text{ }^\circ\text{C}$ | 28 | | 42 |
| V_{pp} | Output voltage ripple (mV _{pp}) | $R_{load} = 4\text{ k}\Omega$ | 460 | | |

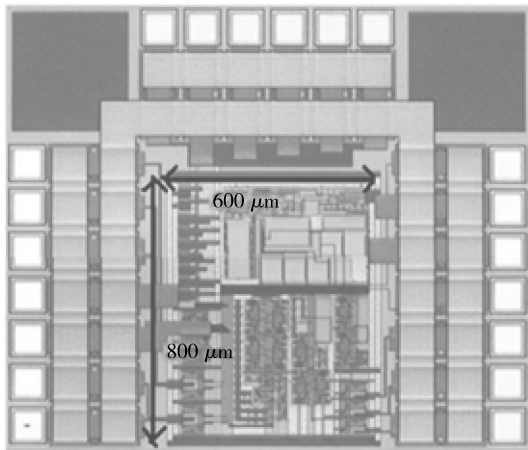


Fig. 6. Micrograph of the proposed DC–DC converter.

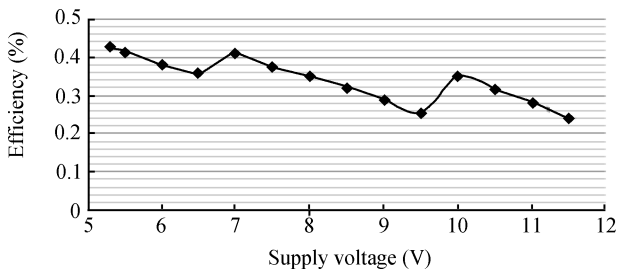


Fig. 7. Measured power converter efficiency variation with different input voltages.

ence voltages at wafer level is mainly contributed by the op-amp offset voltage.

4. Measurement results

The SC converter circuits have been taped out in the 0.35 μm CMOS process with EEPROM technology, provided by the Chartered Corporation. A micrograph of the proposed DC–DC converter is shown in Fig. 6. The size of the core circuit is $600 \times 800\text{ }\mu\text{m}^2$.

Figure 7 presents the measured power converter efficiency versus input voltage with the maximum load current. The measured curve shows that the converter efficiency decreases with input voltage before changing the step-down conversion ratio. When the input voltage just exceeds the threshold voltage, the step-down conversion ratio is set to be maxi-

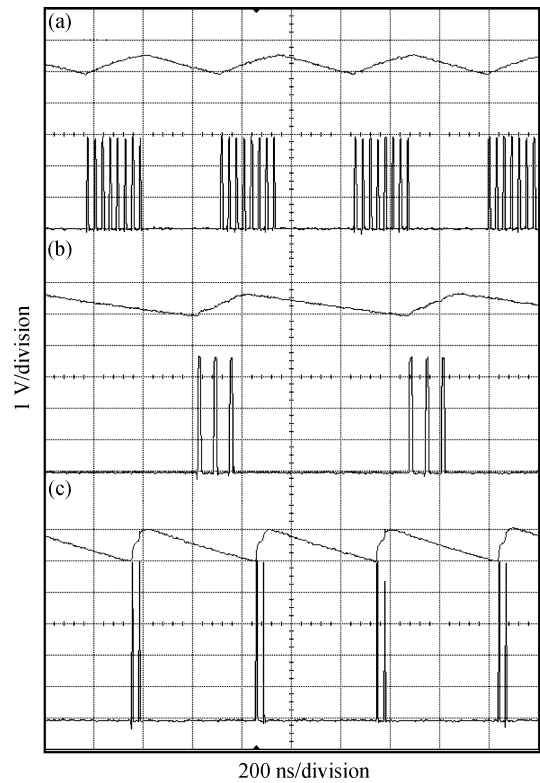


Fig. 8. Waveform of output voltage and stacked clock in different step-down conversion ratios: (a) $V_{DD} = 5.5\text{ V}$, ratio = 2/3; (b) $V_{DD} = 7\text{ V}$, ratio = 1/2; (c) $V_{DD} = 11\text{ V}$, ratio = 1/3.

mum 2/3. When the input voltage increases, the converter efficiency goes down, because system energy loss increases with supply voltage. When the input voltage reaches the settled value, the ratio turns to 1/2 and efficiency bounces up because its no-load output voltage is closer to the load voltage desired. This also happens when the ratio changes from 1/2 to 1/3. The maximum efficiency occurs when the input voltage is 5 V. Figure 8 shows the waveform of the output voltage and stacked clock in different step-down conversion ratios with the same load. The higher the input voltage is, the less time the converter works for in a period.

Table 2 presents the whole circuit’s performance. Measurement results show that the DC–DC converter can dynamically scale the charged capacitor supply from 5–15 to 2 V and supply at least 560 μA . The converter efficiency of the SC con-

verter can reach 61%, and the efficiency of the whole system ranges from 28% to 42%, which is much higher than 17.6% in Ref. [3] and 19% in Ref. [2].

5. Conclusions

A variable step-down conversion ratio switched capacitor DC–DC converter has been presented here to advance the converter efficiency of charge on the stored capacitor in a wireless monitoring system of orthopedic implants. The proposed converter works in intermittent mode to efficiently regulate from 15 V down to approximately 2 V. The SC topologies can be switched automatically to keep efficiency high over the entire supply voltage range. The stacked switches technique is also used to reduce leakage current in the switching process of the SC DC–DC converter. The total converter efficiency can reach 42% including all auxiliary components' power consumption, which is far higher than previous work. This DC–DC converter could be also used in other similar intermittent energy harvest-

ing systems.

References

- [1] Chen Hong, Jia Chen, Chen Yi, et al. A low-power IC design for the wireless monitoring system of the orthopedic implants. *IEEE Custom Integrated Circuits Conference*, 2008: 363
- [2] Kymissis J, Kendall C, Paradiso J, et al. Parasitic power harvesting in shoes. *Proc 2nd IEEE Int Conf Wearable Computing*, Los Alamitos, CA, August 1998: 132
- [3] Shenck N S, Paradiso J A. Energy scavenging with shoe-mounted piezoelectric. *IEEE Micro*, 2001, 21(3): 30
- [4] Makowski M S, Maksimovic D. Performance limits of Switched capacitor DC–DC converters. *26th Annual IEEE PESC'95 Record*, 1995: 1215
- [5] Jia Chen, Chen Hong, Liu Ming, et al. Integrated power management circuit for piezoelectronic generator in wireless monitoring system of orthopaedic implants. *IET Circuit, Device and System*, 2008, 12(6): 485