Improvements on high voltage performance of power static induction transistors*

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Abstract: A novel structure for designing and fabricating a power static induction transistor (SIT) with excellent high breakdown voltage performance is presented. The active region of the device is designed to be surrounded by a deep trench to cut off the various probable parasitical effects that may degrade the device performance, and to avoid the parallel-current effect in particular. Three ring-shape junctions (RSJ) are arranged around the gate junction to reduce the electric field intensity. It is important to achieve maximum gate–source breakdown voltage BV_{GS}, gate–drain breakdown voltage BV_{GD} and blocking voltage for high power application. A number of technological methods to increase BV_{GD} and BV_{GS} are presented. The BV_{GS} of the power SIT has been increased to 110 V from a previous value of 50–60 V, and the performance of the power SIT has been greatly improved. The optimal distance between two adjacent ring-shape junctions and the trench depth for the maximum BV_{GS} of the structure are also presented.

Key words: static induction transistor; parasitic effect; breakdown voltage; deep trench

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1. Introduction

Static induction transistors (SIT) have been widely used in electronic equipment for power application. SIT have many special advantages such as high frequency, high power and low power consumption. In recent years, a great deal of research work on SIT has been done for high frequency and high power application[1−10]. As a high power device, an SIT must withstand high voltage with a very small leakage current in the reverse blocking state, and can conduct large current with a small voltage drop in the forward conducting state. The high current performances of power SIT and their technological improvement methods have been investigated in depth in our previous paper[4]. The gate–source breakdown voltage BV_{GS} and gate–drain breakdown voltage BV_{GD} are the main limiting factors of SIT in the high power application region. In order to improve the high voltage capability, the active region of the SIT is designed to be surrounded by three ring-shape junctions (RSJ) to reduce the electric field concentration resulting from the curvature of junction planes and a ring-shape deep trench to cut off any probable parasitical effects that may degrade the device performance, and to avoid the parallel-current effect in particular, thereby increasing breakdown voltage effectively in this paper. The optimum distance between two adjacent ring junctions, the depth of junction and the voltage drop across two adjacent ring junctions are presented for high voltage performance of the SIT. In addition, the effects of RSJ and a deep trench on the high voltage performance of SIT are analyzed and discussed in depth. The simulated results agree very well with the experimental values. The designed structures are promising and offer the prospect of improving the high voltage performance of SIT in the high power application region.

2. Device structure and design consideration

In order to increase the current capability, SITs are usually designed to be composed of many units in parallel. Their channels and gate stripes are alternately arranged on the same plane, making it convenient to accomplish the paralleling of many units as shown in Fig. 1. The gate stripes are connected by a gate body alleyway. There are various probable parasitical effects in SIT that may deteriorate their electrical performance, such as an increase in leakage current in the blocking state and abnormal *I*–*V* characteristics. In an SIT, a parasitical npn bipolar transistor is composed of the epitaxial layer (n), gate body alleyway (p) and drift region (n), which is biased in the reverse amplifying region in the blocking state. The effect

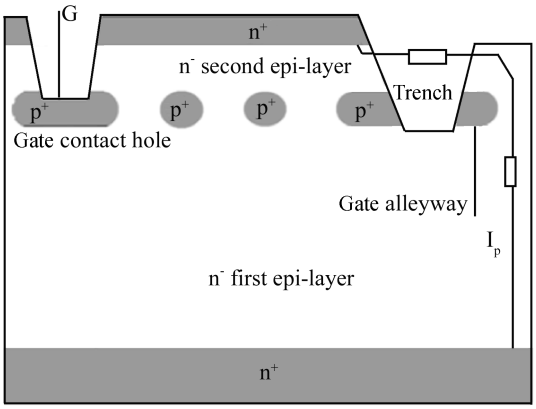

Fig. 1. Cross-section of a unit in SIT.

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of the parasitic npn bipolar transistor on the electrical performance can be neglected because of the long length of the base region and low current gain. When the SIT is biased in the forward conducting state, a number of electrons injected from the source region drift towards the drain mainly through the channel where the height of the potential barrier is modulated by the gate voltage. However, some of the injected electrons may flow transversely along the epitaxial layer and detour the gate body alleyway entering the drifting region outside the active region to reach the drain, forming a parasitic current I_P that cannot be controlled by the gate, and may degrade the SIT's electrical performance. In order to eliminate the performance deterioration resulting from the parasitical effect, it is necessary to cut off the electrical connection between the active and passive regions. Therefore, the device is designed such that the active region is surrounded by a deep trench with a width of 200 μm and a depth of 60 μm. On the other hand, the marginal positive angular profile of the pn junction between the epitaxial layer and the gate body alleyway at the margin of the chip formed by etching a deep trench is beneficial to the improvement of BV_{GS} and blocking voltage V_{block}.

3. Influence of parasitical effects on electrical performance

The electric field distribution at the junction plane of the epitaxial layer-gate pn junction can be controlled by a marginal positive angular profile formed by etching the deep trench, and therefore increasing BV_{GS} and V_{block}. The electrical performance of the SIT is sensitively dependent on the depth of the trench.

3.1. Effects of a shallow trench

The positive angular profile of the pn junction between the epitaxial layer and the gate body alleyway formed by etching a shallow trench has the following characteristics:

(1) When the oblique angle decreases, the width of the space charge region of the pn junction at the surface is increased and the electric field distribution is entirely reduced.

(2) The maximum electric field intensity at the surface then falls continuously, and the position of the peak electric field intensity shifts towards the region doped with lighter impurity concentration.

(3) When the positive oblique angle is reduced to 45°, the magnitude of the electric field intensity at the surface is 1/2 of its bulk value. The maximum electric field intensity appears at the planar plane of the pn junction.

(4) As the space charge region is widened along the profile surface by the positive oblique angle, the electric field intensity at the surface is greatly reduced, so the requirement of high voltage can be satisfied.

3.2. Effect of a deep trench

Although a shallow trench with a small depth can be easily etched, the trench depth accuracy must be accurately controlled within ±1 μm, resulting in significant technological difficulties. Furthermore, since the shallow trench cannot cut off the gate body alleyway at the cutting boundary of the SITH, the pn junction formed by the gate body alleyway and substrate in the blocking state extends towards the scribing boundary at the chip margin where there are a number of imperfections. Breakdown phenomena may occur firstly in the vicinity of the cutting boundary due to electric field concentration, decreasing the blocking voltage.

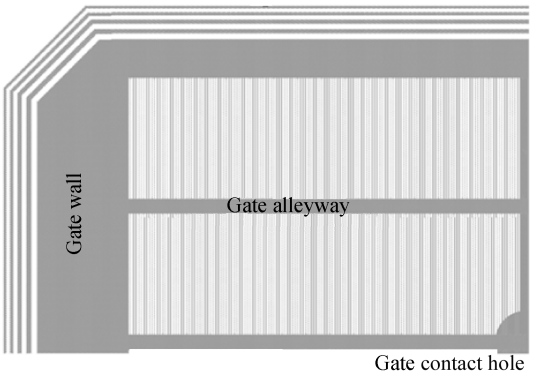

Fig. 2. Schematic top view of a portion in an SIT.

Taking comprehensive account of these factors, a deep trench surrounding the active region of the SIT was etched to optimize the electrical performance, and to increase BV_{GS}. A positive angular profile for the pn junction between the epitaxial layer and the gate body alleyway formed by deep trench etching can decrease surface electric field, satisfying the high voltage resistance requirement of the SIT, and the formation of a negative angular profile for the pn junction between the gate body alleyway and substrate can not only reduce the surface electric field, but can also effectively prevent bulk breakdown occurring. Furthermore, a deep trench can isolate the active region from the scribing boundary to avoid any probable influences of various defects on device performance. A schematic view of the trench mask is shown in Fig. 2.

4. Gate–drain breakdown voltage BV_{GD}

4.1. Influence of thickness of drift region epitaxial layer

With the increase in thickness of the drift region epitaxial layer, the BV_{GD} of the SIT is much improved due to the increase in gate–drain distance (l_{DG}) as shown in Fig. 3. But the thickness of the epitaxial layer of the drift region is constrained by many other factors. For example, in order for the SIT to have triode-like I–V characteristics, the depletion layer of the gate junction must reach the drain terminal before the drain voltage V_D approaches the power source voltage V_B. The optimum thickness l_{GD} of the drift region epitaxial layer for acquiring high BV_{GD} can be empirically expressed as:

$$l_{GD} = 1.25 \times \left[\frac{2\varepsilon_0 \varepsilon_S \left(V_{bi} + V_B/2\right)}{eN_{Drift}} \right]^{1/2}, \qquad (1)$$

where V_{bi} is the built-in potential, V_B is the power source voltage and N_{Drift} is the doping concentration of the drift region. The thickness of the drift region epitaxial layer l_{GD} must

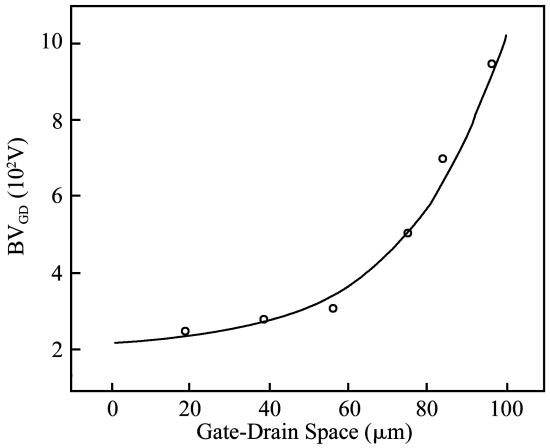

Fig. 3. Dependence of BV_{GD} on gate–drain space.

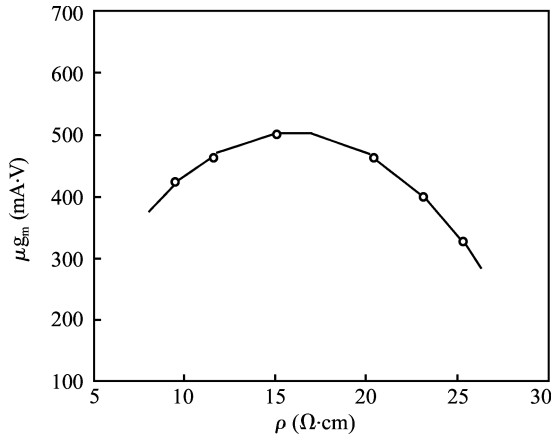

Fig. 4. Dependence of BV_{GD} on resistivity of first epitaxial layer.

be designed to satisfy the requirement that the BV_{DG} must be more than twice as high as the power source voltage V_B ($BV_{GD} > 2V_B$).

4.2. Dependence of BV_{GD} on resistivity of drift region epitaxial layer

As the SIT is a triode-like enhancement mode device, the gate depletion layer should extend to the drain terminal. Since punch-through breakdown occurs before avalanche, the actual value of breakdown voltage is lower than the theoretical one. Although the increase in resistivity ρ_d of the drift region epitaxial layer can improve BV_{GD}, it is also limited by other parameters. The dependence of figure of merit, defined as the product (μg_m) of voltage amplification μ and transconductance g_m for describing the electrical performance of an SIT, on the resistivity of the epitaxial layer is shown in Fig. 4. The experimental result shows that the resistivity of the epitaxial layer must be chosen in accordance with the gate-to-gate space. The optimum resistivities of the epitaxial layer for acquiring excellent electrical performance are 6–10, 15–18 and 16–24 Ω·cm corresponding to gate-to-gate spaces of 8 μm, 10 Ω·cm and 15 Ω·cm, respectively.

4.3. Influence of geometrical dimension on BV_{GD}

The decrease in channel thickness (d_c) can reduce the pinch-off voltage V_P, increase voltage gain μ and BV_{GD}. A small voltage is required for the whole thickness of the channel to be occupied by the depletion layer of the gate-channel p^+n^- junction. In the critical pinching off point, the dependence of pinch-off voltage V_P on channel thickness (d_c) can be written as:

$$d_c = 2\sqrt{\frac{2\varepsilon_0\varepsilon(\phi_S + V_P)}{eN_d}}, \tag{2}$$

where ϕ_S is the built-in potential, and N_d is the doping concentration of the channel. When the channel thickness decreases, a small voltage V_p is needed to pinch off the channel. The voltage gain describing the controlling capability of the drain voltage to the potential barrier in the channel related to the gate voltage can be defined as[4]:

$$\mu = \exp\left(\pi\frac{l_c}{d_c}\right), \tag{3}$$

where l_c is the length of the channel. When the channel thickness decreases, the voltage gain μ increases exponentially. Modulating the thickness of the channel to increase BV_{GD} is a feasible technical approach. The dependence of BV_{GD} on pinch-off voltage V_P and voltage gain. μ is shown in Fig. 5, respectively.

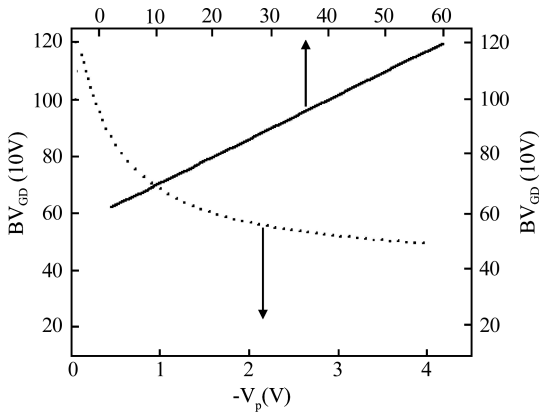

Fig. 5. Influence of pinch-off voltage on BV_{GD} (dotted line) and on voltage gain μ (solid line).

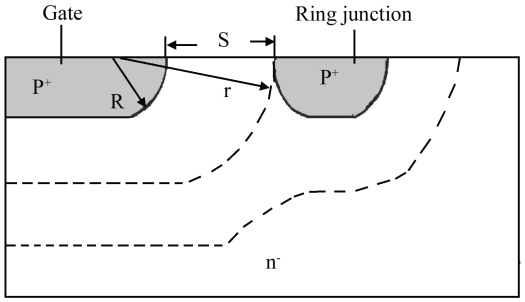

Fig. 6. Cross-section of a main junction and an RSJ junction.

4.4. Application of ring-shape junction

The BV_{GD} are much improved by appropriately increasing the diffusion depth of the gate body and applying three ring-shape junctions surrounding the gate junction. The cross-section of a p^+–n planar junction of the SIT with an RSJ structure is shown in Fig. 6. The maximum electric field at the outer

profile of the junction can be expressed as:

$$E_{\max} = \frac{eN_{\rm d}}{2\varepsilon_0\varepsilon_{\rm S}}\left(\frac{r^2}{R} - R\right), \tag{4}$$

where $N_{\rm d}$ is the donor doping concentration of the epitaxial layer. The voltage drop across two adjacent rings can be approximately written as:

$$\delta V = 8 \times \frac{N_{\rm d}}{10^{16}} \times \left\{(s+R)^2\left[\ln\left(1+\frac{s}{R}\right) - \frac{1}{2}\right] + \frac{R^2}{2}\right\}. \tag{5}$$

The optimum space between adjacent rings $d_{\rm i}$ for acquiring high breakdown voltage is expressed as:

$$S \approx \left(R^2 + \frac{5.0\times10^{14}}{N_{\rm d}^{7/8}}R\right)^{1/2} - R. \tag{6}$$

The space between two adjacent ring-shape junctions is determined by the radius of curvature, doping concentration and the semiconductor material parameters. Although the increase in space between adjacent ring junctions can enhance the voltage division effect of the ring junction, the electric field at the junction plane should not be higher than the breakdown field determined by the semiconductor material. Different ring spaces and curvature radii are required for different device specifications used in application regions. In experiment, in order to achieve the desired breakdown voltage $\rm BV_{GD}$ = 1200 V, for $N_{\rm d} = 3\times10^{13}$ cm^{-3} the calculated junction plane radius of curvature is 6.8 μm, and the ring spaces between three ring-shape junctions are 35.6, 27.8 and 15.5 μm, respectively. The experimentally measured average value is 1138 V.

5. Gate–source breakdown voltage $\rm BV_{GS}$

As a power switching device, the maximum operating voltage of an SIT is determined by its forward blocking capability. The increase in blocking capability of the SIT results from the high potential barrier in the channel, formed by negatively biased gate–source voltage, high enough to block the large current produced by a high drain positive voltage.

In order to increase the dynamical operation region, and improve the blocking capability of the SIT, it is necessary to increase $\rm BV_{GS}$. $\rm BV_{GS}$ must reach a value of 70–110 V for an SIT with 1 kW power dissipation. Technological and structural measures must be taken to improve gate–source breakdown performance. To improve $\rm BV_{GS}$, the following technological approaches are presented according to the experimental results:

(1) To increase the thickness of the second epitaxial layer (22 μm) and appropriately controlling its doping concentration for an SIT with buried gate structure.

(2) To decrease doping concentration in the channel and increase the sheet resistance of the gate region ($R_\square$ = 45 Ω/□).

(3) To increase the sheet resistance of the channel region (1000–4000 Ω/□).

(4) To increase the boron diffusion depth of the gate body (8 μm).

(5) To absorb boron atoms by wet oxidation.

(6) To remove BSG and PSG.

(7) To increase the space between gate and source regions as much as possible.

(8) To adopt local oxidation and self-aligned technology.

6. Results and conclusions

The various probable parasitical effects existing in an SIT such as a parasitical npn bipolar transistor and irregular parasitical parallel current effects in the boundary region that cannot be controlled by gate voltage may deteriorate the electrical performance of the SIT, even resulting in high leakage current in the blocking state and abnormal I–V characteristics. A deep trench designed around the active region of the SIT can not only effectively cut off parasitical current, but can also significantly improve gate–source and gate–drain breakdown voltages by the marginal profile of the pn junction between the gate alleyway and epitaxial layer. In order to cut off the parasitical effects adequately, the trench depth must be slightly larger than the sum of the gate diffusion depth and the thickness of the second epitaxial layer. In other words, the deep trench must penetrate through the gate wall at the marginal region. The experimental results and theoretical analysis demonstrate that a deep trench is more effective than a shallow one for improving high voltage performance due to the positive angular profile formed.

The $\rm BV_{GD}$ of a power SIT is sensitively dependent on the resistivity, the thickness of the drift region epitaxial layer and the geometrical dimensions of the channel. There is an optimum resistivity of the epitaxial layer of 15 Ω·cm for a channel length of 10 μm for acquiring excellent high voltage performance of the power SIT. The increase in thickness of the drift region epitaxial layer can also improve the $\rm BV_{GD}$ of the SIT due to the increase in gate–drain distance. The decrease in channel thickness can obviously improve high voltage performance by reducing the pinch-off voltage $V_{\rm P}$ and increasing the voltage gain μ.

The use of ring-shape junctions surrounding the gate body of the SIT is an efficient approach to increase breakdown voltage and blocking capability. It can diminish electric field concentration resulting from the curvature effect on junction surfaces.

$\rm BV_{GS}$ can be increased by a number of technical measures. The equality and doping concentration of the second epitaxial layer are critical factors in improving $\rm BV_{GS}$. In order to achieve $\rm BV_{GS}$ = 120 V, the sheet resistance of the channel region must be chosen within 1000–4000 Ω/□.

By taking a number of designing and technological measures presented in this paper, a power SIT, with $\rm BV_{GS}$ = 120 V, $\rm BV_{GD}$ = 1200 V and correct I–V characteristics, has been successfully fabricated. The structure and technological methods are promising and offer the prospect of fabricating a power SIT with high voltage capability.

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