A low power high gain UWB LNA in 0.18-μm CMOS*

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Abstract: A low power high gain differential UWB low noise amplifier (LNA) operating at 3–5 GHz is presented. A common gate input stage is used for wideband input matching; capacitor cross coupling (CCC) and current reuse techniques are combined to achieve high gain under low power consumption. The prototypes fabricated in 0.18-μm CMOS achieve a peak power gain of 17.5 dB with a –3 dB bandwidth of 2.8–5 GHz, a measured minimum noise figure (NF) of 3.35 dB and –12.6 dBm input-referred compression point at 5 GHz, while drawing 4.4 mA from a 1.8 V supply. The peak power gain is 14 dB under a 4.5 mW power consumption (3 mA from a 1.5 V supply). The proposed differential LNA occupies an area of 1.01 mm^2 including test pads.

Key words: UWB; LNA; high gain; low power
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1. Introduction

UWB is a new wireless technology which is able to transmit data over short distances with high data rates and low power consumption. The Federal Communication Committee (FCC) has set aside the 3.1–10.6 GHz band for commercial use since 2002[1]. This whole band can be divided into two sub-bands, 3.1–5 GHz for the lower band and 6–10.6 GHz for the upper band. It is the lower band that is used in our UWB system.

Design of a broadband low noise amplifier (LNA) across 3.1–5 GHz is critical for the UWB receiver, as it should achieve high gain, low return loss and a low noise figure over the 2 GHz bandwidth, while keeping a strict limit on power consumption and die area. Many structures of UWB LNA have been fabricated in CMOS technology, such as an inductively degenerated common source amplifier with a multi-section LC band-pass filter for input wideband matching[1] and resistive feedback[2] structures. As a wideband input match can be easily obtained by setting the transconductance of the common gate topology[3] without extra passive components, it is also popular for realizing a wideband LNA.

This paper presents a novel differential common gate UWB LNA with CCC and current reuse techniques to reduce the noise figure and improve the power gain.

2. Circuit design and analysis

Figure 1 shows the proposed CMOS UWB LNA circuit utilizing the CCC[3] and current reuse techniques. It is proved in Ref. [3] that the CCC technique is able to reduce the noise figure and power consumption and improve the effective transconductance of the conventional common-gate LNA, while maintaining wideband input matching. But the gain and bandwidth of the CCC LNA in Ref. [3] cannot meet the gain and bandwidth specifications of the UWB LNA without extra bandwidth extension techniques. In the proposed LNA, L1,2 is used as the shunt peaking load of the input stage; it is also used to conduct DC current and block RF signal to implement the current reuse technique for the second cascode stage (M3,4 & M5,6) with shunt peaking[4]. Therefore a larger gain and wider bandwidth can be achieved without increasing the DC current of the LNA. M7,8 is a source follow buffer only for measurement purposes, and will not be presented when applied in the UWB receiver.

2.1. Noise figure

The NF of a multi-stage structure is dominated by the first stage. In the proposed UWB LNA, the NF is dominated

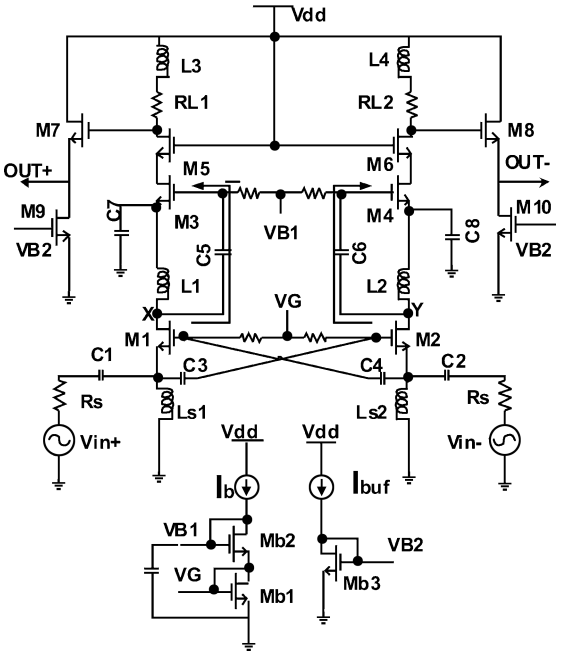

Fig. 1. Proposed UWB LNA topology.

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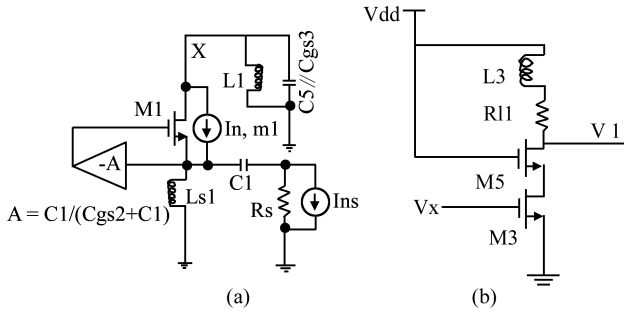

Fig. 2. (a) Equivalent circuit of the first stage; (b) Equivalent circuit of the second stage.

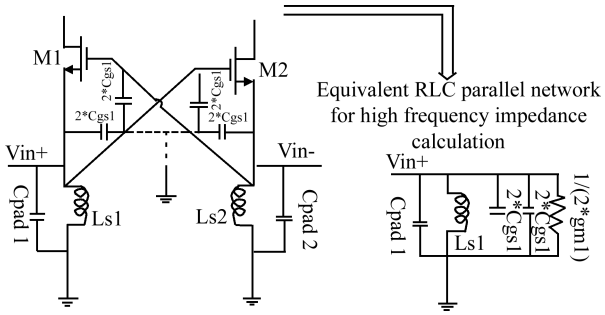

Fig. 3. Input network and its equivalent circuit.

by the common gate input stage [Fig. 2(a)]. As gate induced noise is always negligibly small in a common gate LNA[3], the NF of this circuit is dominated by channel current noise $i_{\mathrm{n,\,m1}}$. The calculated NF is[5]:

$$F = 1 + \frac{\overline{i_{\mathrm{nd}}^2}\{1/[1+(1+A)g_{\mathrm{m1}}R_{\mathrm{s}}]\}^2}{\overline{i_{\mathrm{ns}}^2}\{(1+A)g_{\mathrm{m1}}R_{\mathrm{s}}/[1+(1+A)g_{\mathrm{m1}}R_{\mathrm{s}}]\}^2}$$

$$= 1 + \frac{\overline{i_{\mathrm{nd}}^2}}{\overline{i_{\mathrm{ns}}^2}}[1/(1+A)g_{\mathrm{m1}}R_{\mathrm{s}}]^2, \tag{1}$$

where

$$\overline{i_{\mathrm{nd}}^2} = 4kT\gamma g_{\mathrm{d0}}\Delta f,\ \overline{i_{\mathrm{ns}}^2} = 4kTR_{\mathrm{s}}^{-1}\Delta f,\ \alpha = g_{\mathrm{m1}}/g_{\mathrm{d0}},$$

$$A = \frac{1/C_{\mathrm{gs}}s}{1/C_{\mathrm{gs}}s + 1/C_1 s} = \frac{C_1}{C_1 + C_{\mathrm{gs}}} \approx 1(C_1 \gg C_{\mathrm{gs}}).$$

Equation (1) can be reduced to:

$$F = 1 + \frac{4kT\gamma g_{\mathrm{d0}}\Delta f}{4kTR_{\mathrm{s}}^{-1}\Delta f}\left(\frac{1}{2g_{\mathrm{m1}}R_{\mathrm{s}}}\right)^2 = 1 + \frac{\gamma}{4\alpha g_{\mathrm{m1}}R_{\mathrm{s}}}. \tag{2}$$

Under perfect matching, the input impedance of the first stage is:

$$Z_{\mathrm{in}} \approx 1/(1+A)g_{\mathrm{m1}} \approx 1/2g_{\mathrm{m1}} = R_{\mathrm{s}}.$$

It can be further reduced to[5]:

$$F = 1 + \frac{\gamma}{2\alpha}. \tag{3}$$

This indicates that the CCC common gate LNA can achieve a better noise performance compared with a conventional common gate LNA ($F = 1 + \frac{\gamma}{\alpha}$[4]), while the current to achieve the same input matching is reduced. For $\gamma/\alpha = 2$, the calculated NF is about 3 dB.

2.2. Wideband and high gain

In a one stage amplifier with shunt peaking is difficult to get 3 dB bandwidth over 2 GHz with high gain; therefore, two stages are cascaded to improve gain and bandwidth. In the proposed topology, the current of the common gate input stage is reused for the following cascode amplifier through the inductor L1,2. The large inductor L1,2 (8 nH in this design) shows high impedance for a high frequency signal, so the signal is blocked from the dc path from M1 to M3 and then is amplified by the subsequent cascode stage shown in Fig. 2(b). In addition, L1,2 is the load of M1,2 to extend the bandwidth of the first stage. It is designed to resonate at the lower frequency limit of 3.1–5 GHz. The second stage also employs the shunt peaking technique (L3,4) [Fig. 2(b)]; resistors $Rl_{1,2}$ are used to lower the quality factor of L3,4 to further extend the bandwidth and maintain gain flatness. Proper design of L3,4 makes the gain of the second stage peak at a frequency near 6 GHz, leaving a little design margin over bandwidth.

2.3. Wideband input matching

The input network and its equivalent RLC network are shown in Fig. 3.

$$Z_{\mathrm{in}}(s) = L_{\mathrm{s1}}s//\frac{1}{2g_{\mathrm{m1}}}//\frac{1}{(2c_{\mathrm{gs1}} + 2c_{\mathrm{gs2}} + c_{\mathrm{pad1}})s}$$

$$= \frac{1}{1/(L_{\mathrm{s1}}s) + (4c_{\mathrm{gs1}} + c_{\mathrm{pad1}})s + 2g_{\mathrm{m1}}}. \tag{4}$$

The resonant frequency ω_o is set at 4 GHz, which is the center of the 3–5 GHz band, $Z_{\mathrm{in}}(\mathrm{j}\omega_{\mathrm{o}}) = \frac{1}{2g_{\mathrm{m1}}} = 50\ \Omega$. In addition, the quality factor of the RLC parallel network can be expressed as[3]:

$$Q_{\mathrm{in}} = \omega_{\mathrm{o}}\frac{1}{2g_{\mathrm{m1}}}(c_{\mathrm{pad1}} + 4c_{\mathrm{gs1}}) < 1. \tag{5}$$

The low quality factor of the input shunt resonant tank indicates that it is applicable for wideband input matching. The above equations are enough to determine input transistor size and inductance for a first order approximation; accurate calculation should take the inductor's parasitic resistor and capacitance into account.

2.4. Low power design

The proposed circuit exploits the capacitor cross coupling and current reuse techniques to save power consumption. Capacitor cross coupling boosts the effective transconductance of the input stage, and therefore it is able to use less current to obtain the same gain. The current reuse technique, which is implemented by inductor L1 and AC coupling capacitance C5, makes the power consumption even less for the required power gain and bandwidth.

2.5. Inductor design and optimization

From the above analysis, the inductors are the key components to obtain high gain, ultra-wideband and power reduction, so they should be designed with special attention and

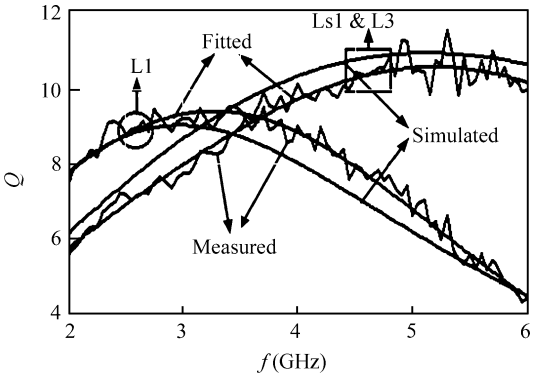

Fig. 4. Quality factor of the inductors.

modeled exactly. Moreover, performances such as gain or die area will be improved by optimizing the geometric parameters of the inductors[6].

At 4 GHz, the skin depth δ for our technology is 1.3 μm, so a narrow track width is feasible at high frequencies. In the proposed circuit, a track width of 4 μm is used to tune the peak quality factor of inductors at the frequency in the 3–5 GHz frequency range; the minimum spacing between tracks has been set to maximize the quality of the inductors; a narrow track width will also help to save die area and reduce substrate coupling through inductors. In the proposed circuit, L1 is designed to have a peak quality factor near 3 GHz, and L3 is designed to have a peak quality factor near 5 GHz. Ls1 has the same size as L3. All the inductors used in this circuit are fabricated with their corresponding test structures, and the simulated and measured results are presented in Section 3.

2.6. ESD protection considerations for the LNA

In a CG LNA, the ESD problem is less sensitive since the RF input is connected to the source of the transistor where a parasitic diode exists (consisting of the n+ region of the M1 source and the p- region of the substrate) to carry the charges for a negative pulse to ground[7]. In addition, the inductor at the source which is used to tune out parasitic capacitance plays another important role for ESD protection as it provides a bidirectional path for ESD current to ground[7]. This kind of inductive ESD protection is especially effective in high frequency applications, as the inductor provides a low impedance path to ground for the ESD pulse ($f_{\rm ESD} < 1$ GHz)[8] but a high impedance for the RF signal ($f_{\rm o}$ = 3–5 GHz). It should be noted that it is implemented without additional components and therefore without degrading the circuit performance, compared with capacitive ESD protection.

3. Measurement results

All the inductors used in the proposed circuit are fabricated with open-short de-embedding structures. Figure 4 shows the simulated, measured and fitted quality factor of the inductors.

The proposed circuit has been fabricated in SMIC 0.18-μm CMOS technology. Photographs of the circuit and inductors are shown in Fig. 5. The die area of the LNA is 840 $\times$ 900 μm^2 excluding test pads.

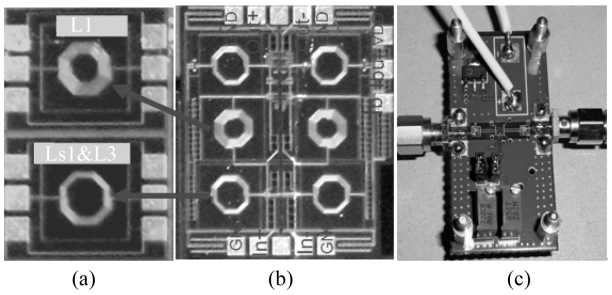

Fig. 5. Photographs of (a) inductors, (b) chip, and (c) PCB.

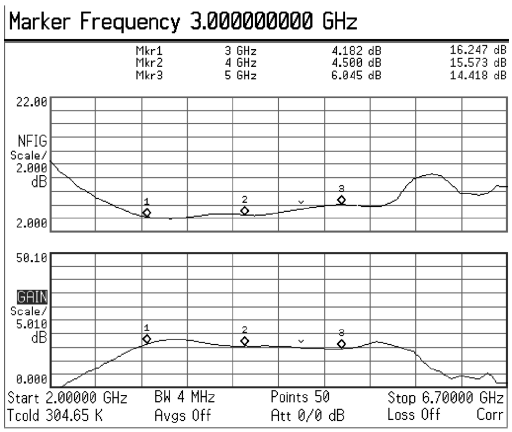

Fig. 6. Measured gain and NF of the LNA.

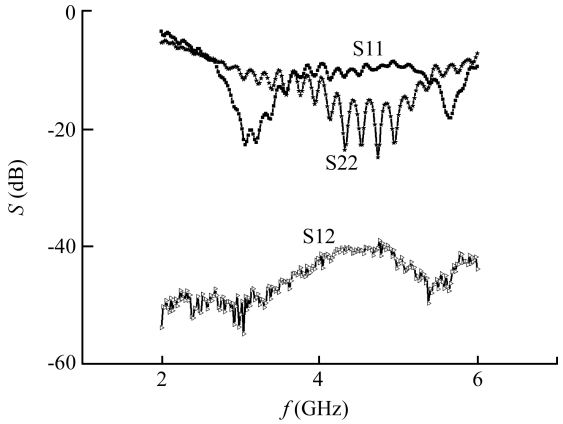

Fig. 7. Measured S parameters.

The proposed chip is mounted on an FR-4 PCB test board (COB) for measurements. The differential input and output signals are converted into a single-ended signal by a passive balun (BD3150N50100A00) with 0.6 B insertion loss. The measured current is 4.4 mA for the differential cores under a 1.8 V supply. An Agilent 8975A noise figure analyzer is used to measure the gain and NF of the differential LNA. Figure 6 shows the measured gain and NF of the LNA. The maximum measured power gain is 17.5 dB at 3.5 GHz. The power gain is 14.4–17.5 dB from 2.8 to 5.4 GHz. The measured NF is 3.95–6.0 dB from 3 to 5.4 GHz. It should be noted that the gain is measured without de-embedding 1.2 dB loss from baluns and 6 dB loss from the output buffer. The NF is 3.35 to 5.4 from 3 to 5.4 GHz as 0.6 dB loss from the input balun should be subtracted from the measured NF[9].

Table 1. Comparisons of the proposed wideband LNA with previously published work.

Reference	Gain (dB)	Power (mW)[c)]	BW_{3dB} (GHz)	S_{11} (dB)	NF (dB)[d)]	iCP (dBm)	Area (mm^2)[e)]	Technology
Ref. [1]	10.4[a)]	9	2.3–9.2	< −9.4	4.2	–18 @ 6 GHz	1.1	0.18 μm CMOS
Ref. [2]	9.8[a)]	12.6	2–4.6	< −9	2.3[g)]	NA	0.9	0.18 μm CMOS
Ref. [10]	9.7[a)]	20	1.2–11.9	< −10	4.5	–16 @ 6 GHz	0.59	0.18 μm CMOS
Ref. [11]	9.5[a)]	16.5[f)]	2–4.6	< −10	3.5	–6 @ 3.1 GHz	1.08	0.13 μm CMOS
Ref. [12]	16	38[f)]	5.9	< −9	4.7	–24	0.24	0.13 μm CMOS
This work	17.5[b)]	7.9[f)]	2.8–5	< −8.5	3.35	–12.6 @ 5 GHz	1.01	0.18 μm CMOS
This work	14[b)]	4.5[f)]	2.8–5	< −10	3.6	NA	1.01	0.18 μm CMOS

[a)] Maximum gain, approximately 6 dB loss due to output buffer; [b)] Maximum gain, approximately 6 dB loss from output buffer and 1.2 dB loss from baluns; [c)] Excluding output buffer; [d)] Minimum NF in the pass band; [e)] Including test pads; [f)] Differential designs; [g)] With external inductor.

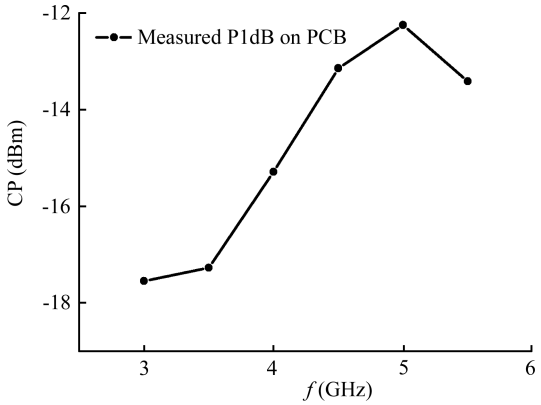

Fig. 8. Measured input 1 dB compression point.

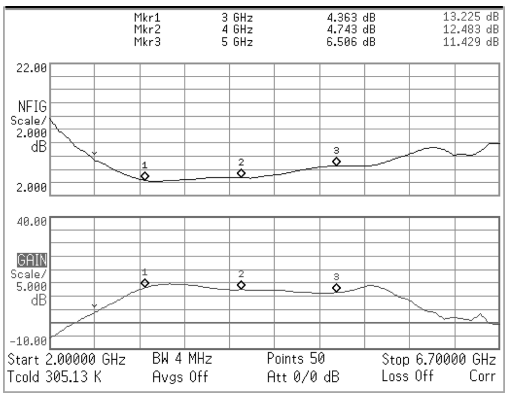

Fig. 9. Measured gain and NF under 4.5 mW power consumption.

An Agilent 8722ES vector network analyzer was used to measure the S parameters; the results are shown in Fig. 7. The measured S_{11} stays below –8.5 dB and S_{22} remains below –10 dB over 2.8–5.4 GHz. Reverse isolation S_{12} < –40 dB from 2 to 6 GHz, which indicates good stability performance.

Figure 8 shows the measured input-referred 1 dB compression point, which shows –12.6 dBm at 5 GHz.

The above-mentioned test results show that the circuit is able to obtain high gain (17.5 dB) under low power consumption (7.9 mW) due to its novel architecture. To further explore its potential for low power operation, the supply is reduced to 1.5 V, the bias current I_b is adjusted to set core current consumption to 3 mA, and the gain and NF are measured and shown in Fig. 9. The measured gain under 4.5 mW remains larger than 10 dB across 2.7–5.6 GHz. The NF is 3.6–6.0 dB (0.6 dB balun loss is subtracted) from 3–5 GHz. Measured S parameters are shown in Fig. 10.

Table 1 summarizes the measurement results and compares them with previously published work.

4. Conclusion

A low power and high gain differential UWB LNA for a 3.1–5 GHz UWB receiver has been designed in this paper. By utilizing the capacitor cross coupling and current-reuse techniques along with proper design of on-chip inductors, high gain (17.5 dB) and low NF (3.35 dB) can be achieved under extremely low power consumption (7.9 mW). COB measurement results show that the proposed LNA can operate at 4.5 mW to provide 14 dB power gain. Moreover, the proposed LNA has the potential to be well protected from ESD pulses although this has not been tested. Due to the narrow track width of the inductors, the proposed differential circuit occupies an area of 1.01 mm^2 including test pads.

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