# TaN wet etch for application in dual-metal-gate integration technology*

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**Abstract:** Wet-etch etchants and the TaN film method for dual-metal-gate integration are investigated. Both HF/HN$O_3$/$H_2O$ and $NH_4OH$/$H_2O_2$ solutions can etch TaN effectively, but poor selectivity to the gate dielectric for the HF/$HNO_3$/$H_2O$ solution due to HF being included in HF/$HNO_3$/$H_2O$, and the fact that TaN is difficult to etch in the $NH_4OH$/$H_2O_2$ solution at the first stage due to the thin $TaO_xN_y$ layer on the TaN surface, mean that they are difficult to individually apply to dual-metal-gate integration. A two-step wet etching strategy using the HF/$HNO_3$/$H_2O$ solution first and the $NH_4OH$/$H_2O_2$ solution later can fully remove thin TaN film with a photo-resist mask and has high selectivity to the HfSiON dielectric film underneath. High-*k* dielectric film surfaces are smooth after wet etching of the TaN metal gate and MOSCAPs show well-behaved *C*–*V* and $J_g$–$V_g$ characteristics, which all prove that the wet etching of TaN has little impact on electrical performance and can be applied to dual-metal-gate integration technology for removing the first TaN metal gate in the PMOS region.

**Key words:** TaN; wet etching; metal gate; high *k* dielectric; integration
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## 1. Introduction

According to the International Roadmap for Semiconductors[1], high dielectric constant (high-*k*) gate materials and dual-metal-gate electrodes with appropriate work functions are demanded to reduce the gate direct tunneling leakage current and to eliminate the poly-Si gate depletion effect, boron penetration effect and Fermi-level pinning when the device dimension is scaled down to the 45 nm node and beyond[2–4]. One of the simplest implementations of dual-metal-gate integration is the deposition–etch–deposition approach. As the name implies, first metal deposition, selective etching and second metal deposition steps are performed sequentially. A key factor in this dual-metal-gate process is the selective etching of the first metal gate without damage to the underlying gate dielectric before deposition of the second metal[5]. Therefore, wet etching is preferred to dry etching to reduce possible damage to the high-*k* dielectric from energetically charged particles[6]. TaN has been identified as a possible metal gate material candidate because of its thermal stability, excellent scalability, adjustable work function and compatibility with high-*k* dielectrics. However, the common acids and alkalis, such as HF, HCl, $HNO_3$, $H_3PO_4$, $H_2SO_4$, aqua-regia and $NH_4OH$, either could not etch TaN or the etch rates were below several Å/min[7]. TaN's chemical resistance makes the wet etch process difficult in the dual-metal-gate system. The development of a reliable wet etch module, therefore, is an integral part of the overall process integration.

In this article, we will introduce two types of TaN etchants and a two-step etching strategy for thin TaN film removal with a photo-resist (PR) mask, which can provide a potential solution for the selective etching of TaN and be integrated into the dual-metal-gate CMOS device process.

## 2. Experiment

A TaN metal gate was deposited through reactive sputtering of a Ta target in Ar/$N_2$ ambient. A preformed positive PR was used for the etching mask of the TaN/$SiO_2$/Si samples. Wet etching was performed using by the two kinds of wet etchants mentioned above under different composition and etching conditions. After etching, the samples were rinsed in de-ionized water and dried by $N_2$ flow. TaN etch rates were obtained from the step height measured with VEECO/Dektak 150 and the etching time. The chemical composition and bonding states of the sample surface were investigated by XPS measurements with a monochromatic AlK$\alpha$ (1486.6 eV) incident X-ray. The surface morphology and the cross section of the samples was investigated using AFM and SEM, respectively.

MOS capacitors with a TaN/HfSiON gate stack were also fabricated to investigate the electrical impacts of TaN metal gate wet etching on the underlying high-*k* dielectrics. After a standard cleaning process, the HfSiON (30 Å) film was deposited onto the $SiO_2$ interface layer by co-sputtering of Hf and Si targets in an Ar/$N_2$ ambience. The HfSiON film after annealing by RTA at 700–900 °C was exposed to the $NH_4OH$/$H_2O_2$ solution before the TaN metal gate was deposited. For comparison, a control TaN/HfSiON capacitor without wet chemical exposure was also fabricated. Finally, all samples were metallized with Al(Si) on the backside at 420 °C in an $N_2$ ambience. The high frequency (1 MHz) capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) were measured by

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Table 1. Etch rates of TaN, $SiO_2$ HfSiON and TEOS by two etchants under our optimum conditions.

| Etch solution | Temperature (°C) | TaN (Å/min) | $SiO_2$ (Å/min) | HfSiON (Å/min) | TEOS (Å/min) |
|---|---|---|---|---|---|
| $NH_4OH/H_2O_2$ | 70 | 123 | 1.18 | 1.09 | 3.04 |
| $HF/HNO_3/H_2O$ | 22 | 58 | 545 | — | 1715 |

an MDC *C*–*V* analyzer and a Keithley 4200 semiconductor parameter analyzer, respectively.

## 3. Results and discussions

### 3.1. Wet-etch etchants for TaN

TaN was not attacked by any of the common acids and alkalis, but we found that two etchants had a high enough etch rate to satisfy the demand of the etching of TaN film: one was a mixture of $HNO_3$ and HF in de-ionized water, and the other was a solution mixed with $NH_4OH$ and $H_2O_2$. De-ionized water is used to dilute all the solutions; the more concentrated the solution, the faster the reaction rate. In addition, a higher temperature will also increase the reaction rate of the solutions to TaN. The etchants both work by continually oxidizing and then etching the surface of the TaN, and dissolving the metals into solution.

Etch rates of TaN, HfSiON, $SiO_2$ dielectric and TEOS hardmask by two etchants under our optimum conditions are shown in Table 1. The $HF/HNO_3/H_2O$ solution with the optimum ratio at room temperature could etch TaN with an average etch rate of 58 Å/min without damaging the PR in 8 min. However, because HF was contained in this wet etchant, which etched $SiO_2$ or HfSiON gate dielectrics and TEOS hardmask very quickly, it was not a suitable wet-etch etchant in terms of integration. In comparison to the $HF/HNO_3/H_2O$ solution, the $NH_4OH/H_2O_2$ etchant with an optimum ratio at 70 °C not only had a high TaN etch rate (123 Å/min) but also had high selectivity to HfSiON (113 : 1), $SiO_2$ (104 : 1) and TEOS (41 : 1). In addition, the $NH_4OH/H_2O_2$ etchant could be used with a PR mask for short etch times (< 3 min), and TEOS could be used as a hardmask for longer etch times. Because of the fast etch rate, high selectivity to gate dielectric and appropriate mask materials, the $NH_4OH/H_2O_2$ etchant is a better choice for dual-metal-gate integration.

### 3.2. Effect of TaN surface oxidation

In the etching experiments of the patterned TaN in the $NH_4OH/H_2O_2$ solution, we found that TaN samples could almost not be etched within 1 min. To find the reason for the difficulty at the beginning of the etching for TaN, chemical analyses of the TaN layers were performed by XPS. Figure 1 shows the XPS spectra of the blanket TaN surface which was only exposed to ambient air in the course of transport prior to being used for the etching experiments. $Ta4f_{7/2}$ and $Ta4f_{5/2}$ peaks were observed at binding energies of 26.0 eV and 28.0 eV in Fig. 1(a), which was believed to originate from Ta–O bonding because the binding energies for $Ta_2O_5$ are 26.32 eV [$Ta4f_{7/2}$] and 28.22 eV [$Ta4f_{5/2}$], and the binding energies

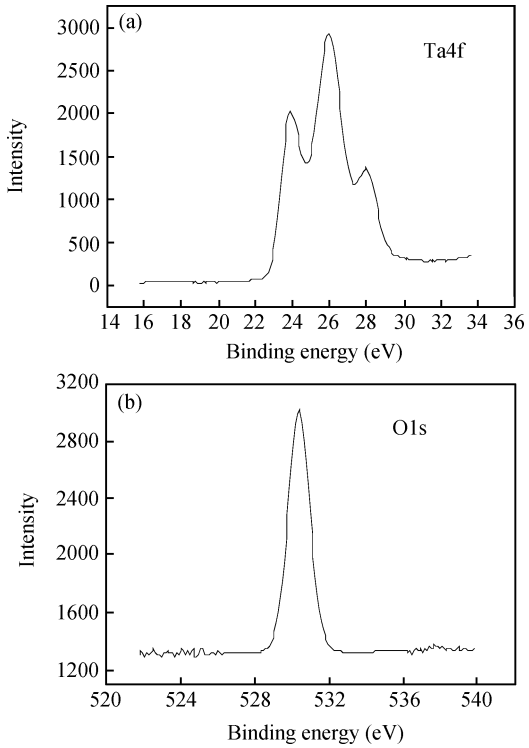


Fig. 1. XPS spectra obtained from the TaN layer exposed to ambient air: (a) Ta4f; (b) O1s.

for TaN are 23.61 eV [$Ta4f_{7/2}$] and 25.51 eV [$Ta4f_{5/2}$][8]. So, it is reasonable to regard the TaN surface as a combination of pure TaN and Ta native oxide, described as the $TaO_xN_y$ layer. The XPS spectra in Fig. 1(b) also show that the O1s peak corresponding to the Ta–O bonding was observed at a binding energy of 530.38 eV[9].

Another chance to oxidize the TaN surface is the standard PR descum process. Figure 2 presents the XPS spectra of the TaN surface that underwent the PR descum process in oxygen plasma for 5 min at 500 W. It shows strong Ta–O peaks and that TaN surfaces were strongly oxidized. So, the oxidation of the surface of TaN that was seen to inhibit the etching in the $NH_4OH/H_2O_2$ solution is presumably attributed to the standard PR descum process and exposure to air. In addition, because the PR descum process and exposure to air are inevitable, it will take a long time to etch TaN clearly in the $NH_4OH/H_2O_2$ solution, which is not compatible with the PR mask.

### 3.3. Two-step wet etching strategy

To reduce the impact of the $TaO_xN_y$ layer and realize selective etching of TaN with the PR mask, $Ar^+$ ion bombardment could be performed before wet etching with the $NH_4OH/H_2O_2$ solution. But it was found that the $HF/HNO_3$

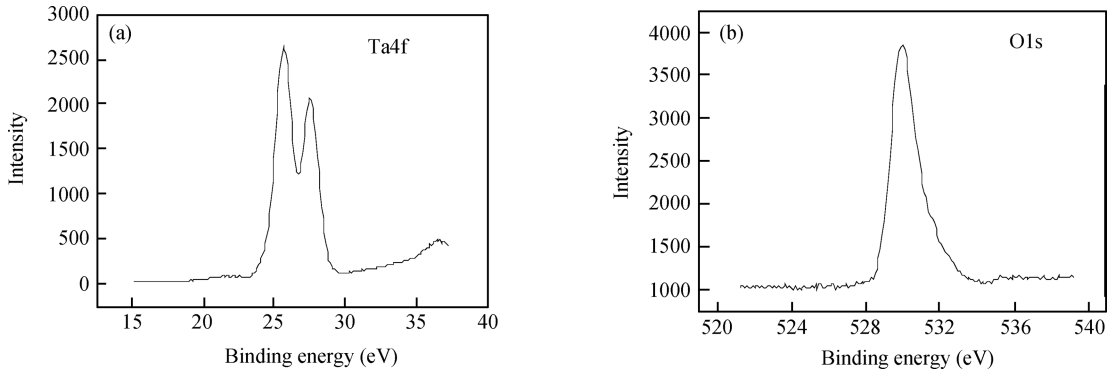


Fig. 2. XPS spectra of the TaN that performed after the PR descum process in oxygen plasma for 5 min at 500 W: (a) Ta4f; (b) O1s.

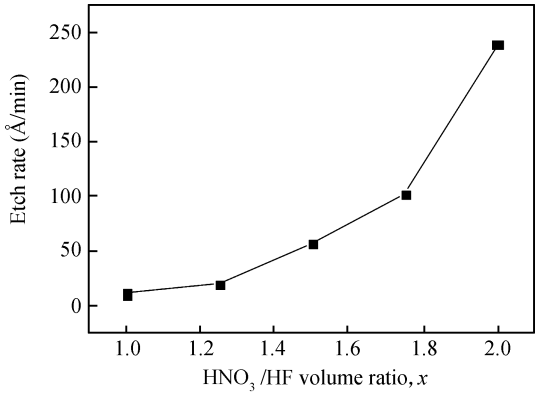


Fig. 3. Etch rate of TaN versus various $HNO_3$/HF volume ratios of $HF/HNO_3/H_2O$ solution.

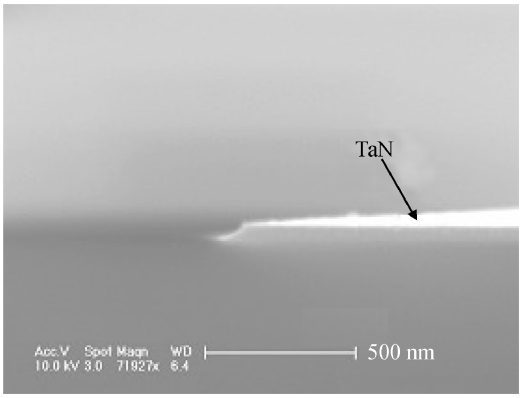


Fig. 4. Tilted SEM image after etching with two-step wet etching strategy.

$/H_2O$ etchant could etch not only the TaN film but also the $TaO_xN_y$ layer. The etch rates of samples fabricated two months ago etched by the $HF/HNO_3/H_2O$ solution with a volume ratio of 1 : $x$ : 5 at room temperature are shown in Fig. 3. The etch rate of the $HF/HNO_3/H_2O$ solution, as compared to the new sample, decreased due to forming a thicker $TaO_xN_y$ layer, but increasing the content of $HNO_3$ could achieve a reasonable etch rate. Therefore, the $TaO_xN_y$ layer will not be an insurmountable obstacle for etching of TaN as long as a $HF/HNO_3/H_2O$ solution is used to etch initially.

In order to realize selective etching of TaN with a PR mask and have high selectivity to the dielectric underneath, we introduce a two-step wet etching strategy: firstly, the $HF/HNO_3/H_2O$ solution removes surface oxidation of the TaN layer and parts of the TaN layer at room temperature; then, re-baking of the wafer at 180 °C for 35 min after the first etch step is required to maintain the adhesion between the TaN and PR; finally, the remaining TaN is removed in the $NH_4OH/H_2O_2$ solution at 60–70 °C. Although the first etch step with the $HF/HNO_3/H_2O$ solution at the optimum ratio did not damage the PR within 8 min, it was found that the suitable longest time for the first etch step is 6.5 min in the two-step wet etching strategy with the PR mask. So, the first etch step could only remove 370 ± 10 Å TaN at the most. After re-baking, the longest time allowed for the second etch step with the PR mask is 75 s because the PR mask can only remain stable in the $NH_4OH/H_2O_2$ solution for 1.5 min. Taking the non-uniformity of the wet etching and the necessary time of over-etching into account, there is less than 75 s to remove the remaining TaN for the second etch step. Therefore, the second etch step, which achieves high selectivity to the gate dielectric, could only remove less than 100 Å TaN even though the $NH_4OH/H_2O_2$ solution has a higher etch rate. Therefore, the two-step wet etching strategy that we propose is suitable for a thickness of TaN less than 450 Å with a PR mask owing to the damage of the PR mask in the wet etch solution. As shown in Fig. 4, 400 Å thick TaN could be fully removed by the two-step wet etching strategy with high selectivity to the gate dielectric, where the etching times of the $HF/HNO_3/H_2O$ solution and the $NH_4OH/H_2O_2$ solution were 375 s and 70 s respectively.

In addition, smooth film surfaces are preferred for lower gate leakage, higher reliability, and higher mobility. So, film surfaces were carefully studied using AFM after the fabrication of the TaN pattern on HfSiON. Figure 5(a) presents AFM images of the HfSiON surface after TaN removal with the two-step wet etching strategy. The HfSiON surface was relatively smooth with a RMS of 1.76 Å, which is comparable to the as-deposited HfSiON film (RMS = 1.59 Å, shown in Fig. 5(b)). Therefore, the two-step wet etching strategy could obtain a relatively smooth HfSiON gate dielectric surface.

### 3.4. Electrical results of MOSCAPs

The capacitance–voltage ($C$–$V$) characteristics and gate leakage–voltage ($J$–$V$) curves for the TaN/HfSiON gate stacks with and without wet etching in the $NH_4OH/H_2O_2$ solution with an optimum ratio at 70 °C are shown in Figs. 6 and 7. As shown in Fig. 6, etching HfSiON with the $NH_4OH/H_2O_2$

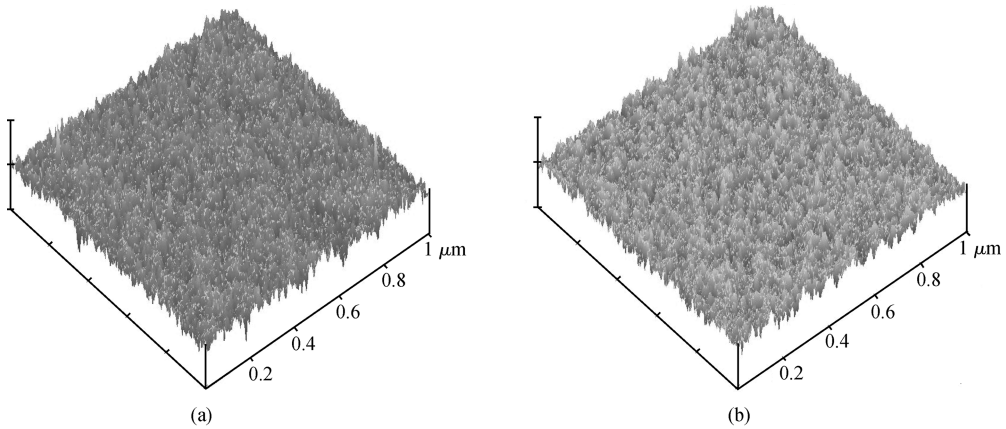


Fig. 5. AFM topography of HfSiON surface: (a) After etching with the two-step wet etching strategy; (b) As-deposited.

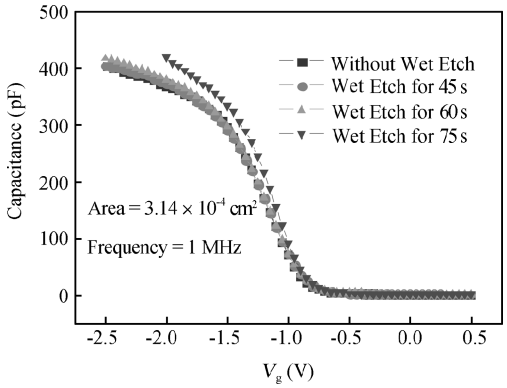


Fig. 6. *C*–*V* curves of TaN/HfSiON capacitors with and without wet etching.

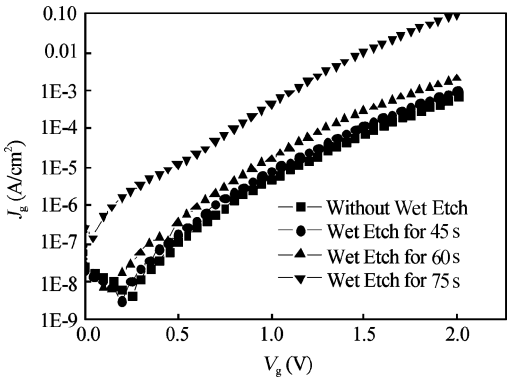


Fig. 7. *J*–*V* curves of TaN/HfSiON capacitors with and without wet etching.

solution for 75 s before TaN deposition resulted in a small $V_{fb}$ shift and an unacceptable EOT loss, but etching of 60 s and less than 60 s led to no flatband voltage shift and a very small EOT loss (less than 1 Å). These results also confirm that the $NH_4OH/H_2O_2$ solution wet etch has very high selectivity to the underlying HfSiON. As shown in Fig. 7, $J_g$ at $V_g = V_{fb} - 1$ V increased 1.5×, 3.3× and 144× for the TaN/HfSiON capacitors where the HfSiON received 45 s, 60 s, 75 s etching compared to the control capacitor. The $J_g$ increase can be accounted for entirely by the EOT loss of the gate dielectrics. So, we propose that our wet etch does not significantly affect the quality of the high-*k* if the over-etch time of the second step wet etching is less than or equal to 60 s, which is enough time to ensure the total removal of TaN on the whole wafer.

## 4. Conclusions

Wet etching etchants and a two-step etching strategy of thin TaN for dual-metal-gate integration have been presented. Highly selective etching of TaN film to the HfSiON gate dielectric was successfully achieved by a two-step wet etching process with a PR mask. More importantly, the wet etching of TaN has little impact on the electrical characteristics of a HfSiON/TaN gate stack. In conclusion, the two-step wet etching strategy is a simple and practical process to be integrated into dual-metal-gate CMOS devices.

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