A 3.1–4.8 GHz transmitter with a high frequency divider in 0.18 μm CMOS for OFDM-UWB*

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Abstract: A fully integrated low power RF transmitter for a WiMedia 3.1–4.8 GHz multiband orthogonal frequency division multiplexing ultra-wideband system is presented. With a separate transconductance stage, the quadrature up-conversion modulator achieves high linearity with low supply voltage. The co-design of different resonant frequencies of the modulator and the differential to single (D2S) converter ensures in-band gain flatness. By means of a series inductor peaking technique, the D2S converter obtains 9 dB more gain without extra power consumption. A divided-by-2 divider is used for carrier signal generation. The measurement results show an output power between –10.7 and –3.1 dBm with 7.6 dB control range, an OIP3 up to 12 dBm, a sideband rejection of 35 dBc and a carrier rejection of 30 dBc. The ESD protected chip is fabricated in the Jazz 0.18 μm RF CMOS process with an area of 1.74 mm^2 and only consumes 32 mA current (at 1.8 V) including the test associated parts.

Key words: multilband orthogonal frequency division multiplexing (MB-OFDM); ultra-wideband (UWB); transmitter; quadrature-modulator; divider; PGA

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1. Introduction

The emerging ultra-wideband (UWB) technology is being actively investigated today due to the wide available bandwidth for very high data rates up to 480 Mb/s and low power service over short distances in the 10 m range[1, 2]. According to FCC, the frequency spectrum allocated for UWB is 3.1–10.6 GHz, and the spectrum shapes of the modulated output power and maximum power level are limited to –41.3 dBm/MHz, which ensures that UWB can coexist with existing spectrum users like GSM, WLAN and Bluetooth. The WiMedia has proposed a standard based on the multilband orthogonal frequency division multiplexing (MB-OFDM) approach[3]. In this proposal, the UWB frequency spectrum from 3.1 to 10.6 GHz is divided into 14 channels with 528 MHz for each channel. The first three channels (3168 to 4752 MHz) are denoted band group #1.

This paper describes the implementation of an RF transmitter with a high frequency divider, covering 3.1–4.8 GHz (group#1) for MB-OFDM UWB in a 0.18 μm CMOS technology. This paper also describes the proposed transmitter architecture as well as its design constraints, and highlights the circuit design and implementation.

2. Architecture and design constraints

The band-group #1 has three channels, and their channel center frequencies are 3432 MHz, 3960 MHz, and 4488 MHz, each with a channel bandwidth of 528 MHz. The carrier frequency can hop between these three bands in different time slots. The transmitted power spectrum density and spectral mask are shown in Fig. 1.

Based on FCC's output spectral density requirement, the maximum transmitted power $P_{\rm TX}$ is about –9.3 dBm as calculated in Eq. (1). In order to compensate the power loss between the front-end and antenna (band pass filter used, etc), the actual power that is required at the output of the power amplifier is considered to be about –7 dBm.

$$P_{\rm TX,hop} = -41.25\,{\rm dBm/MHz} + 10\lg(3\times 528) = -9.3\,{\rm dBm}. \quad (1)$$

The proposed transmitter block diagram is shown in Fig. 2; it adopts direct conversion architecture, consisting of a voltage–current (V2I) converter, a quadrature up-conversion modulator, a D2S converter and a programmable gain amplifier (PGA). I/Q baseband signals (4.125–264 MHz) are converted to an RF signal at the output of the modulator. After

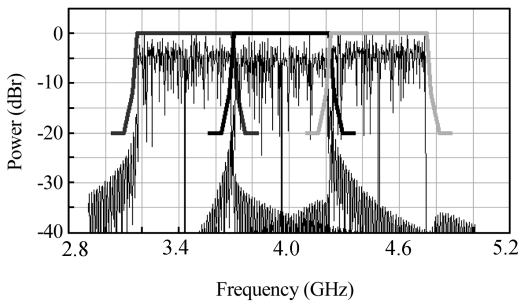

Fig. 1. Normalized transmitted spectral mask of band group #1.

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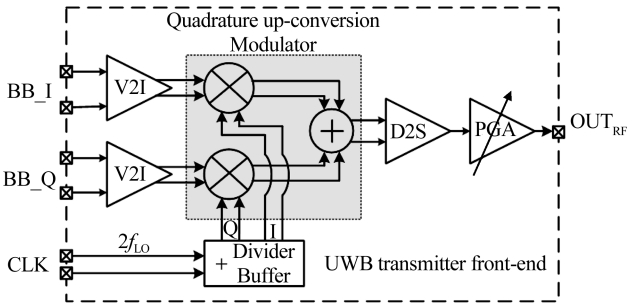

Fig. 2. Block diagram of the UWB transmitter.

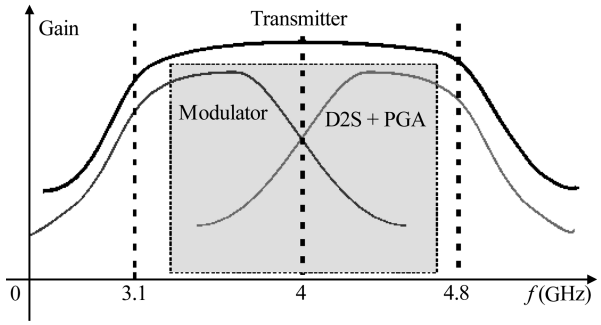

Fig. 3. Wideband gain with two resonant loads.

conversion to single-end by D2S and amplification by the PGA, the output RF signal can be sent directly to the antenna.

For chip testability purposes, a divided-by-2 divider with its LC buffer is proposed for orthogonal carrier frequency signal generation with a differential $2f_{\rm LO}$ frequency signal as the input.

The direct conversion architecture has the advantages of high integration, low power, low cost and so on, despite its inherent drawbacks like I/Q mismatch, dc-offset and $1/f$ noise. Due to these drawbacks, the design of a UWB transmitter having flat gain response in 3.1–4.8 GHz with high sideband signal suppression and carrier leakage suppression is a difficult task, especially in the case of the low power high linearity requirements under a 1.8 V supply voltage.

2.1. 3.1–4.8 GHz wideband gain flatness

Traditionally, a shunt-peaking load technique can be used to extend a circuit's bandwidth performance[4]. By this shunt-peaking technique, the frequency response of the quadrature up-conversion modulator can only be extended to a certain value but not enough from a whole transmitter flatness point of view. This is because the gain flatness is not determined by the modulator itself and the gain performance is worse if the Q factor of the shunt-peaking LC tank is lower for wider bandwidth.

To achieve ultra-wideband gain flatness, a method of combining two shunt-peaking loads with different resonant frequencies is proposed. As shown in Fig. 3, the load of modulator resonant frequency is around 3.5 GHz; D2S with the PGA's load resonant frequency is around 4.5 GHz; with proper adjustment, they can achieve a flat gain response for the transmitter chain over the full bandwidth of 3.1–4.8 GHz.

The desired wideband characteristics can be obtained by

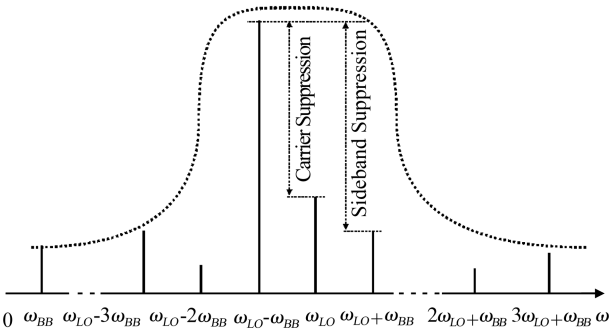

Fig. 4. Output spectrum components.

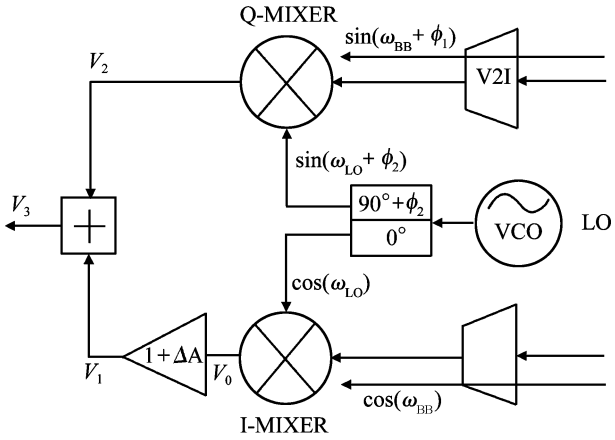

Fig. 5. Modulator with I/Q amp/phase mismatch.

optimizing the value of the peaking elements L, C and R. In actual circuit design, the load inductance L and shunt parasitic capacitor determine the resonant frequency; the load series resistance R is independent of this resonant frequency, but it can alter the Q factor of the resonant tank, which relates to the gain flatness.

2.2. Sideband and carrier leakage suppression

Ideally, the up-conversion modulator works as[4]

$$\cos\omega_{\rm BB}\cos\omega_{\rm LO} \pm \sin\omega_{\rm BB}\sin\omega_{\rm LO} = \cos\omega_{\rm LO} \mp \omega_{\rm BB}, \quad (2)$$

where $\cos\omega_{\rm BB}$, $\sin\omega_{\rm BB}$ are the input I/Q baseband signals; $\cos\omega_{\rm LO}$, $\sin\omega_{\rm LO}$ are the quadrature carrier signals. Due to the non-ideal factors in the direct conversion transmitter, the output spectrum consists of unwanted components. For example, the sideband signal at $\omega_{\rm LO} + \omega_{\rm BB}$ is caused by I/Q mismatch, the carrier leakage signal at $\omega_{\rm LO}$ is caused by the dc-offset, and the signals at $\omega_{\rm LO} \pm 3\omega_{\rm BB}$, $2\omega_{\rm LO} \pm \omega_{\rm BB}$, $3\omega_{\rm LO} \pm \omega_{\rm BB}$ are from the non-linearity of the modulator, as shown in Fig. 4. The out-band ones can be filtered out, leaving the modulator's linearity on the transconductance stage (the component at $\omega_{\rm LO} \pm 3\omega_{\rm BB}$).

The mismatch induced sideband signal degrades the output spectrum and linearity. Supposing the amplitude and phase mismatch come from both baseband and carrier path due to layout and process variation, as shown in Fig. 5, we can rewrite Eq. (2) as follows:

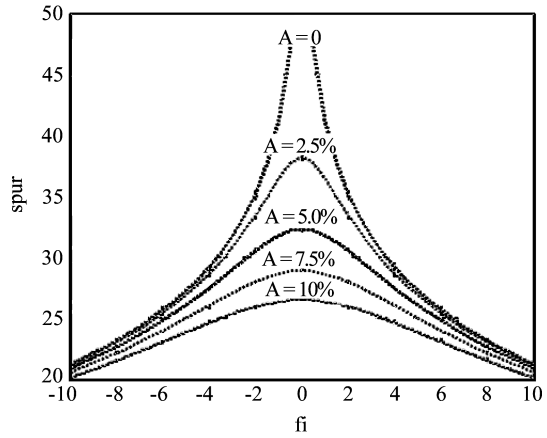

Fig. 6. SBRR with different amp/phase mismatches.

$$V_1 = (1+\Delta A)\cos\omega_1 t\cos\omega_2 t = \frac{1}{2}(1+\Delta A)[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t], \quad (3)$$

$$V_2 = \sin(\omega_1 t+\phi_1)\sin(\omega_2 t+\phi_2) = \frac{1}{2}[\cos(\omega_1 t-\omega_2 t+\phi_1-\phi_2) - \cos(\omega_1 t+\omega_2 t+\phi_1+\phi_2)]. \quad (4)$$

$$V_3 = V_1 + V_2 = \frac{1}{2}(1+\Delta A)\cos(\omega_1-\omega_2)t + \frac{1}{2}\cos[(\omega_1-\omega_2)t+(\phi_1-\phi_2)] + \frac{1}{2}(1+\Delta A)\cos(\omega_1+\omega_2)t - \frac{1}{2}\cos[(\omega_1+\omega_2)t+(\phi_1+\phi_2)]. \quad (5)$$

Here, $\omega_{BB} = \omega_1$ and $\omega_{LO} = \omega_2$, and the output fundamental signal and sideband signal can be expressed as

$$V_{Fund} = \frac{1}{2}(1+\Delta A)\cos(\omega_1-\omega_2)t + \frac{1}{2}\cos(\omega_1-\omega_2)t\cos(\phi_1-\phi_2) - \frac{1}{2}\sin(\omega_1-\omega_2)t\sin(\phi_1-\phi_2). \quad (6)$$

$$V_{Side} = \frac{1}{2}(1+\Delta A)\cos(\omega_1+\omega_2)t - \frac{1}{2}\cos(\omega_1+\omega_2)t\cos(\phi_1+\phi_2) + \frac{1}{2}\sin(\omega_1+\omega_2)t\sin(\phi_1+\phi_2). \quad (7)$$

The sideband rejection ratio (SBRR) can be defined as a power comparison between these two signals,

$$\mathrm{SBRR} = 10\lg\frac{|V_{Fund}|^2}{|V_{SB}|^2} = 10\lg\left(\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\phi_1-\phi_2)}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\phi_1+\phi_2)}\right). \quad (8)$$

In Eq. (8), $\cos(\phi_1-\phi_2)\approx 1$ and defining $\mathrm{fi} = \phi_1+\phi_2$, the output SBRR with different amplitudes and phase errors can be plotted in Fig. 6.

Ideally, $\phi_1 = \phi_2 = 0$ and $\Delta A = 0$, SBRR $= \infty$, there is no sideband signal at output; because the amplitude error is 2.5%, the phase error should be lower than 1.8 ° to achieve a sideband signal rejection larger than 35 dBc. This really is a tough task for wideband circuit design, because the up to 264 MHz input baseband signals limit the transistor size of the transconductance stage, which is where the mismatch comes from, due to process variation.

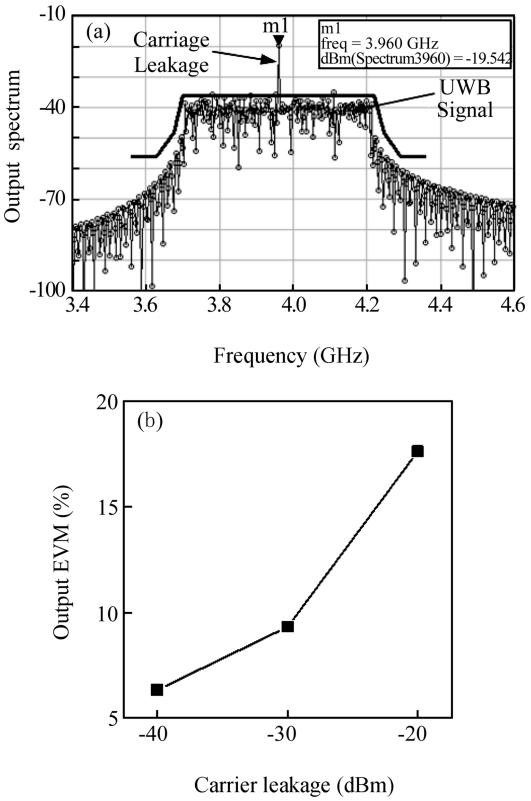

Fig. 7. Carriage leakage problem: (a) Output spectrum; (b) Output EVM.

Another drawback of the direct conversion architecture is the carrier leakage. Even if the baseband and modulator are a well balanced design, the process variation induced dc-offset still can cause a serious carrier leakage problem at the output of the modulator and this carrier signal together with the wanted signals will be amplified by the PGA to output. The carrier leakage at the output of the modulator is calculated as[4]:

$$V_{CL} = \frac{4R_L}{\pi}\Delta I_{OS}\cos\omega_{LO}. \quad (9)$$

Here, V_{CL} is the carrier leakage voltage; R_L is the load of modulator and I_{OS} is the baseband offset current to the modulator. Equation (9) shows that the carrier leakage is linearly proportional to the offset current caused by mismatch.

As shown in Fig. 7(a), carrier leakage can peak out of the signal band and cause EVM deterioration to exceed the specification, as shown in Fig. 7(b), which shows that a carrier suppression of 30 dBc or higher is necessary to keep the linearity unaffected by carrier leakage.

Other design issues such as high linearity modulator design with 1.8 V supply voltage, high frequency differential to signal converter design, gain control technique and low power consideration will be discussed in next section.

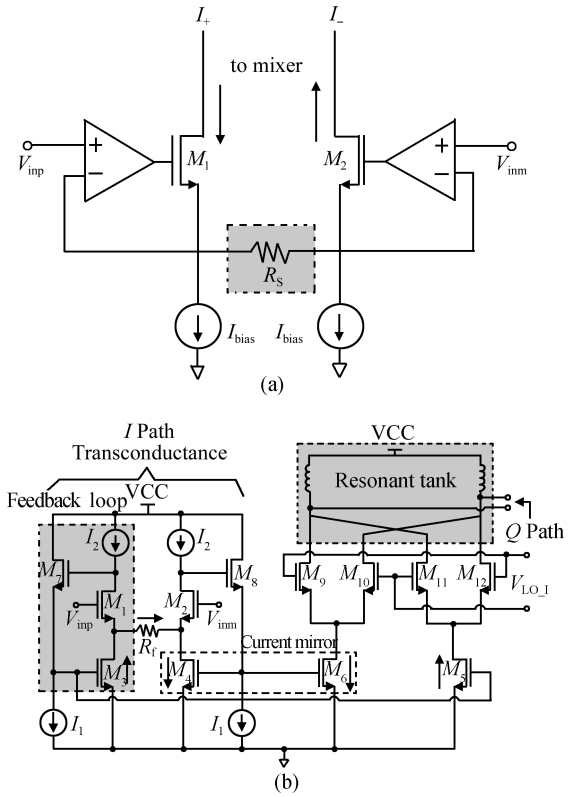

Fig. 8. (a) OTA assistant transconductance stage; (b) Simplified schematic of the proposed modulator.

3. Circuit design

3.1. Low voltage high linearity modulator

The design of the modulator determines the performance of the transmitter from three aspects: linearity, gain and its flatness, sideband and carrier suppression.

The I path schematic of the proposed modulator is shown in Fig. 8(b)[9]. The up-conversion mixer adopts double balanced Gilbert topology to suppress the carrier leakage and the transconductance stage uses source resistor degeneration to improve the linearity.

The widely used OTA assistant transconductance stage in Fig. 8(a) can achieve better linearity in principle[5], but it is not useful for low voltage and wideband applications. Because for the 264 MHz input baseband signal, the OTA's unit gain bandwidth (GBW) requires a very large current consumption.

In Fig. 8(b), the differential baseband input signal is applied at the gates of M1, M2, which have a constant drain current controlled by I_2. Helping with the feedback loop of M7, I_1, and M3, the applied voltage signals $V_{\rm inp}$ and $V_{\rm inm}$ are converted to current by the feedback resistor $R_{\rm f}$. The generated current I is circulated in M3, M4, which is amplified by the mirror transistor M5, M6 respectively and sent to the mixer stage. The transconductance of the modulator can be expressed as:

$$G_{\rm m} = \frac{i_{\rm out}}{v_{\rm in}} = \frac{1}{R_{\rm f}}\frac{W_{\rm M5}}{W_{\rm M3}} = \frac{k_0}{R_{\rm f}}. \tag{10}$$

Here, $i_{\rm out}$ is current to mixer, k_0 is the gate width ratio of M5 and M3, and $R_{\rm f}$ is the source degeneration resistor. Equation (10) shows that the transconductance is mainly determined by the feedback resistor $R_{\rm f}$. Compared with the common source input of the traditional Gilbert mixer, the transconductance stage can offer much better linearity and the 1.8 V supply voltage is enough for the overdrive voltage $V_{\rm DS6}$ plus $V_{\rm DS9}$ with the current mirror topology.

A large transistor size is appreciated for the transconductance stage to reduce the mismatch, which means better sideband and carrier signal suppression. The k_0 is 2 to compensate the gain drop due to the large feedback resistor for linearity.

At the output nodes, the modulated signals from I-path and Q-path are summed and converted to a voltage signal by the shunt peaking load of $R_{\rm L}$, $L_{\rm load}$ and the $C_{\rm load}$ (parasitic capacitor at the output nodes and the capacitor from the next stage). The differential inductor $L_{\rm load}$ is tuned to be resonant with the relatively constant $C_{\rm load}$ around 3.5 GHz as required in Fig. 3 and the Q-factor of the resonant tank is tuned by the resistor $R_{\rm L}$. In this design, $L_{\rm load}$ = 4.2 nH, $R_{\rm L}$ = 40 Ω.

Another important figure of merit for the modulator design is the linearity. The transfer function of the transconductance stage can be written as

$$i_{\rm in} = g_1 v_{\rm in} + g_2 v_{\rm in}^2 + g_3 v_{\rm in}^3, \tag{11}$$

and the switch function of the mixer is

$$i_{\rm o} = s_1 i_{\rm in} + s_2 i_{\rm in}^2 + s_2 i_{\rm in}^3. \tag{12}$$

Then the overall output transferred current is

$$\begin{aligned} i_{\rm o} &= g_1 s_1 v_{\rm in} + \left(g_2 s_2 + g_1^2 s_2\right) v_{\rm in}^2 \\ &\quad + \left(g_3 s_1 + 2 g_1 g_2 s_2 + g_1^3 s_3\right) v_{\rm in}^3 \\ &= d_1 v_{\rm in} + d_2 v_{\rm in}^2 + d_3 v_{\rm in}^3. \end{aligned} \tag{13}$$

Thus, the overall third-order intermodulation distortion ($\rm IM_3$) is:

$$\rm IM_3 = \frac{3}{4}\frac{d_3}{d_1} V_{in}^2 \approx \frac{3}{4}\left(\frac{g_3}{g_1} + \frac{s_3}{s_s} g_1^2\right) v_{\rm in}^2. \tag{14}$$

Here, $v_{\rm in}$ is the input baseband signal. The first and second terms in the bracket each stand for the distortion caused by the transconductance stage and the switch stage of the mixer. Normally, s_3/s_2 is small with the assumption of good switch character and can be ignored compared to the first term. The $\rm IM_3$ component from transconductance g_3/g_1 dominates the linearity of the modulator as

$$i_{\rm IM3} \approx \frac{3}{8}\frac{1}{R_{\rm f}^4 \sqrt{\beta}\sqrt{I_2^5}}, \tag{15}$$

where $\beta = \mu_{\rm n} C_{\rm OX} W/L$ of M3, M4 in Fig. 8(b), and I_2 is the bias current. From Eq. (15), we can see that the linearity can be improved by increasing the value of $R_{\rm f}$ or I_2 at the price of decreasing the gain, as can seen from Eq. (10), and increasing the power consumption. Also, increasing β by W/L can improve the linearity; the problem is that the parasitic capacitor at gate and drain limits the absolute transistor size. So a trade-off has to be made between these parameters in order to achieve a better linearity.

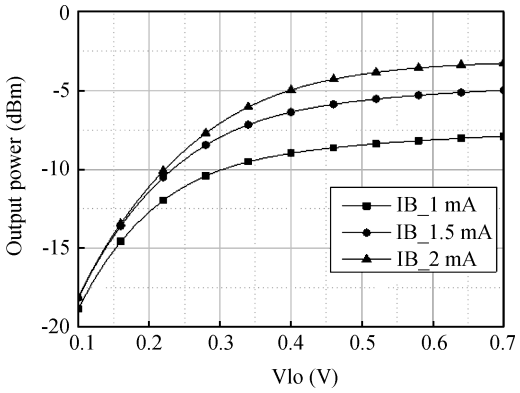

Fig. 9. Output power with different LO signals.

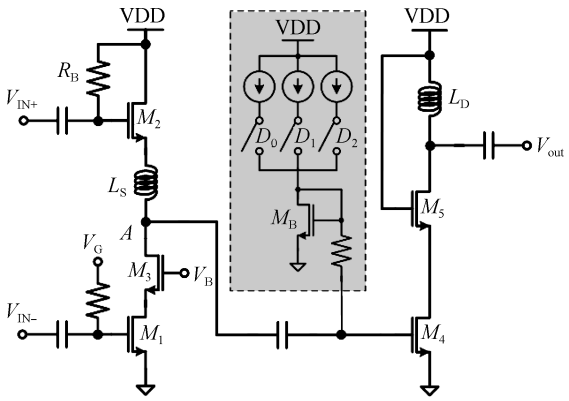

Fig. 10. Simplified schematic of the D2S and PGA.

To satisfy the above assumption for the linearity consideration, the transistors M9–M12 in Fig. 8(b) should work in a hard switch mode. One way is to increase the transistor's size or lower the bias current, but this will decrease the gain. The other way is to use a large LO signal to reduce the time that transistors M9 and M10 are both on. As shown in Fig. 9, with a differential LO signal larger than 400 mV, the output power saturates, which means that the switch transistor comes to hard switch[6].

3.2. D2S and PGA

A simplified D2S and PGA schematic is shown in Fig. 10. The modulator output differential signal is AC coupled to the D2S and the converted single-end RF signal is amplified by the PGA with a 3 bit gain-control range. The output signal can be sent directly to the antenna without an external balun, providing a higher on-chip integration compared to Ref. [7], where a differential PGA with an external balun is adopted.

The D2S is based on a common drain (M2) and common source (M1) pair as shown in Fig. 10; compared to the D2S in Ref. [8], M3 is used to reduce the Miller capacitance of M1 and improve the reverse isolation; an inductor L_S is inserted between M2 and M3 serving as a peaking element resonant with the parasitic capacitor at the output of the D2S. The small signal gain is:

$$\frac{V_{out}}{V_{in}} = \frac{2g_m + g_m C_{gs} L_s s^2 + \left(L_s g_m^2 + C_{gs}\right) s}{2\left[g_m + C_{gs} C_{load} L_s s^3 + C_{load} g_m L_s s^2 + \left(C_{gs} + C_{load}\right) s\right]}, \quad (16)$$

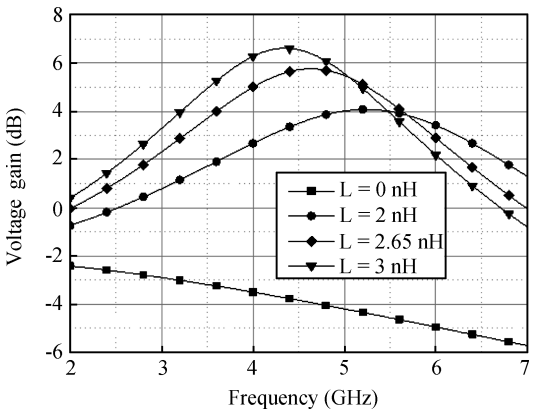

Fig. 11. Voltage gain response with inductor L_S.

where g_m is the transconductance of M1, M2; C_{gs} is the input gate-source capacitor and C_{load} is the total parasitic capacitance at point A. Figure 11 plots this voltage gain response with different values of L_S; it clearly shows that with proper L_S (2.65 nH), the gain can peak around 4.5 GHz as required in Fig. 3 and nearly 9 dB more gain can be obtained without extra current consumption compared to the case where no inductor is used.

The PGA uses a single-end common-source amplifier with a cascade configuration, as shown in Fig. 10. M5 can reduce the Miller capacitor to improve the isolation and gain performance, and prevent the M4 from being broken down by the possible high voltage of $2V_{DD}$ at the output. The output matching circuit consists of an on-chip inductor L_D and a coupling capacitor to the 50 Ω antenna. For the bias, a current mirror configuration between M4 and MB is used. By setting control bit D_0, D_1, D_2, the PGA gain can be varied to satisfy the output power requirement.

By co-design of modulator, D2S and PGA, gain flatness of the transmitter over 3.1–4.8 GHz is obtained with low power consumption. In Ref. [9], one path of the differential signal from the modulator is directly connected to the PGA, causing 6 dB gain loss. In Fig. 10, the differential signal is fully utilized and the passive inductor L_S can peak the gain without extra current consumption. The current in the single-end PGA is about half that of the differential amplifier used in Ref. [8] and it can be even lower in the case of a large input baseband signal with bias current control.

3.3. High frequency divider

For chip testability, the on-chip test circuit is required to generate quadrature carrier signals covering 3.1 to 4.8 GHz, with the amplitude and phase error as low as possible. A poly phase filter (PPF) can be used to generate the quadrature signals with the characteristic of precision[10], but a PPF is conventionally used in narrow band systems; the high order PPF gain attenuation and mismatch limit its wideband application. In this paper, a divided-by-2 divider is used for the quadrature carrier signal generation. It can work in a very wide frequency range, providing a relatively accurate and large carrier signal for high conversion gain. The issue is to design an up to

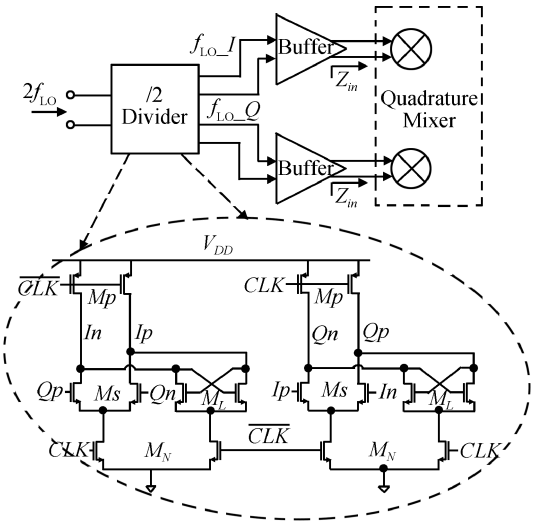

Fig. 12. Circuit schematic of dynamic-loading SCL[1] divider. SCL[1]: source coupled logic.

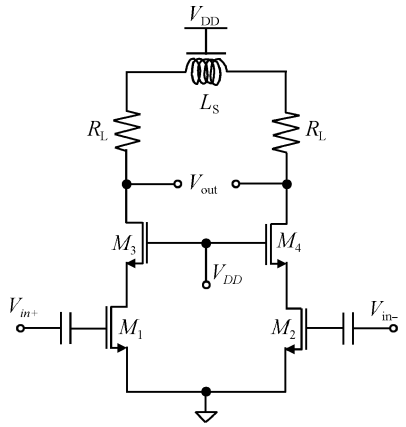

Fig. 13. LC buffer for the divider.

10 GHz divider in 0.18 μm CMOS. A signal diagram and circuit schematic of the divider are shown in Fig. 12.

The divider is based on source-coupled logic (SCL) with dynamic loading to provide the operation frequencies over 10 GHz[11]. The two D flip-flops always operate periodically and alternately between sensing and latching mode, enabling the output frequency to be half of the input frequency. Compared with the fixed resistor load SCL divider, the dynamic-load divider has the following advantages: (1) higher operation frequency with low conducting impedance when Mp is in the linear region; (2) lower power requirements for the same operation frequency; (3) lower sensitivity to process variation.

For the divider, it is a critical requirement that the big MOS-FETs of the modulator do not load the divider, because the time constant RC at the divider output determines the operation frequency of the divider. The lower the parasitic capacitance at the output of the divider, the higher the work frequency it can achieve. Considering the conversion gain performance of the modulator, a constant LO signal level at each channel is preferred. So the LC buffer shown in Fig. 13 is inserted between the divider and the modulator to solve these problems. The tuned inductor is shunt peaking with the parasitic capacitor and the wideband characteristic is controlled by the series resistor R_L. The post-layout simulation results

Table 1. Post-simulation results of the divider.

Input frequency	6 GHz (3 dBm)	8 GHz (3 dBm)	10 GHz (6 dBm)
CLK CLKB in	344 mV	544 mV	866 mV
Divider output	665 mV	493 mV	543 mV
Buffer output	695 mV	788 mV	729 mV

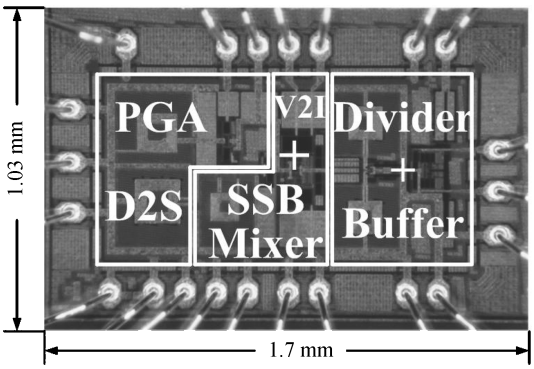

Fig. 14. UWB transmitter chip photograph.

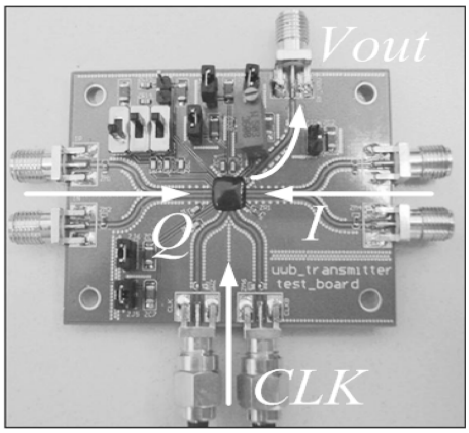

Fig. 15. PCB test board photo.

of the divider with an LC buffer are summarized in Table 1; it shows that the divider can work up to 10 GHz with high enough LO signals.

4. Implementation and measurements

The final UWB transmitter with a high frequency divider is fabricated in the Jazz 0.18 μm 1P6M RF CMOS process.

The chip die covers an area of 1.74 mm^2 including the pads, which are ESD protected with a tolerance of 1.36 kV, as shown in Fig. 14.

For the measurement, the chip uses chip-on-board (COB) packaging technology and Rogers4003c board material, as shown in Fig. 15.

For the spectrum measurement, 40 MHz baseband signals are supplied to the I/Q inputs and $2f_{LO}$ = 8 GHz. RF signals are supplied to the CLK/CLK$_{bar}$ of the divider, as shown in Fig. 15. The LO carrier frequency is 4 GHz, the modulated RF output is at 4040 MHz and the image side-band signal is at 3960 MHz. An output spectrum at this band is shown in Fig. 16; the carrier leakage and the side-band suppression are 30.1 dB and 35.6 dB respectively. This result also demonstrates that the divider can provide relatively accurate quadra-

Table 2. Key performance parameter comparison.

Parameter	Ref. [1]	Ref. [7]	Ref. [8]	Ref. [9]	This work	
					Post-Sim[13]	Test results
Technology	0.13 μm CMOS	90 nm CMOS	90 nm CMOS	0.25 μm GeSi	0.18 μm CMOS	
OIP_3 (dBm)	—	–1.41	10	9	14	12/11/4.8
OP_{1dB} (dBm)	–10	—	n/a	—	4	–1/–3.5/–6
P_{out} (dBm)	–10	–5.7	–10/–12/–8	–6.8	–8 to –2	–7 (controllable)
Carrier suppression (dBc)	–30	–35.2	–41[a)]	–28	–34	–30.1
Image suppression (dBc)	–28	–33.8	–49[b)]	–32	–44	–35.6
Power control range (dB)	0	0	n/a	13	6	7.6
Power: $I \times V$(mW)	n/a	$60 \times 1.2/72$	$75 \times 1.2/90$	$43 \times 2.7/116$	$32 \times 1.8/57.6$[c)]	

[a)] with DC offset compensation; [a)] and [b)] do not have the same comparison standard (which is thought to be incorrect); [c)] core circuit is about 17 mA.

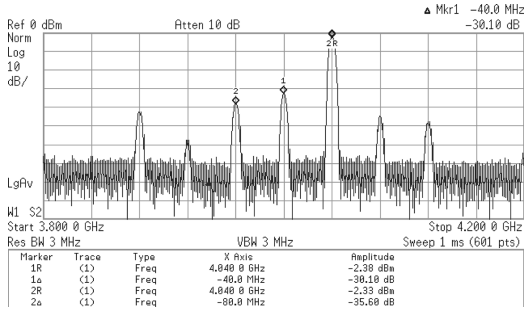

Fig. 16. Measured single-tone output spectrum at 3960 band, with LO leakage and image suppression.

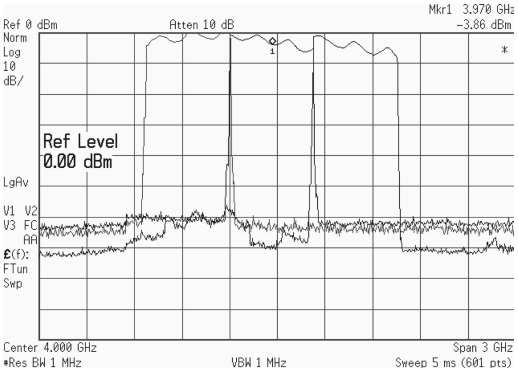

Fig. 17. Output power of transmitter in 3 bands. The figure is the "maximum hold" of the output power at any frequency in the 3 bands, not the power density proposed by FCC as shown in Fig. 1.

ture LO signals, as required in Fig. 6.

The output power of the transmitter in bands 1 to 3 is shown in Fig. 17; the output power is around –7 dBm with a variation of less than 3 dB in the first two bands. At band 3, the gain drops more compared with band 2, so a power control bit D_0 is on to compensate the gain drop. The high frequency gain drop comes from the larger parasitic capacitance than expected and the inaccurate simulation results due to the PDK model with large signal analysis. Figure 18 shows about 7.6 dB output power control range at band 1, 2 by $D_2D_1D_0$, in this band, and the output power displays much flatness with a variation of less than 3 dB.

The output 1 dB compression points at three bands are shown in Fig. 19. The results show that band 1 has the best

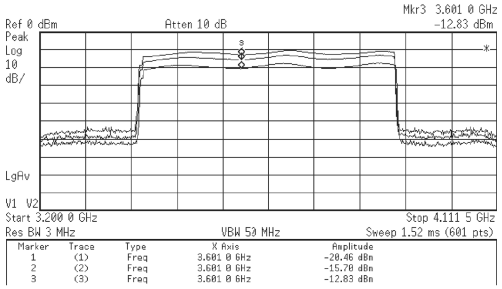

Fig. 18. Output power control range at bands 1, 2 with $D_2D_1D_0$.

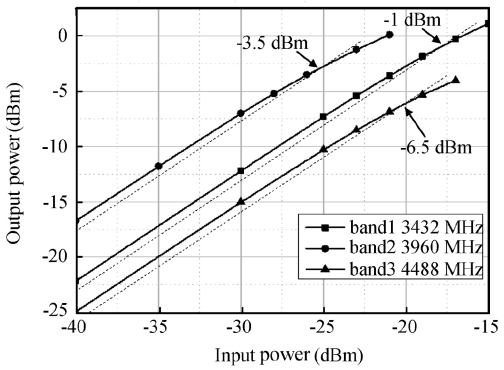

Fig.19. Output 1 dB compression point at three bands.

linearity and the value degrades as frequency increases due to gain loss, but it is still above –6.5 dBm at band 3. With a two tone test, the corresponding output third order intercept point (OIP3) at band 3 is shown in Fig. 20, and better values at bands 1 and 2 are 12 dBm and 11 dBm, not shown here. Table 2 compares the post-simulation and measurement results; the difference comes from the extra parasitic capacitance and inaccurate PDK model with large signal simulation.

The measurement results are summarized in Table 2 along with recently published work. A comparison shows that the transmitter performance is competitive with a lower cost process and low power consumption.

5. Conclusion

A low power RF transmitter with a high frequency divider design for 3.1–4.8 GHz MB-OFDM UWB is presented. With the co-design of the D2S and PGA, it achieves the re-

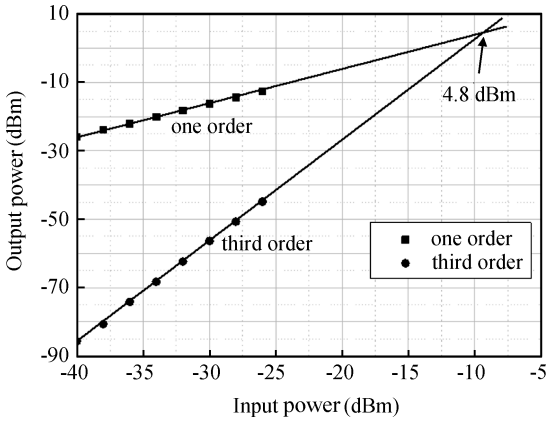

Fig. 20. Output third-order intercept point of the RF transmitter.

quired single-ended output power with a gain control range of 7.6 dB. By using the passive inductor series-peaking technique, the full chip consumes only 32 mA current from a 1.8 V supply. The results also demonstrate that the divider is suitable for high frequency wideband measurements. The transmitter front-end has been integrated into a complete UWB transceiver.

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