Clear correspondence between gated-diode R–G current and performance degradation of SOI n-MOSFETs after F–N stress tests*

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Abstract: A clear correspondence between the gated-diode generation–recombination (R–G) current and the performance degradation of an SOI n-channel MOS transistor after F–N stress tests has been demonstrated. Due to the increase of interface traps after F–N stress tests, the R–G current of the gated-diode in the SOI-MOSFET architecture increases while the performance characteristics of the MOSFET transistor such as the saturation drain current and sub-threshold slope are degraded. From a series of experimental measurements of the gated-diode and SOI-MOSFET DC characteristics, a linear decrease of the drain saturation current and increase of the threshold voltage as well as a like-line rise of the sub-threshold swing and a corresponding degradation in the trans-conductance are also observed. These results provide theoretical and experimental evidence for us to use the gated-diode tool to monitor SOI-MOSFET degradation.

Key words: MOSFET degradation; F–N stress; interface traps; gated-diode method; SOI technology
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1. Introduction

SOI devices are of great interest for low-voltage low-power CMOS circuits, memory and high frequency and high temperature applications. The main advantages are related to improved isolation, reduced sub-threshold slope, parasitic capacitance and low leakage currents, as well as possible reduction of the short channel effects compared with bulk silicon devices. However, when the devices are scaled down, SOI MOSFETs also suffer from hot carrier effects. In order to control and model transistor performance, it is essential to accurately monitor hot carrier injection-induced interface states in SOI MOSFETs.

Recently, a refined forward gated-diode method has been used to characterize the interface states and extract the bulk carrier recombination lifetime in SOI devices[1–3]. This method uses the gate-voltage-controlled interfacial recombination generation current (R–G) I_{R-G} to monitor the generation rate of interface traps and the charging rate of oxide traps in MOSFETs. Some very good results have been achieved with this simple, sensitive, quickly applicable and nondestructive method.

However, traditional transistor reliability measurements monitor the shifts in the saturation drain current ΔI_{dsat}, threshold gate voltage ΔV_{th}, maximum trans-conductance ΔG_m, and sub-threshold voltage swing ΔS of the MOSFET transistors[4,5]. Although the forward gated-diode method can also be well applied for studying the performance degradation of nano-scale FinFET devices[6], for the purposes of simplification and obtaining a clear figure, a large-scale PD SOI device is used to demonstrate the anticipated dependences of these traditional characteristics on the forward gated-diode R–G current from experiments with MOSFET's F–N stress tests.

2. Experiment

The experiments were performed in a PD SOI n-channel MOSTFET, fabricated on a SIMOX wafer. This tested SOI-MOST has a drawn channel length/width aspect ratio of L/W = 30 μm/15 μm, a 16 nm gate oxide, and separate source, drain, gate, and body contact pads. The top review of the fabricated SOI device and the experimental set-up are shown in Figs. 1(a) and 1(b), respectively.

During the stress-and-measure (SAM) experiments, the nMOSFETs are stressed by F–N tunneling current under the conditions of a constant gate voltage of 5 V and different stress times while their electrical characteristics are measured after each stress duration. In each gated-diode method experiment, the R–G current is obtained under the conditions that the source and drain are connected to ground while applying a biased voltage V_b of 0.35 V to the body contact. As a result, the source and drain/body contact forms a forward diode. By scanning the gate voltage, we can obtain the R–G current characteristics modulated by the gate voltage. In each measure-

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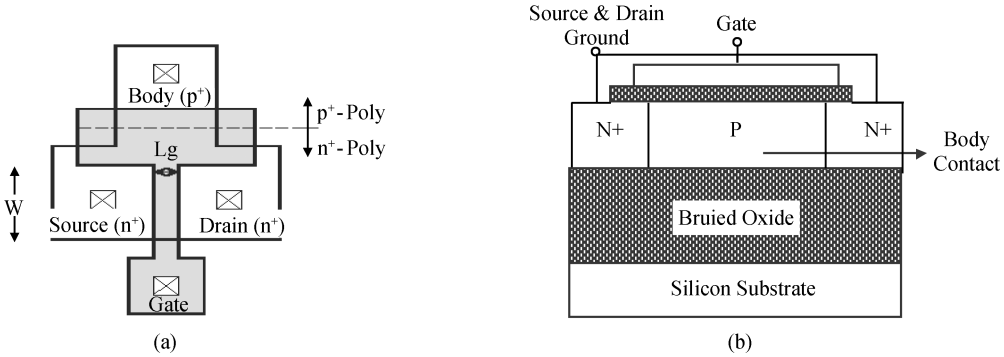

Fig. 1. (a) Top view of the fabricated SOI device; (b) Diagram of the experimental set-up.

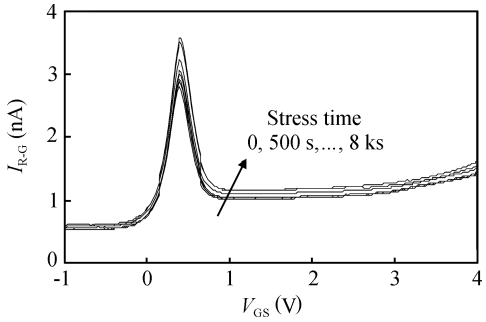

Fig. 2. Dependence of R–G current on F–N stress time.

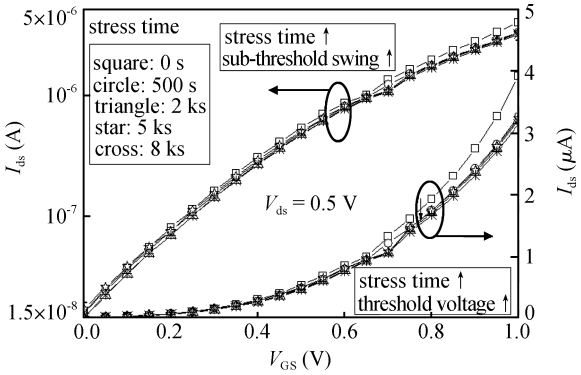

Fig. 3. Typical transfer characteristics of SOI n-channel MOSFET devices with different F–N stress times.

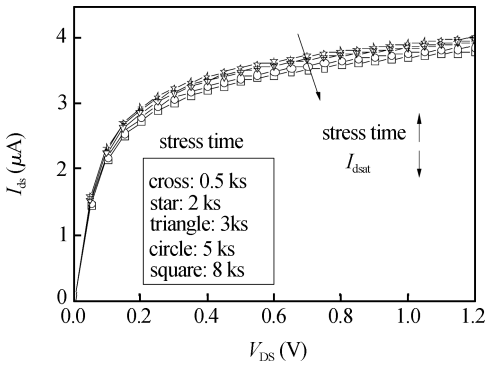

Fig. 4. Typical output characteristics of the n-channel SOI MOSFET device under different F–N stress times.

ment of the MOSFET performance, the drain saturation current is measured at V_{DS} = V_{GS} = 1.0 V. The threshold voltage is defined as the gate voltage at I_{ds} = 1 μA with V_{DS} = 0.5 V. The sub-threshold slope is computed at I_{ds} = 100 nA with V_{DS} = 0.5 V while the maximum trans-conductance is obtained from the same curve.

3. Results and discussion

Figure 2 shows the typical gated-diode I_{R-G}–V_G characteristics with increasing accumulated stress time of an nMOST stressed by the F–N effect. As seen in this figure, the $I_{R-G-peak}$ increases with F–N stress time and occurs at a nearly constant $V_G \approx 0.45$ V. The rise of $I_{R-G-peak}$ is due to the stress-generated SiO_2/Si interface traps over the channel space-charge region. The negligible V_G shift of the $I_{R-G-peak}$ indicates negligible charging of the oxide fixed charges over the total channel space-charge region because the F–N stress effect does not have sufficient kinetic energy, $KE = q(V_{DS} - V_{DS-sat}) \approx q[V_{DS} - (V_{GS} - V_T)] \approx 3.3$ eV – 1.6 eV = 1.7 eV, to surmount the 3.13 eV SiO_2/Si barrier[7].

The typical transfer characteristics of this n-channel device with different F–N stress times are shown in Fig. 3 with stress time ranging from 0, 500, 2000, 5000, to 8000 s and a drain voltage V_{ds} of 0.5 V. The stress-induced widening of the sub-threshold swing and the corresponding threshold voltage shift can be observed in this figure. As the stress time increases, the sub-threshold swing increases as well as the threshold voltage extracted by linear extrapolation. According to our requirement mentioned above, the sub-threshold swing and the threshold voltage for different F–N stress times can be extracted and the dependence on stress time is obtained.

Figure 4 shows the dependence of the drain current on the sets of stress conditions. This linear dependence is anticipated from the simple textbook theory of I_{dsat} and V_{GT}. Carrier mobility degradation in the channel should be responsible for the decrease of the drain current in the linear region. The greater decrease of the drain current in the saturation region is determined by two key factors, the mobility degradation and the threshold voltage shift. From the simple square equation of the MOST current, $I_{dsat} = (W/2L)C_{ox}\mu_{eff}(V_{GS} - V_{th})^2$, the output characteristic degradation with stress time is easy tounderstand. It is obvious that saturation current I_{dsat} degrades with increasing stress time due to the mobility and threshold voltage degradation.

Based on our obtained R–G current of the gated-diode, transfer curve and output curve characteristics of the n-channel SOI MOSFET device, it is easy to perform a correspon

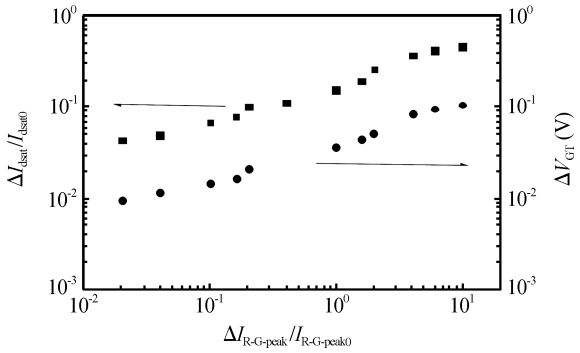

Fig. 5. Extracted correspondence between $\Delta I_{\rm dsat}/I_{\rm dsat0}$, $\Delta V_{\rm th}$ and $\Delta I_{\rm R-G-peak}/I_{\rm R-G-peak0}$ from the measured gated-diode R–G current and the SOI-MOSFET output characteristics.

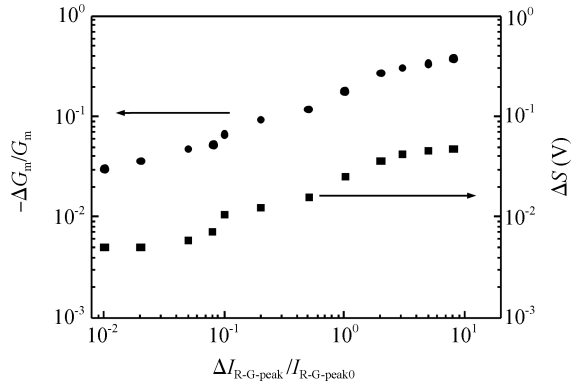

Fig. 6. Extracted correspondence between ΔS, $\Delta G_{\rm m}/G_{\rm m}$ and $\Delta I_{\rm R-G-peak}/I_{\rm R-G-peak0}$.

dence analysis between the R–G current and the performance degradation of the MOSFET after F–N stress tests.

Figure 5 demonstrates the linear dependence of $\Delta I_{\rm dsat}$ and $\Delta V_{\rm th}$ on $\Delta I_{\rm R-G-peak}$ for the F–N stress effect. This linear relationship is anticipated from the simple theory of $I_{\rm dsat}$ and $V_{\rm th}$ from the parabolic equation of the MOST output characteristics in the saturation region, mentioned above; we obtain $I_{\rm dsat}/I_{\rm dsat0} \approx -(2\Delta V_{\rm th})(V_{\rm G}-V_{\rm th})$ where $I_{\rm dsat0}$ denotes the pre-stress value. Since $\Delta V_{\rm th} = -q(\Delta N_{\rm ot}+\Delta N_{\rm it})C_{\rm ox}$ and $I_{\rm R-G-peak} \propto N_{\rm it}$, the oxide traps can be negligible from Fig. 2; we can immediately obtain $\Delta I_{\rm dsat} \propto \Delta V_{\rm th} \propto I_{\rm R-G-peak}$. As shown in Fig. 5, both $\Delta I_{\rm dsat}/I_{\rm dsat0}$ and $\Delta V_{\rm GY}$ are linearly dependent on $\Delta I_{\rm R-G-peak}/I_{\rm R-G-peak0}$ in a log–log plot.

The calculated sub-threshold swing variation and the trans-conductance degradation are shown in Fig. 6. It increases initially as $\Delta S \propto \Delta I_{\rm R-G-peak}$, then rises faster, and finally approaches $\Delta S \propto \Delta I_{\rm R-G-peak}$ again. This is consistent with the simple expression $S = 2.303(kT/q)[1+(C_{\rm it}+C_{\rm d})/C_{\rm ox}]$ where $C_{\rm it} = qN_{\rm it}$ which indicates an initial and final linear dependence, $\Delta S \propto \Delta C_{\rm it} \propto qN_{\rm it} \propto I_{\rm R-G-peak}$, while the super-linear rise of ΔS in the mid-range of stress is caused by faster change of the surface potential with $\Delta V_{\rm th}$ relative to the change of $N_{\rm it}$. The trans-conductance degradation of $\Delta G_{\rm m}/G_{\rm m}$ can be explained in a similar way. However, due to the unique kink feature of PD SOI MOSFET devices, the trans-conductance degradation of this SOI device demonstrates more complexity.

4. Conclusions

The clear correspondence between performance degradation of an SOI n-channel MOS transistor and gated-diode R–G current after F–N stress tests has been studied experimentally. Proof is given of the theoretically expected dependence of saturation drain current, threshold voltage, sub-threshold swing and trans-conductance degradation on the gated-diode R–G current peak. This correlation provides the basis for using the forward gated-diode method to monitor MOS transistor degradation.

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