# Fabrication and characteristics of the nc-Si/c-Si heterojunction MAGFET*

Zhao Xiaofeng(赵晓锋)[1,2] and Wen Dianzhong(温殿忠)[1,2,†]

*(1 Key Laboratory of Electronics Engineering, Collage of Heilongjiang Province, Heilongjiang University, Harbin 150080, China)*

*(2 Major Laboratories of Integrated Circuits, Heilongjiang University, Harbin 150080, China)*

**Abstract:** A MAGFET using an nc-Si/c-Si heterojunction as source and drain was fabricated by CMOS technology, using two ohm-contact electrodes as Hall outputs on double sides of the channel situated $0.7L$ from the source. The experimental results show that when $V_{DS} = -7.0$ V, the magnetic sensitivity of the single nc-Si/c-Si heterojunction magnetic metal oxide semiconductor field effect transistor (MAGFET) with an $L : W$ ratio of 2 : 1 is 21.26 mV/T, and that with an $L : W$ ratio of 4 : 1 is 13.88 mV/T. When the outputs of double nc-Si/c-Si heterojunction MAGFETs with an $L : W$ ratio of 4 : 1 are in series, their magnetic sensitivity is 22.74 mV/T, which is an improvement of about 64% compared with that of a single nc-Si/c-Si heterojunction MAGFET.

**Key words:** nc-Si/c-Si heterojunction; MAGFET; CMOS technology; serial output; magnetic sensitivity

**DOI:** 10.1088/1674-4926/30/11/114002 **PACC:** 7340L; 7340Q

## 1. Introduction

The Hall effect was discovered by Dr. Edwin Hall in 1879 at Johns Hopkins University. The MOS device was first proposed as a magnetic sensor by Gallagher and Corak in 1966. A MAGFET (magnetic metal oxide semiconductor field effect transistor) consists of a MOSFET structure with additional contacts in the channel region.

In recent years, with the development of CMOS technology, a large number of MAGFET studies have been carried out at home and abroad[1,2]. By studying the influence of channel size and channel shape (rectangular, concave, convex type, sector, etc.) on the magnetic properties of the MAGFET[3–9], the magnetic sensitivity of the MAGFET could be improved.

In this paper, a MAGFET is fabricated on n-type ⟨100⟩ crystal silicon with high resistance ($\rho > 100\ \Omega\cdot$cm) by CMOS technology, using an nc-Si/c-Si heterojunction as source and drain, with a Hall output as the series output to improve its magnetic sensitivity.

## 2. Basic structure and operation principle

### 2.1. Basic structure

The basic structure of the nc-Si/c-Si heterojunction MAGFET is shown in Fig. 1: (a) top view, (b) cross-section A–A′ of the nc-Si/c-Si heterojunction MAGFET. The nc-Si/c-Si heterojunction MAGFET has a source, drain, gate, substrate and the two ohm-contact electrodes, which are taken as Hall outputs on double sides of the channel situated $0.7L$ from the source. The nc-Si/c-Si heterojunction MAGFET source and substrate are connected together, so $V_{BS} = 0$ V.

### 2.2. Operation principle

Equations (1) and (2) respectively give the $I$–$V$ characteristic equations of the p-MOSFET lying in the linear and saturation fields[10]:

$$I_{DS} = -\frac{\mu_p C_{ox}}{2}\frac{W}{L}\left[2\left(|V_{GS}| - |V_{TP}|\right)|V_{DS}| - |V_{DS}|^2\right], \quad (1)$$

$$I_{DS} = -\frac{\mu_p C_{ox}}{2}\frac{W}{L}\left(|V_{GS}| - |V_{TP}|\right)^2, \quad (2)$$

where $\mu_p$ is the carrier mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $W$ and $L$ are channel width and length, $V_{TP}$ is the threshold voltage, $V_{GS}$ is the gate to source voltage, and $V_{DS}$ is the drain to source voltage.

The operation principle of the single nc-Si/c-Si heterojunction MAGFET is shown in Fig. 2. When there is no magnetic field ($B = 0$), drain current distribution is uniform, as shown in Fig. 2(a).

Theoretically, the Hall outputs on both sides of the channel should be the same potential; the Hall output voltage is:

$$V_H = V_{H1} - V_{H2} = 0. \quad (3)$$

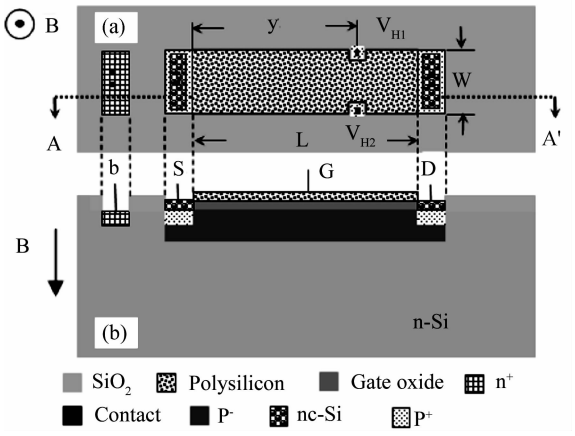


Fig. 1. Basic structure of the nc-Si/c-Si heterojunction MAGFET: (a) Top view; (b) Cross-section A–A′.

* Project supported by the National Natural Science Foundation of China (No. 60676044) and the Science and Technology Research Program of Heilongjiang Provincial Department of Education (No. 11521215).

† Corresponding author. Email: wendianzhong@126.com

Received 21 May 2009

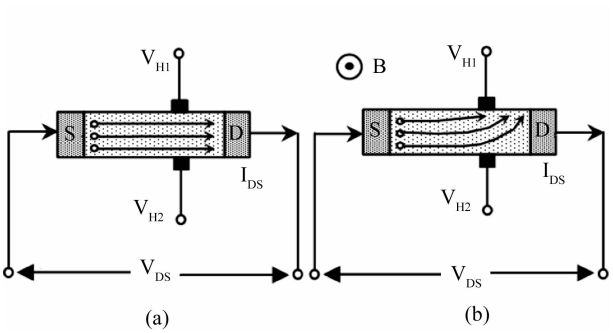


Fig. 2. Operation principle of the nc-Si/c-Si heterojunction MAGFET: (a) $B = 0$ T; (b) $B \neq 0$ T.

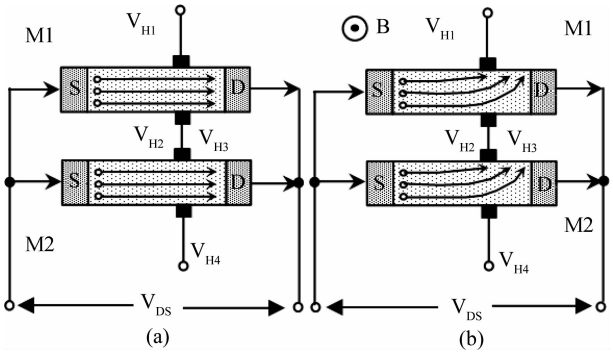


Fig. 3. Series output of the double nc-Si/c-Si heterojunction MAGFETs: (a) $B = 0$ T; (b) $B \neq 0$ T.

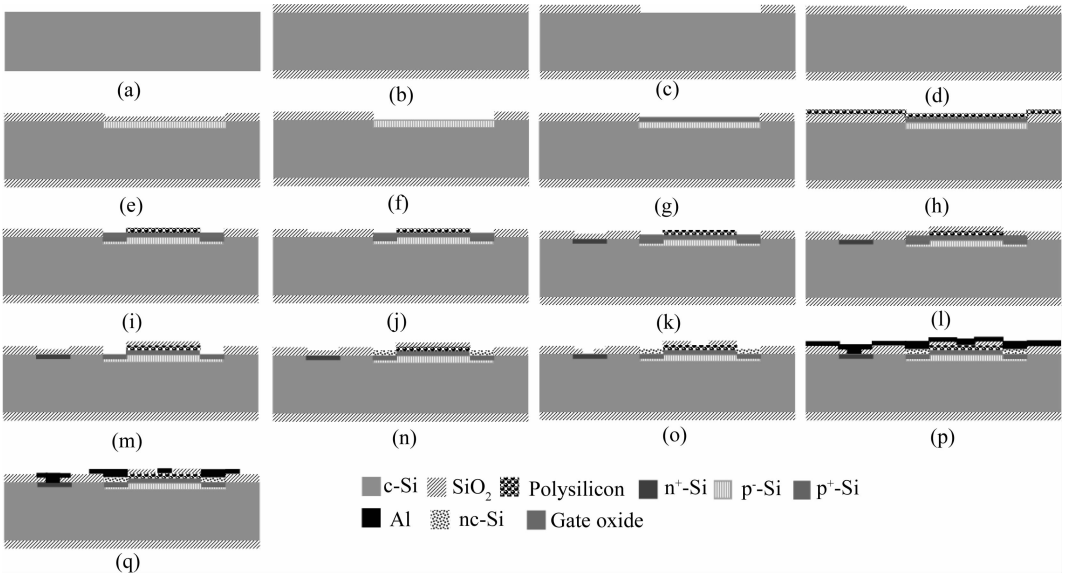


Fig. 4. Fabrication process of the nc-Si/c-Si heterojunction MAGFET.

When an additional magnetic field $B$ is applied orthogonally to the MAGFET gate surface, the Lorentz force will force the channel carriers to deflect, which will change the current $I_{\mathrm{DS}}$. The Hall voltage $V_{\mathrm{H}}$ of the single nc-Si/c-Si heterojunction MAGFET generated by a magnetic field $B$ perpendicular to the MAGFET surface is given by

$$V_{\mathrm{H}} = \mu_{\mathrm{p}} \frac{W}{L} \frac{|V_{\mathrm{DS}}|}{2\left[1 - \frac{x}{L}\right]^{1/2}} B \cdot f'_{\mathrm{H}}\left(\frac{L}{W}, \theta\right), \tag{4}$$

where $x$ is the Hall output electrode position, and $f'_{\mathrm{H}}\left(\frac{L}{W}, \theta\right)$ is the geometrical correction factor.

Series output structure diagrams of the double nc-Si/c-Si heterojunction MAGFETs are shown in Fig. 3. When there is no magnetic field ($B = 0$), the Hall voltages of M1 and M2 are as follows:

$$V_{\mathrm{H}} = V_{\mathrm{M1}} - V_{\mathrm{M2}} = (V_{\mathrm{H1}} - V_{\mathrm{H2}}) - (V_{\mathrm{H3}} - V_{\mathrm{H4}}) = 0. \tag{5}$$

When a magnetic field $B$ is applied to the nc-Si/c-Si heterojunction MAGFET, the Hall voltages of M1 and M2 are as follows:

$$V_{\mathrm{H}} = V_{\mathrm{M1}} - V_{\mathrm{M2}} = 2\mu_{\mathrm{p}} \frac{W}{L} \frac{|V_{\mathrm{DS}}|}{2\left[1 - \frac{x}{L}\right]^{1/2}} B\, f'_{\mathrm{H}}\left(\frac{L}{W}, \theta\right). \tag{6}$$

Using Eqs. (4) and (6), under the same working conditions, the series Hall output voltage of the double nc-Si/c-Si heterojunction MAGFETs is theoretically twice that of the single nc-Si/c-Si heterojunction MAGFET.

## 3. Fabrication

Figure 4 shows the fabrication technology process of the nc-Si/c-Si heterojunction MAGFET chip: (a) n-type ⟨100⟩ double sided polished single crystal silicon wafer with high resistance and thickness 450 $\mu$m; (b) first oxidation: thermal oxidation process to grow silicon oxide ($SiO_2$) with thickness of 650 nm; (c) first lithography to form the active region window of the nc-Si/c-Si heterojunction MAGFET; (d) second oxidation: thermal oxidation process to grow silicon oxide ($SiO_2$) with thickness of 50 nm in order to improve ion implantation uniformity; (e) using an ion implantation machine to obtain p-type implantation by injecting B ions: the energy of the implanted ions is 40 keV, and the dose of the implanted ions is 6.0 $\times 10^{13}$ cm$^{-2}$; (f) etching silicon oxide ($SiO_2$) with thickness of 50 nm; (g) third oxidation to grow gate oxide with thickness of 50 nm; (h) depositing polysilicon by LPCVD and polysilicon P diffusion; (i) second lithography, etching polysilicon to form a polysilicon gate and B ion implantation, so that the MOSFET source and drain with p-type doping are formed; (j) third lithography to form substrate contact hole opening; (k)

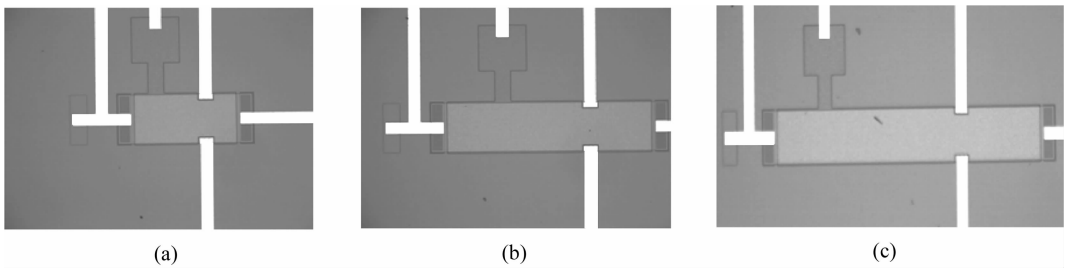


Fig. 5. Basic structure photographs of the nc-Si /c-Si heterojunction MAGFET with different channel length-width ratios: (a) $L : W = 2 : 1$; (b) $L : W = 4 : 1$; (c) $L : W = 6 : 1$.

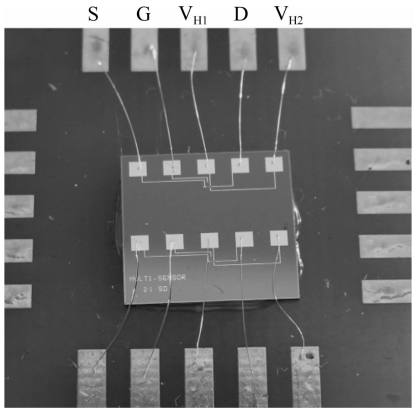


Fig. 6. Package structure photograph of the nc-Si/c-Si heterojunction MAGFET chip.

implanting P to form $n^+$ substrate; (l) polysilicon oxide to grow silicon oxide with thickness of 59.7 nm; (m) fourth lithography to source and drain of the p-MOSFET; (n) depositing nc-Si thin films with thickness of 30 nm by LPCVD and fifth lithography; (o) sixth lithography to etch contact hole opening; (p) depositing aluminum electrode by magnetron sputtering on the positive silicon wafer; (q) seventh lithography to form aluminum electrodes, source, drain, gate, substrate and Hall output electrode contacts of the nc-Si/c-Si heterojunction MAGFET.

Figures 5(a), 5(b) and 5(c) respectively show structure photographs of the nc-Si/c-Si heterojunction MAGFET chips with different channel length-width ratios of 2 : 1, 4 : 1 and 6 : 1. Figure 6 is a package test structure photograph of the nc-Si/c-Si heterojunction MAGFET chip, which shows the source (S), drain (D), gate (G), substrate (B) and Hall output $V_{H1}$, $V_{H2}$ of the sensor.

## 4. Experimental results and discussion

### 4.1. Magnetic characteristics

At room temperature, the magnetic characteristics of the nc-Si/c-Si heterojunction MAGFET were tested by an HP34401A multimeter and a magnetic field generator; the additional magnetic field range was from –0.5 T to 0.5 T, the supply voltage $V_{DS}$ is 0 to –7.0 V, $V_{BS}$ = 0 V, and the gate is vacant.

When the supply voltage $V_{DS}$ is given different values, Figures 7(a), 7(b), 7(c) show the respective magnetic characteristic curves for Hall output voltage $V_H$ and the additional magnetic field $B$ of the single nc-Si/c-Si heterojunction

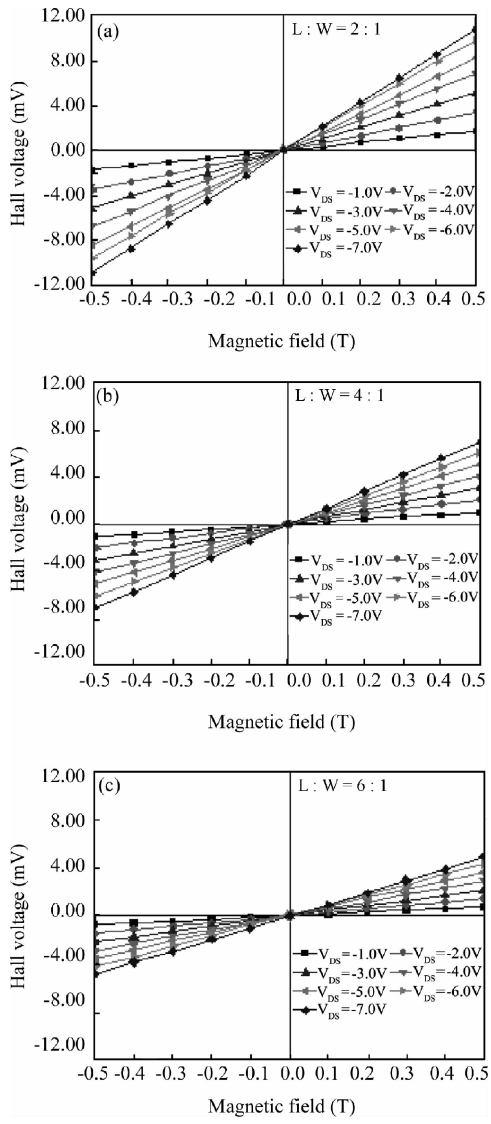


Fig. 7. Magnetic characteristics curves of the MAGFET at room temperature: (a) $L : W = 2 : 1$; (b) $L : W = 4 : 1$; (c) $L : W = 6 : 1$.

MAGFET with $L : W$ ratios of 2 : 1, 4 : 1 and 6 : 1. When the additional magnetic field $B$ is constant, with an increasing absolute value of supply voltage $V_{DS}$, the output voltage $V_H$ of the nc-Si/c-Si heterojunction MAGFET gradually increases. When the supply voltage $V_{DS}$ = –7.0 V, the magnetic sensitivity of the single nc-Si/c-Si heterojunction MAGFET with an $L : W$ ratio of 2 : 1 is 21.26 mV/T, and the accuracy is 1.834% FS; the magnetic sensitivity of the single nc-Si/c-Si heterojunction MAGFET with an $L : W$ ratio of 4 : 1 is 13.88 mV/T, and that with an $L : W$ ratio of 6 : 1 is 9.76 mV/T.

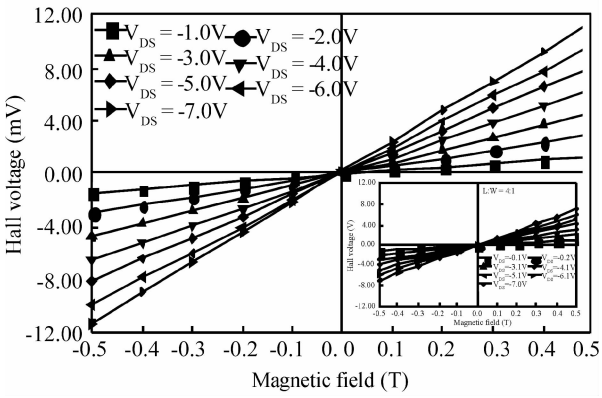


Fig. 8. Magnetic characteristics curves of series output of the double nc-Si/c-Si heterojunction MAGFETs with length-width ratio of 4 : 1.

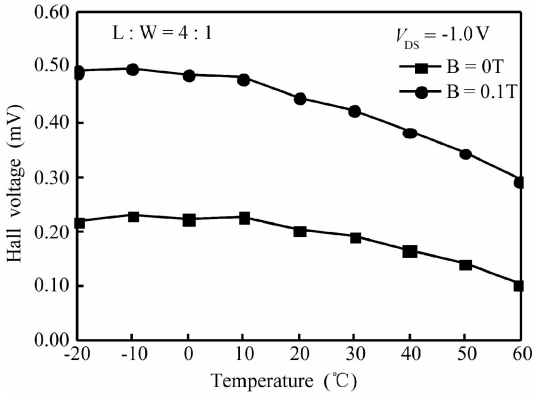


Fig. 9. Temperature characteristics curves of the nc-Si/c-Si heterojunction MAGFET with length-width ratio of 4 : 1.

Figure 8 shows the magnetic characteristic curves of the series outputs of the double nc-Si/c-Si heterojunction MAGFETs with an $L$ : $W$ ratio of 4 : 1; the iconograph shows the magnetic characteristics curves of the single nc-Si/c-Si heterojunction MAGFET. By using the nc-Si/c-Si heterojunction as a series output, when $V_{DS}$ = –7.0 V, the magnetic sensitivity of the double nc-Si/c-Si heterojunction MAGFETs with an $L$ : $W$ ratio of 4 : 1 is 22.74 mV/T, which is an improvement of about 64% compared with that of the single nc-Si/c-Si heterojunction MAGFET.

### 4.2. Temperature characteristics

A Shanghai Blue Leopard LGS-010C high and low temperature chamber was used to do high and low temperature experiments on the nc-Si/c-Si heterojunction MAGFET with a ratio of 4 : 1 from –20 to 60 °C when the supply voltage $V_{DS}$ was –1.0 V; the experimental curves of temperature characteristics for the single nc-Si/c-Si heterojunction MAGFET are shown in Fig. 9.

By using a certain magnetic field $B$ and the supply voltage $V_{DS}$, the Hall voltage temperature coefficient is given in Eq. (7):

$$\alpha = \frac{1}{V_H}\frac{\partial V_H}{\partial T} = \frac{V_H(T_2) - V_H(T_1)}{V_H(T_1) \times (T_2 - T_1)} \times 100\% \approx -0.439\%/^{\circ}\mathrm{C}, \quad (7)$$

where $V_H(T_1)$ is the Hall voltage of the temperature $T_1$, and $V_H(T_2)$ is the Hall voltage of the temperature $T_2$.

## 5. Conclusion

A MAGFET using an nc-Si/c-Si heterojunction as source and drain was fabricated by CMOS technology; its magnetic sensitivity is proportional to the absolute value of the supply voltage $V_{DS}$. When $V_{DS}$ = –7.0 V, the magnetic sensitivities of the single nc-Si/c-Si heterojunction MAGFET with length–width ratios of 2 : 1, 4: 1, 6 : 1 are 21.26 mV/T, 13.88 mV/T and 9.76 mV/T, respectively. By using the series Hall output of the double nc-Si/c-Si heterojunction MAGFETs with an $L$ : $W$ ratio of 4 : 1, the magnetic sensitivity of the MAGFET is 22.74 mV/T, which is an improvement of about 64% compared with that of the single MAGFET, 13.88 mV/T. The experimental results show that by using the double nc-Si/c-Si heterojunction MAGFETs series output, the magnetic sensitivity of the nc-Si/c-Si heterojunction MAGFET could be clearly improved.

## References

[1] Rao G R M, Carr W N. Magnetic sensitivity of a MAGFET of uniform channel current density. Solid-State Electron, 1971, 14: 995

[2] Rodríguez-Torres R, Gutiérrez-Domínguez E A. Analysis of split-drain MAGFETs. IEEE Trans Electron Devices, 2004, 51: 2237

[3] Yao Yunruo, Zhu Dazhong, Guo Qing. Sector split-drain magnetic field-effect transistor based on CMOS technology. Sensors and Actuators A, 2005, 121: 347

[4] Yao Yunruo, Zhu Dazhong. Sector split drain MAGFET structure and model based on standard CMOS technology. Chinese Journal of Semiconductors, 2005, 26: 751

[5] Guo Qing, Zhu Dazhong, Yao Yunruo. CMOS magnetic sensor integrated circuit with sectorial MAGFET. Sensors and Actuators A, 2006, 126: 154

[6] Sung G M. Error correction for transformed concave and convex MAGFETs with dc supply voltage. Sensors and Actuators A, 2005, 117: 41

[7] Cruz C A M, Ferraz E A. MAGFET with embedded Gilbert gain cell. Proceedings of the 7th International Caribbean Conference on Devices, Circuits and Systems, Mexico, 2008: 28

[8] Blanchard H, de Montmollin F, Hubin J, et al. Highly sensitive Hall sensor in CMOS technology. Sensors and Actuators A, 2000, 82: 144

[9] Vandooren A, Cristoloveanu S, Flandre D, et al. Hall effect measurements in double-gate SOI MOSFETs. Solid-State Electron, 2001, 45: 1793

[10] Lau J, Ko P K, Chan P C H. Modeling of split-drain magnetic field effect transistor. Sensors and Actuators A, 1995, 49: 155