A constant-g_m and high-slew-rate operational amplifier for an LCD driver*

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Abstract: To drive the backplane of a liquid crystal display device and achieve different kinds of grey levels, a high-slew-rate operational amplifier with constant-g_m input stage is presented. A Zener-diode structure is inserted between the tails of the complementary input pairs to keep the g_m of the input stage constant. A novel slew rate enhancement circuit is implemented to achieve a very high slew rate. The chip has been implemented in a 0.5 μm CMOS process and the chip area of the operational amplifier circuit is 0.11 mm^2. The testing results indicate that in the 5–8 V input range, the maximum g_m fluctuation is only 4.2%. The result exhibits a high slew rate of 111 V/μs and 102 V/μs for the rising and falling edges under a 20 pF capacitance load, and the low frequency gain is up to 109 dB with a phase margin of 70 °C.

Key words: constant-g_m; operational amplifier; Zener diode; slew rate
DOI: 10.1088/1674-4926/30/12/125002 **EEACC:** 1205; 1220

1. Introduction

The operational amplifier is an essential block in the driver of a thin film transistor-liquid crystal display (TFT-LCD), and can provide source and sink current alternately, so that output voltage fluctuations can be rejected effectively[1]. A number of techniques are used to control the dc bias current of input differential pairs to keep the total g_m of the input stage constant, including square root circuits[2] and 1 : 3 current mirror circuits[3]. Another example is using tunable level shifters and a single differential pair to obtain a constant g_m[4]. These methods need circuitry such as switch and current mirrors, making the input stage much more complicated than the generic input stage.

On the other hand, the requirements for the output buffer in a high quality flat-panel-display (FPD) are high resolution, large voltage swing, and driving speed[5]. Slew rate enhancement is an effective way to obtain a high driving speed. Many two-stage operational amplifiers with class AB output stage which have been discussed are characterized by relatively modest effective slew rate improvement factors[6, 7], but they require complex circuitry, increased supply voltage or PSRR degradation[8]. Reference [9] enhances slew rate by significantly increasing the maximum swing at internal nodes of the OTA, but the resistors connected between the drain and gate of the load transistors need to be calculated precisely.

The proposed rail-to-rail operational amplifier with high driving capability is presented on the basis of the 0.5 μm CMOS process, using a Zener-diode[10] structure inserted between the tails of the complementary input pairs to keep the g_m of the input stage constant. Also, the high slew rate is optimized without affecting the electrical characteristics and the power dissipation of the whole circuit. Measurement results show that the proposed circuit exhibits good performance. In the 5–8 V input range, the maximum g_m fluctuation is only 4.2%. The slew rate is 111 V/μs and 102 V/μs for the rising and falling edges under a 20 pF capacitance load.

2. Architecture of the proposed amplifier

2.1. Principle of the proposed g_m-control design

The well known complementary input stage structure is shown in Fig. 1, where double differential pairs, M1/M4 and M2/M3, are utilized. The problem arises that the g_m varies over the input common-mode voltage range. This variation still blocks a power-efficient frequency compensation of the operational amplifier. Hence, effort should be focused on the design of the constant-g_m control. As illustrated in Fig. 1, a good feature of the input stage with a Zener-diode structure applied here is to keep the sum of the gate-source voltages of the input transistors, consisting of M5, M6, constant, and therefore the total g_m of the input stage remains constant.

The principles of the g_m-control can be best understood by dividing three parts of the common-mode voltage. The

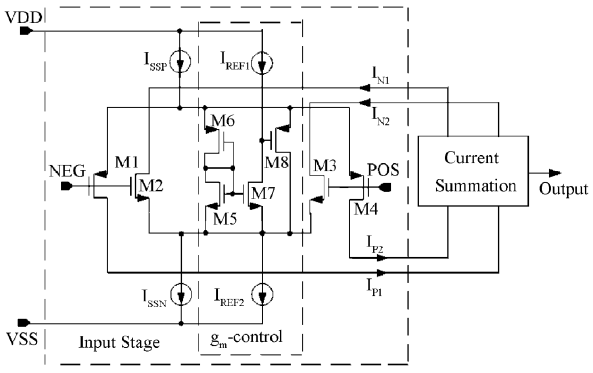

Fig. 1. Input stage with constant-g_m control using the Zener-diode structure.

* Project supported by the National Natural Science Foundation of China (No. 60876023).
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Received 26 May 2009, revised manuscript received 13 July 2009

equivalent g_m of the input stage is:

$$g_{m(equal)} = g_{mP} + g_{mN} =$$

$$\begin{cases} 2K(|V_{GSP}| - |V_{THP}|), & \text{low-voltage region,} \\ 2K(V_{GSN} + |V_{GSP}| - V_{THN} - |V_{THP}|), & \text{mid-voltage region,} \\ 2K(V_{GSN} - V_{THN}), & \text{high-voltage region,} \end{cases} \tag{1}$$

where g_{mN} and g_{mP} are the g_m of NMOS and PMOS input stage pairs, V_{TH} is the threshold voltage of the MOSFET, and the factor K is the g_m parameter which is given by:

$$K = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_N = \frac{1}{2}\mu_P C_{OX}\left(\frac{W}{L}\right)_p, \tag{2}$$

where μ_n and μ_p are the mobility of the electron and hole, and C_{OX} is the gate oxide capacitance per unit area.

As the value of common-mode voltage is very high or low, the voltage between the tails of the PMOS and NMOS transistor pair is comparably low. As a consequence, the Zener-diode structure is inactive. In the mid-voltage region, the voltage between the tails of the PMOS and NMOS transistor pair increases and the Zener-diode structure starts to operate. In this case, the voltage between the tails of the PMOS and NMOS transistor pair increases and the Zener-diode structure starts to operate. Therefore the voltage between of the sources of the input stage is obtained as:

$$V_{SM1} - V_{SM2} = |V_{GSM1}| + V_{GSM2} = V_{GSM5} + V_{GSM6}, \tag{3}$$

where V_{SM1} and V_{SM2} are the source voltages of M1 and M2. Note that, in order to keep total g_m constant over the input common-mode voltage range, it is necessary to make sure that the sum of the gate–source voltages of M1 and M2 is constant. With M7, M8, I_{REF1} and I_{REF2}, if the current through M5 and M6 increases, M7 turns on and the gate voltage of the M8 declines. Consequently, M8 is in parallel with M5 and M6, and removes part of the tail current. As a result, the current through M5 and M6 remains invariable. In the realization, the size of M6 and M8 must be the same as that of M1 and M4, while the size of M5 and M7 has to be equal to that of M2 and M3. In conclusion, the principal advantage of this g_m-control technique over the existing methods is that it results in a very compact structure which takes up a smaller area of the whole chip. Furthermore, this structure does not introduce additional quiescent current.

2.2. Frequency compensation

For stability, two frequency compensation stages are used as shown in Fig. 2, where g_{m1} and g_{m2} are the g_m of the input and output stage respectively. One is Miller compensation and the other is zero compensation with a resistor added between two push-pull output stages for stable driving under different capacitance loads. Assuming C_{O1}, $C_{O2} < C_C < C_L$; R_C, $R_L < R_{O1}$, R_{O2}; $g_{m2}R_L < 1$; and A_{dc} is the dc gain of the open-loop, the open-loop transfer function can be obtained as:

$$A_O(s) = A_{dc}\frac{(1 + s/\omega_{Z1})(1 + s/\omega_{Z2})}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}, \tag{4}$$

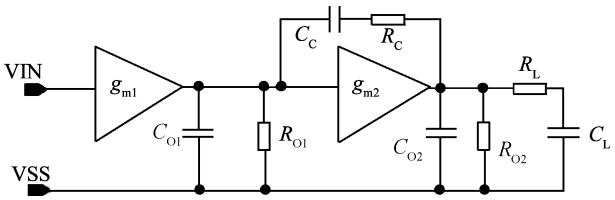

Fig. 2. Miller compensation for system stability.

where

$$\begin{cases} \omega_{Z1} = \dfrac{1}{R_L C_L}, \\ \omega_{Z2} = \dfrac{1}{(R_C - 1/g_{m2})C_C}, \\ \omega_{P1} \cong \dfrac{1}{R_{O1}(g_{m2}R_{O2})C_C + R_{O2}C_L}, \\ \omega_{P2} \cong \dfrac{C_L + g_{m2}R_{O1}C_C}{R_{O1}C_C C_L}. \end{cases} \tag{5}$$

Based on the Miller effect, the dominant pole ω_{P1} is related to the compensation capacitor C_C. Therefore, the value of C_C determines the system's stability. Here, resistor R_C is introduced to cancel the RHP zero and to achieve a better high-frequency dynamic range. Furthermore, a proper resistor load at the output node can also reduce the output impedance for better stability.

2.3. Slew rate enhancement

The setting time of an operational amplifier is a composite parameter, which is affected by the slew rate and the frequency response[11].The slew rate is defined by the maximum available current to charge up all the capacitance (including parasitic and compensation capacitance):

$$SR = \frac{I_{MAX}}{C_{tot}}. \tag{6}$$

The slew rate enhancement is illustrated in Fig. 3. Take the high-voltage region as an example where only NMOS transistors operate: if there is no slew rate enhancement circuit, the voltage V_X will decrease and M12 will be off during the positive slewing. As a result, M3 and its tail current source will be in the linear region. Apparently, it takes a long time for V_X to return to its normal operating point after M2 turns on.

To overcome this weakness, a slew rate enhancement circuit is introduced. Positive slewing can be understood as two parts: (1) In the high-voltage input region where only NMOS transistors operate, the tail current I_{SSN} totally passes through M3. In this case, M17 will be on as the voltage V_X declines. Consequently the current mirror (M21, M22, M27 and M28) is operational, which increases the current of discharging the output node capacitance of the input stage. (2) In the low-voltage region where only PMOS input transistors are active, the current through M1 is equal to the tail current I_{SSP}. At this time, the voltage V_P increases and M19 is active so that M14 cannot be off, avoiding a much higher swing of V_P after M4 turns on. A similar discussion can show that the current to charge the output node capacitance of the input stage increases when the negative slewing occurs. Obviously, the output node slew rate of the input stage can be expressed as:

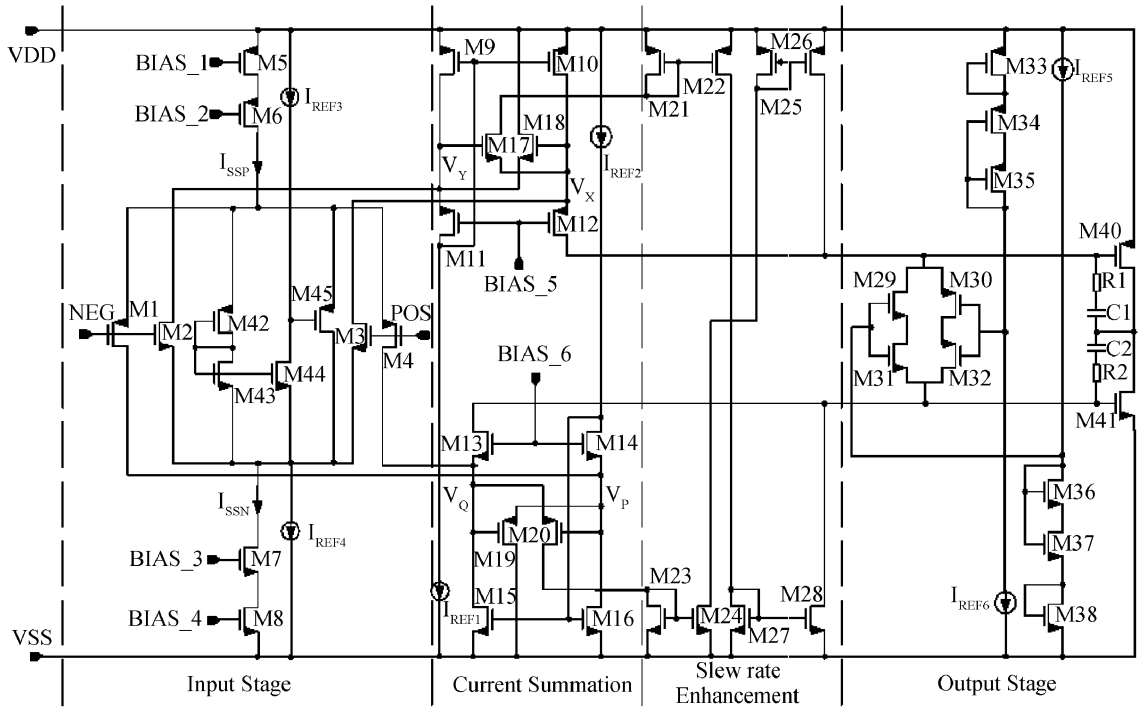

Fig. 3. Realization of the compact operational amplifier.

$$\mathrm{SR}^{+}=\begin{cases}\left(I_{\mathrm{SSP}}+I_{\mathrm{REF2}}-I_{\mathrm{M19}}\right)/C_{\mathrm{tot}}, & \text{low-voltage region,}\\ \left(\left(I_{\mathrm{SSP}}+I_{\mathrm{REF2}}-I_{\mathrm{M19}}\right)+K_1\left(I_{\mathrm{SSN}}-I_{\mathrm{REF1}}\right)\right)/C_{\mathrm{tot}}, & \text{mid-voltage region,}\\ K_1\left(I_{\mathrm{SSN}}-I_{\mathrm{REF1}}\right)/C_{\mathrm{tot}}, & \text{high-voltage region,}\end{cases} \tag{7}$$

$$\mathrm{SR}^{-}=\begin{cases}K_2\left(I_{\mathrm{SSP}}-I_{\mathrm{REF2}}\right)/C_{\mathrm{tot}}, & \text{low-voltage region,}\\ \left(\left(I_{\mathrm{SSPN}}+I_{\mathrm{REF1}}-I_{\mathrm{M18}}\right)+K_2\left(I_{\mathrm{SSP}}-I_{\mathrm{REF2}}\right)\right)/C_{\mathrm{tot}}, & \text{mid-voltage region,}\\ \left(I_{\mathrm{SSPN}}+I_{\mathrm{REF1}}-I_{\mathrm{M18}}\right)/C_{\mathrm{tot}}, & \text{high-voltage region,}\end{cases} \tag{8}$$

where

$$\begin{cases}K_1=\dfrac{(W/L)_{\mathrm{M22}}(W/L)_{\mathrm{M28}}}{(W/L)_{\mathrm{M21}}(W/L)_{\mathrm{M27}}},\\ K_2=\dfrac{(W/L)_{\mathrm{M24}}(W/L)_{\mathrm{M23}}}{(W/L)_{\mathrm{M26}}(W/L)_{\mathrm{M25}}},\\ C_{\mathrm{tot}}\approx\left(g_{\mathrm{m40}}+g_{\mathrm{m41}}\right)\left(r_{\mathrm{o40}}\,\|r_{\mathrm{o41}}\right)\left(C_1+C_2\right)+\left(C_{\mathrm{GS(M40)}}+C_{\mathrm{GS(M41)}}\right),\end{cases} \tag{9}$$

where C_1 and C_2 are the Miller capacitors, and $C_{\mathrm{GS(M40)}}$ and $C_{\mathrm{GS(M41)}}$ are the parasitic capacitors between the gate and the source of M40 and M41. As mentioned above, the proposed slew rate enhancement is not active in small-signal operation. Consequently, the electrical characteristics and the power dissipation of the whole circuit cannot be affected.

2.4. Circuit design

As shown in Fig. 3, a rail-to-rail operational amplifier, which contains bias circuits (M5–M8, I_{REF1}–I_{REF6}), complementary differential input stage (M1–M4), current summation (M9–M16), frequency compensation stage (R_1, R_2, C_1, C_2), and class AB output stage (M29–M38), is proposed. The folded-cascode current summation is used as the active load of the rail-to-rail differential pair to obtain a large gain and a low value of systematic offset voltage. For high driving speeds, two push-pull output stages (M40 and M41) are also introduced. Hence, the total dc gain of the circuit in Fig. 3 can be expressed as:

$$\begin{cases}A_{\mathrm{dc}}=A_{\mathrm{dc1}}A_{\mathrm{dc2}},\\ A_{\mathrm{dc1}}=g_{\mathrm{m(equal)}}R_{\mathrm{OUT1}},\\ R_{\mathrm{OUT1}}=\left(g_{\mathrm{m12}}r_{\mathrm{o12}}\left(r_{\mathrm{o10}}\,\|r_{\mathrm{oN}}\right)\right)\|\left(g_{\mathrm{m13}}r_{\mathrm{o13}}\left(r_{\mathrm{o15}}\,\|r_{\mathrm{oP}}\right)\right),\\ A_{\mathrm{dc2}}=\left(g_{\mathrm{m40}}+g_{\mathrm{m41}}\right)R_{\mathrm{OUT2}},\\ R_{\mathrm{OUT2}}=r_{\mathrm{o40}}\,\|r_{\mathrm{o41}},\end{cases} \tag{10}$$

where A_{dc1} and A_{dc2} are the dc gain of the input and the output stage, $g_{\mathrm{m(equal)}}$ is the equivalent g_{m} of the input stage, g_{m12}, g_{m13}, g_{m40} and g_{m41} are the g_{m} of M12, M13, M40 and M41. In addition, R_{OUT1} and R_{OUT2} are the output resistors of the input and the output stage, and r_{o10}, r_{o12}, r_{o13}, r_{o15}, r_{o40} and r_{o41} are the output resistors of M10, M12, M13, M15, M40 and M41. r_{oP} and r_{oN} are the output resistors of the PMOS and NMOS input pairs.

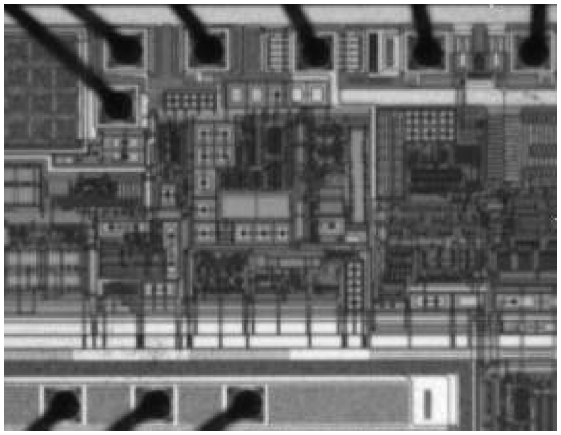

Fig. 4. Microphotograph of the proposed operational amplifier.

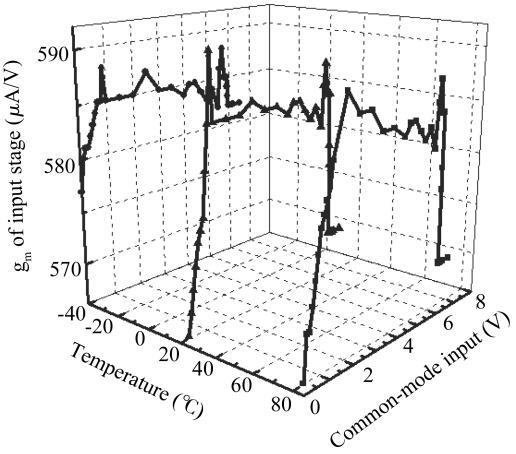

Fig. 5. Simulated g_m of input stage with a Zener-diode structure.

3. Simulation and experimental results

3.1. Layout design and entire circuit simulation results

The operational amplifier circuit is fabricated in the 0.5 μm CMOS process. The layout of the circuit is shown in Fig. 4. The circuit area is 400×275 μm^2.

Based on the 0.5 μm CMOS process, the circuit is simulated using H-Spice. Powered by an 8 V supply, adjusting the supply voltage from 0 to 8 V, the simulated g_m of the input stage is plotted in Fig. 5, when the temperature is at −40, 25 and 85 °C. The curve is flat over a wide range of input voltages from 0 to 8 V with a drift of about 24.5 μA/V. A dramatic change happens when supply voltage is below 2 V or exceeds 6 V. This is due to the variation of the current through the weak inversion transistors and the finite output resistance. It can be seen that the maximum g_m fluctuation is 4.2% over the input common mode range, which is beneficial to the power-efficient frequency compensation of the operational amplifier.

Figure 6 demonstrates the transient response to an 8 V step input when the temperature is at −40, 25 and 85 °C. Here, a supply voltage of 8 V is applied and a 10 kΩ load resistor is in series with a 20 pF load capacitor. The slew rate is up to 101 V/μs and 102 V/μs for the rising and falling edges, which verifies that the slew rate enhancement circuit makes the operational amplifier have a good transient response to a large-signal input.

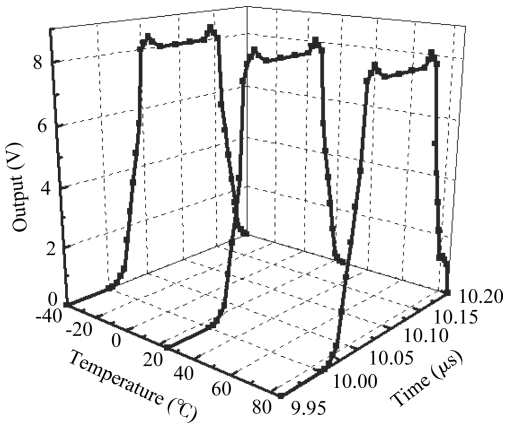

Fig. 6. Simulated step response of the compact operational amplifier.

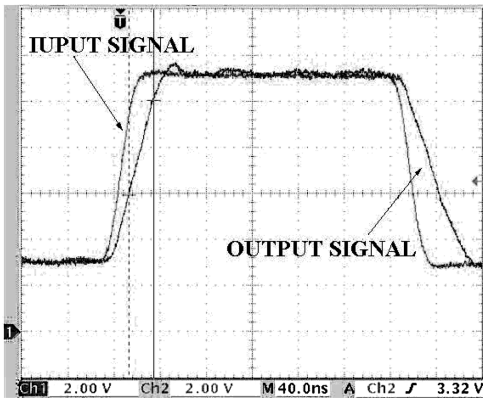

Fig. 7. Measured result of the large signal response.

3.2. Testing results

To test and verify the function of the slew rate enhancement of the chip, the large-signal response is tested, in which a 10 kΩ load resistor is in series with a 20 pF load capacitor. The testing conditions are V_{DD} = 8 V and the operation amplifier is in a buffer configuration. In Fig. 7, the input signal is an 8 V step input, whose rising and falling time is 50 ns. The result shows that the slew rate of the circuit has been improved with the slew rate enhancement, and the slew rate is 111 and 102 V/μs for the rising and falling edges. Moreover, the circuit has a setting time of 72 and 78 ns for the rising and falling edges. In addition, the circuit is in a buffer configuration, powered by an 8 V supply, and the rail-to-rail input/output characteristic is shown in Fig. 8, which demonstrates the good performance of the dynamic input/output range. Table 1 summarizes the operational amplifier specifications obtained from simulation and measurement, and makes a comparison with published ones. All of the results listed in the table are chip test results and show that the structure in this work shows a better performance than those previously reported with respect to high dc gain, large unity gain bandwidth, large output swing, and significantly high slew rate.

4. Conclusion

Based on an analysis of the operational amplifier, a constant-g_m rail-to-rail operational amplifier with a high slew

Table 1. Comparison of electrical characteristics of the proposed operational amplifier with reference ones.

Parameter	Ref. [4]	Ref. [6]	Ref. [7]	Ref. [10]	This work	
					Simulated	Measured
Power supply (V)	1.5	3.3	1.8	2.7–6	5–8	5–8
Quiescent current (mA)	0.34	1.63	1.97	0.215	1.2	1.05
$\Delta g_{m(max)}(\%)$	±0.35	—	4	8	4.9	4.2
Input offset (mV)	—	4	—	3	0.088	0.074
Output swing (V)	—	—	$V_{SS} - V_{DD}$	V_{SS} + 0.1 to V_{DD} − 0.1	V_{SS} + 0.077 to V_{DD} − 0.071	V_{SS} + 0.065 to V_{DD} − 0.068
Low frequency gain (dB)	89	80	100	85	101	109
Phase margin (°)	54	73	47	80	71	70
Unity gain bandwidth (MHz)	1.2	2	100	1.9	18	18.6
(SR^+/SR^-) (V/μs)	5/ − 5	35/ − 35	22.5/ − 46	8/ − 8	106/ − 101	111/−102
Setting time (rise/fall) (ns)	—	60/60	114.5/114.5	300/300	74/76	72/78
CMRR (dB)	80	—	147	80	92	96
R_L (kΩ)	1	—	—	0.01	10	10
C_L (pF)	—	20	15	10	20	20

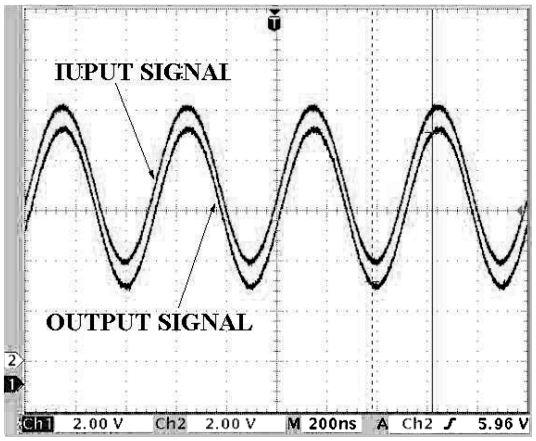

Fig. 8. Measured result of rail-to-rail input/output characteristic.

rate is designed. The principle of operation has been presented. The performance improvement is proven and verified by the simulation and experimental results. The design and outcomes introduced in this paper can be applied in other LCD-TFT driver ICs.

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