A novel precision curvature-compensated bandgap reference

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Abstract: A high precision high-order curvature-compensated bandgap reference compatible with the standard CMOS process, which uses a compensation proportional to $V_{\rm T}\ln T$ realized by utilizing voltage to current converters and the voltage current characteristics of a base–emitter junction, is presented. Experiment results of the proposed bandgap reference implemented with the CSMC 0.5-μm CMOS process demonstrate that a temperature coefficient of 3.9 ppm/°C is realized at 3.6 V power supply, a power supply rejection ratio of 72 dB is achieved, and the line regulation is better than 0.304 mV/V dissipating a maximum supply current of 42 μA.

Key words: high-order curvature compensation; CMOS bandgap reference; temperature coefficient; PSRR
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1. Introduction

Precision bandgap references are necessarily in great demand for many applications ranging from purely analog, mixed-mode to purely digital circuits, such as A/D converters, DRAMS, power converters and flash memory controlling circuits, for their high accuracy and temperature independence[1−3]. The reference voltage is required to be stable over the supply voltage and temperature variations, and also to be implemented without modification of the fabrication process[1].

A traditional bandgap reference circuit is first-order temperature compensated. It is a weighted sum of negative TC voltage $V_{\rm BE}$, and positive TC voltage $V_{\rm T}$ which is the thermal voltage kT/q. With regard to the nonlinearity of the voltage $V_{\rm BE}$, the TC of first-order temperature compensated references is always limited between 20 and 100 ppm/°C[3−6]. In order to overcome this limitation, many high-order temperature compensation approaches have been developed, such as the quadratic temperature compensation proposed by Song *et al.*[7], the exponential temperature compensation developed by Lee *et al.*[3], the piecewise linear curvature correction presented by Rincon-Mora *et al.*[4, 8], and the temperature dependent resistor ratio with a high resistive poly resistor and a diffusion resistor proposed by Leung *et al.*[2]. Although the temperature stability of bandgap references has been improved with these techniques, it increases the requirements of precise matching of the current mirror, pre-regulated supply voltage, or high resistive resistance.

In order to avoid the application range limit of the Taylor series expansion used in traditional theory explanations for temperature compensation, the proposed compensation will use the expression of $V_{\rm BE}$ directly. Utilizing voltage to current converters and the voltage current characteristics of a base–emitter junction to realize a compensation item approximately proportional to $V_{\rm T}\ln T$, a high-order curvature-compensated CMOS bandgap reference is presented in this paper. It eliminates the impact of the resistance temperature coefficient on the circuit by using resistance ratios.

2. Proposed curvature compensation method

The relationship between collector current and base–emitter voltage $V_{\rm EB}$ of pnp BJTs, which are biased in the forward active region, can be expressed as[5, 9]

$$V_{\rm EB}(T) = V_{\rm G0} - mV_{\rm T} - (\eta - \alpha)V_{\rm T}\ln T, \tag{1}$$

where m is a temperature-independent constant, α is the order of the temperature dependence of the collector current, $V_{\rm T}$ is the thermal voltage, and $V_{\rm G0}$ is the bandgap voltage of silicon extrapolated to 0 K. $\eta = 4 - n$; η is always between 3 and 4 with the most representative value being 3.45[10]. The $V_{\rm T}\ln T$ term demonstrates the high-order nonlinearity of $V_{\rm EB}$. As a result, a high-order compensated bandgap reference cannot be achieved by conversional linear compensation only.

A schematic of the proposed curvature compensated bandgap reference is shown in Fig. 1. All the resistances are made of the same material. The proposed bandgap reference can be divided into six parts, as shown in Fig. 1. For convenience of description, the TC of the resistances is ignored temporarily, and the influence of the resistance temperature coefficient on the bandgap reference will be considered at the end of the analysis.

The V–I module shown in Fig. 1 is used to convert voltage signal into relevant current signal, and a schematic of it with bias current source $I_{\rm bias}$ and output stage P1, P2 is shown in Fig. 2. To bias the transistors N1 and N2 in the active region, and make the transistors N1 and N2 have the same W/L ratio, the source voltages of transistors N1 and N2 acquire the same voltage. With regard to Kirchhoff's voltage law, and given $(W/L)_{\rm P2} = X(W/L)_{\rm P1}$, the output current $I_{\rm out}$ can be given by

$$I_{\rm out} = X\frac{V_{\rm DC}}{R}. \tag{2}$$

2.1. Startup circuit

Transistor MS is biased in the triode region acting as a large resistance. When the enable signal EN changes to high voltage,

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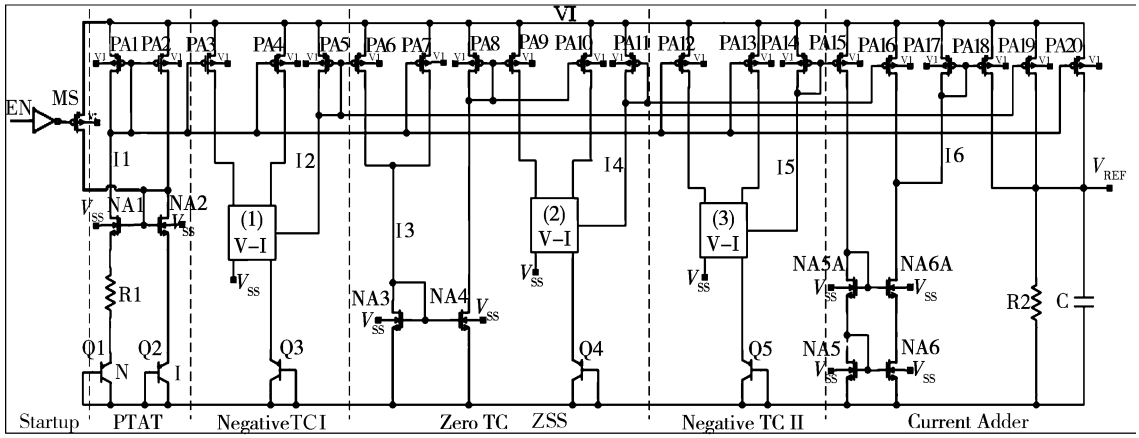

Fig. 1. Schematic of the proposed bandgap reference.

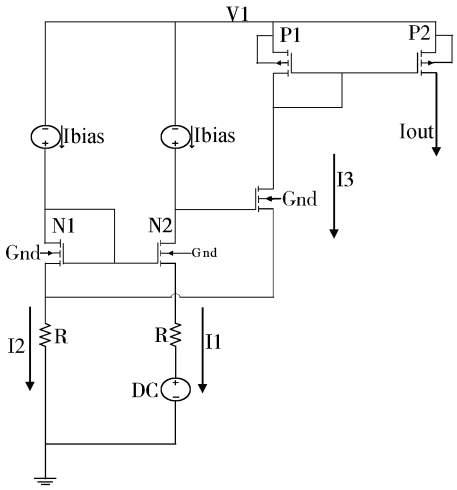

Fig. 2. Schematic of the V–I module.

MS turns on and injects a little current into the drain of transistor NA2 in order to drive the PTAT current source towards the desired stable state.

2.2. Proportional to absolute temperature (PTAT) current source

Given that transistors PA1 and PA2 have the same W/L ratio, and NA1 and NA2 have the same W/L ratio, according to Kirchhoff's voltage law and the voltage current characteristic of base–emitter junction, the current $I_{\mathrm{D\ (MPA1)}}$ can be given by

$$I_{\mathrm{D\ (MPA1)}} = I_{\mathrm{R_1}} = \frac{V_{\mathrm{T}} \ln N}{R_1}. \tag{3}$$

Because the thermal voltage V_{T} is proportional to absolute temperature, the TC of current $I_{\mathrm{D\ (MPA1)}}$ is constant.

2.3. Negative TC current source I

Given that the resistance used in module V–I (1) is R_3, $(W/L)_{\mathrm{PA3,\,PA4}} = A(W/L)_{\mathrm{PA1}}$, and $X = 1$, combining Eqs. (1) and (2), the current of transistor PA5 can be expressed as

$$I_2 = \frac{V_{\mathrm{G0}} - mV_{\mathrm{T}} - (\eta - \alpha)V_{\mathrm{T}} \ln T}{R_3}. \tag{4}$$

Because of the negative TC of V_{EB}, the TC of current I_2 is negative.

2.4. Zero TC current source

Given that $(W/L)_{\mathrm{PA6}} = B(W/L)_{\mathrm{PA5}}$, and $(W/L)_{\mathrm{PA7}} = C(W/L)_{\mathrm{PA1}}$, the current of transistor NA3 can be written as

$$I_3 = B\frac{V_{\mathrm{G0}} - mV_{\mathrm{T}} - (\eta - \alpha)V_{\mathrm{T}} \ln T}{R_2} + C\frac{V_{\mathrm{T}} \ln N}{R_1}. \tag{5}$$

The current I_3 can realize zero TC at some temperatures by properly choosing the parameters B, C, N, R_1 and R_2, whose theory is the same as that of a traditional bandgap voltage circuit. Given that the resistance used in module V–I (2) is R_4, $(W/L)_{\mathrm{NA4}} = D(W/L)_{\mathrm{NA3}}$, $(W/L)_{\mathrm{PA9,\,PA10}} = E(W/L)_{\mathrm{PA8}}$, and $X = 1$, combining Eqs. (2) and (5), the current of transistor PA11 can be generated as

$$I_4 = \frac{V_{\mathrm{T}}}{R_4} \ln\left[DE\left(B\frac{V_{\mathrm{G0}} - mV_{\mathrm{T}} - (\eta - \alpha)V_{\mathrm{T}} \ln T}{R_3} + \frac{V_{\mathrm{T}} \ln N}{R_1}\right)/I_{\mathrm{S4}}\right]. \tag{6}$$

2.5. Negative TC current source II

Given that the resistance used in module $V-I$ (3) is R_5, $R_5 = FR_4$, $(W/L)_{\mathrm{PA12,\,PA13}} = G(W/L)_{\mathrm{PA1}}$, and $X = 1$, combining the voltage current characteristic of the base–emitter junction with Eq. (2), the current of transistor PA14 can be given by

$$I_5 = \frac{V_{\mathrm{T}} \ln\left(G\frac{V_{\mathrm{T}} \ln N}{R_1}/I_{\mathrm{S5}}\right)}{FR_4}. \tag{7}$$

Because of the negative TC of V_{EB}, the TC of current I_5 is negative.

2.6. Current adder

Given that $(W/L)_{\mathrm{PA15}} = H(W/L)_{\mathrm{PA14}}$, $(W/L)_{\mathrm{PA16}} = J(W/L)_{\mathrm{PA11}}$, $(W/L)_{\mathrm{PA18}} = L(W/L)_{\mathrm{PA17}}$, $(W/L)_{\mathrm{PA19}} = M(W/L)_{\mathrm{PA5}}$, $(W/L)_{\mathrm{NA6}} = (W/L)_{\mathrm{NA6A}} = K(W/L)_{\mathrm{NA5}} = K(W/L)_{\mathrm{NA5A}}$, $(W/L)_{\mathrm{PA20}} = N(W/L)_{\mathrm{PA1}}$, and the emitter area of transistor Q5 is P times larger than that of transistor Q4, with regard to Kirchhoff's current law, and letting

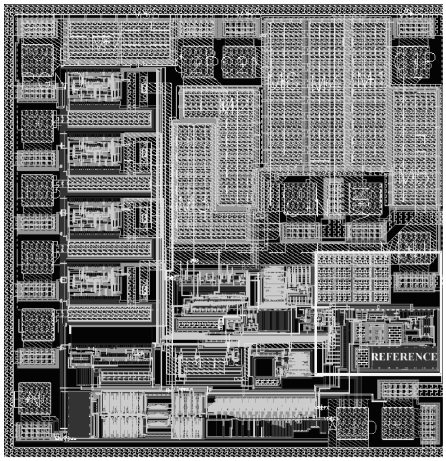

Fig. 3. Layout of the proposed bandgap reference used in a DC–DC converter.

$KH/F = J = S_1$, $BDEP/G = S_2$ and $CP/G = S_3$, the current I_6 is generated as

$$I_6 = \frac{S_1}{R_4} V_{\mathrm{T}} \times \ln \frac{V_{\mathrm{T}} \ln N}{S_2 \dfrac{R_1}{R_3}(V_{\mathrm{G0}} + mV_{\mathrm{T}} - V_{\mathrm{T}}(\eta - \alpha)\ln T) + S_3 V_{\mathrm{T}} \ln N}. \quad (8)$$

From Eq. (8), it can be noticed that the denominator of the logarithm item can realize first-order curvature compensation by properly selecting the parameters S_2, S_3, N, and the ratio of R_1 and R_3. In this way, the current I_6 can be regarded as a current approximately proportional to $V_{\mathrm{T}} \ln T$.

Using Kirchhoff's current law with transistors PA18, PA19, PA20, resistance R_2, and combining Eqs. (3), (4), and (8) yields

$$V_{\mathrm{REF}} = \frac{Y_1 R_2}{R_4} V_{\mathrm{T}} \times \ln \frac{V_{\mathrm{T}} \ln N}{S_2 \dfrac{R_1}{R_3}(V_{\mathrm{G0}} + mV_{\mathrm{T}} - V_{\mathrm{T}}(\eta - \alpha)\ln T) + S_3 V_{\mathrm{T}} \ln N} + \frac{Y_3 R_2}{R_1} V_{\mathrm{T}} \ln N + \frac{Y_2 R_2}{R_3}[V_{\mathrm{G0}} - mV_{\mathrm{T}} - (\eta - \alpha) V_{\mathrm{T}} \ln T], \quad (9)$$

where Y_1, Y_2 and Y_3 are modulation coefficients. If the parameters in Eq. (9) are properly adjusted, the item $Y_3 V_{\mathrm{T}} \ln N(\mathrm{R}_2/R_1)$ can be eliminated with the item $-Y_2 V_{\mathrm{T}} m(R_2/R_3)$, and the first item can be eliminated with the item $-(\eta - \alpha) V_{\mathrm{T}} \ln T Y_2(R_2/R_3)$ at some temperatures. Thereby, the high-order curvature-compensated bandgap reference circuit is realized, and the TC of the output voltage is zero at some temperatures. The capacitance is used to filter some disturbance signals, and stabilize the bandgap reference output voltage.

The above-mentioned analysis does not consider the impact of the resistance temperature coefficient on the bandgap reference circuit. Equation (9) indicates that all the resistances used in the circuit appear in the form of resistances ratios. Therefore, the temperature coefficient of the resistances has no influence on the reference output voltage by using the same type of resistances. As there are no requirements for the exact value of resistances and device size, except the ratios, the technology will have no impact on the ratios, and the proposed reference can work stably when the parameters are decided by some form of technology.

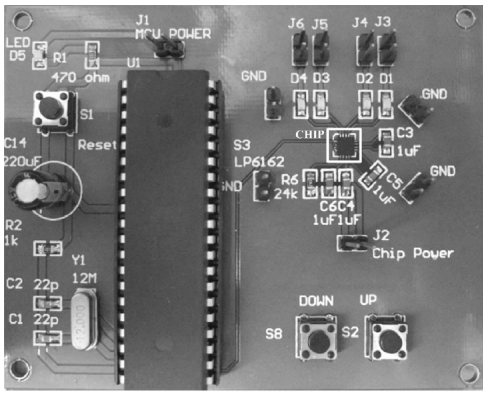

Fig. 4. Photograph of test board.

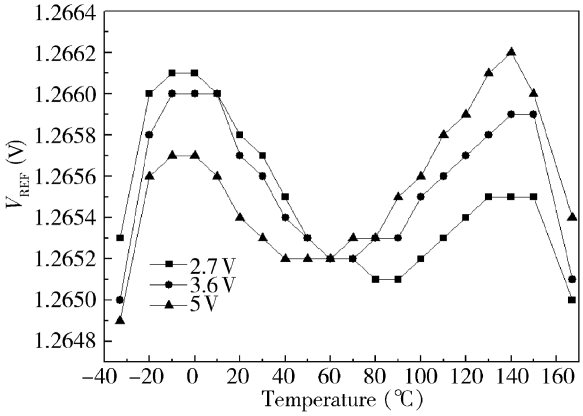

Fig. 5. Measured temperature dependence of the proposed bandgap voltage reference.

3. Experimental results and discussion

The proposed bandgap reference shown in Fig. 1 has been implemented in CSMC 0.5-μm CMOS technology with a minimum emitter size of 5×5 $\mu\mathrm{m}^2$. A 10×10 $\mu\mathrm{m}^2$ p–n–p transistor, which is 4 times as large as the minimum transistor, was used as a unit transistor to increase matching properties. The threshold voltage of this technology is about $V_{\mathrm{THN}} \approx 0.70$ V, $|V_{\mathrm{THP}}| \approx 0.95$ V at 0 °C. The layout of the proposed bandgap reference used in a DC–DC converter is shown in Fig. 3. The reference is placed in the white frame. A photograph of the test board used in the measurement is shown in Fig. 4. The chip is placed in the white frame on the right-hand side of the board. The temperature dependence of the reference voltage for different supply voltage values is illustrated in Fig. 5. The output voltage V_{REF} of the proposed bandgap reference has a deviation of 0.078% with temperature ranging from –33 to 167 °C at 3.6 V power supply. The temperature coefficient is 3.9 ppm/°C at 3.6 V and the maximum temperature coefficient is 5.1 ppm/°C with power supply ranging from 2.7 to 5 V.

Table 1. Summary of the performance of the proposed bandgap voltage reference.

Reference	Proposed	Song *et al.*[7]	Lee *et al.* [3]	Rincon-Mora *et al.* [8]	Leung *et al.* [2]
Technology	CSMC 0.5 μm CMOS	CMOS	BiCMOS	BiCMOS	CMOS
Supply voltage (V)	2.7 | 3 | 5	$\pm$5	5	1.1 (min)	2 | 3 | 4
Supply current (μA)	42 (max)	1200	74	15 (min)	23 (max)
VREF (V)	1.2655 $\pm$ 0.0007	1.192	1.264	0.595	1.142 $\pm$ 0.00285
TC (ppm/°)C	4.3 | 3.9 | 5.1	25.6	8.9	$<$ 20	5.3 | 6.1 | 2.6
Line regulation (mV/V)	0.174 @ –33 °C, 0.174 @ 30 °C, 0.043 @ 70 °C, 0.304 @ 167 °C	—	—	408 ppm/V	$\pm$1.25 @ 0 °C, $\pm$1.43 @ 27 °C, $\pm$1.35 @ 100 °C
PSRR (dB)	–72 @ 10 Hz, –63 @ 1 kHz, –54 @ 10 kHz	–55	–73	—	–47 @ 10 Hz –20 @ 1 kHz –10 @ 10 MHz
Chip area (mm^2)	0.073	2.258	0.044	0.223	0.057

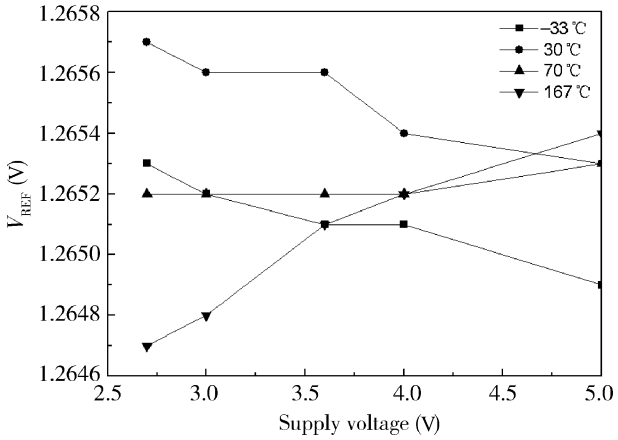

Fig. 6. Measured supply voltage dependence of the proposed bandgap voltage reference under different temperatures.

The measured supply dependence at −33, 30, 70, and 167 °C is shown in Fig. 6. The output voltage deviation of the proposed bandgap reference is within 0.7 mV when the power supply voltage changes from 2.7 to 5 V, and the line regulation is less than 0.304 mV/V in the temperature range from –33 to 167 °C.

Table 1 summarizes a brief comparison of the results of the proposed bandgap reference and other voltage references reported in the literature to show the improvements of the proposed structure.

4. Conclusion

Based on the expression of V_{EB} directly avoiding the application range limit of the Taylor series expansion, a high precision high-order curvature compensated CMOS bandgap voltage reference has been proposed and implemented with CSMC 0.5-μm CMOS technology. Utilizing a compensation item proportional to $V_T \ln T$ to compensate the high-order TC of V_{EB}, a high-order curvature-compensated CMOS bandgap voltage reference dissipating a maximum supply current of 42 μA is presented by artful use of simple circuit structures. With the improvement mentioned above, the temperature coefficient of the proposed circuit is 3.9 ppm/°C over a temperature range of –33 to 165 °C at 3.6 V power supply. The output reference voltage achieves 72 dB PSRR with 3.6 V power supply at room temperature, and exhibits a line regulation of better than 0.304 mV/V. Although the proposed circuit is realized with the standard CMOS process in this paper, this novel curvature-correcting scheme can be used in almost any process technology yielding reliable temperature compensation. The additional circuitry required for this correction is compact and is easily implemented. The architecture also lends itself to versatile trimming procedures. The proposed bandgap reference is well suited for many mixed-signal systems because of its high precision and high performance.

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