A quasi-3-dimensional simulation method for a high-voltage level-shifting circuit structure*

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Abstract: A new quasi-three-dimensional (quasi-3D) numeric simulation method for a high-voltage level-shifting circuit structure is proposed. The performances of the 3D structure are analyzed by combining some 2D device structures; the 2D devices are in two planes perpendicular to each other and to the surface of the semiconductor. In comparison with Davinci, the full 3D device simulation tool, the quasi-3D simulation method can give results for the potential and current distribution of the 3D high-voltage level-shifting circuit structure with appropriate accuracy and the total CPU time for simulation is significantly reduced. The quasi-3D simulation technique can be used in many cases with advantages such as saving computing time, making no demands on the high-end computer terminals, and being easy to operate.

Key words: quasi-3D; 3D; device simulation; high-voltage level-shifting
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1. Introduction

A conventional half-bridge driver requires a high-voltage level-shifting circuit to transmit the drive signal from the low-voltage control logic circuit to the floating high-side gate driver. Figure 1(a) shows a typical connection of the high voltage integrated circuit (HVIC) and the MOSFET half bridge. The high-side and low-side gate drivers supply the gate drive signals for the power MOSFETs: M1 and M2. The high-voltage MOSFETs, HVM1 and HVM2 together have the function of level-shifting, transmitting the on-signal and off-signal through R1 and R2 from the control logic circuit to the high-side gate driver. The control logic circuit and high-side gate driver are all made by low voltage devices with power supply voltages of V_{CC} and V_{DD} respectively. However, the former takes the ground as reference, whereas the latter takes the "TUB", marked as terminal "O" in the figure, as reference, which has a floating voltage V_o with respect to the ground. Further explanation on the structure and operation of the high-voltage level-shifting circuit can be found in Refs. [1, 2].

Figure 1(b) shows a local top view of a structure made on a semiconductor substrate of the high-voltage level-shifting circuit enclosed by the dashed lines of Fig. 1(a) except for the two wires connected with the two terminals of R2. In this study, the structure of the high-voltage level-shifting circuit is the same as that in Ref. [3]. The structure consists of three parts: HVM1, the high-voltage junction terminal (HVJT) region of the TUB, and the isolation region between the HVJT and HVM1. Here, the drift region of HVM1 and the HVJT uses the RESURF technique, and the isolation region is the p-sub region. Figure 1(c) shows the local 3D structure of the high-voltage level-shifting circuit, which is the region enclosed by dashed lines in Fig. 1(b).

There are two problems that must be considered in Fig. 1(c). (1) The isolation region must be able to endure the voltage differences between HVJT and HVM1 anywhere along the z-direction. (2) The currents from HVM1 to R1 should be limited in the area marked HVM1. Problem 1 has been solved successfully and several approaches have been proposed[1−9]. However, problem 2 needs three-dimensional (3D) simulation tools to confirm whether the current for transmitting the logic signal is limited in the right regions of the structure.

Full 3D-simulations are impractical because they would require long computation time and utilize high-end workstations and even supercomputers. For high-voltage integrated circuits in particular, 3D simulation needs a lot of nodes in the mesh of the structure to get accurate results. The maximum number of nodes in 3D simulation tools is normally limited, e.g., the maximum number of nodes available in Davinci is 60 000[10]. So a complex high-voltage structure cannot be totally simulated and therefore the results may be inaccurate. In order to solve the 3D simulation problem, some quasi-3D simulation methods are proposed for the key regions of the specific structures[11−15].

In this paper, a new quasi-3D simulation technique is proposed by using the circuit analysis advanced application module (CA-AAM) of the 2D device simulation software MEDICI and applied to the high-voltage level-shifting circuit structure. Firstly, the numerical technique of the quasi-3D simulation method is described. Then, the high-voltage level-shifting

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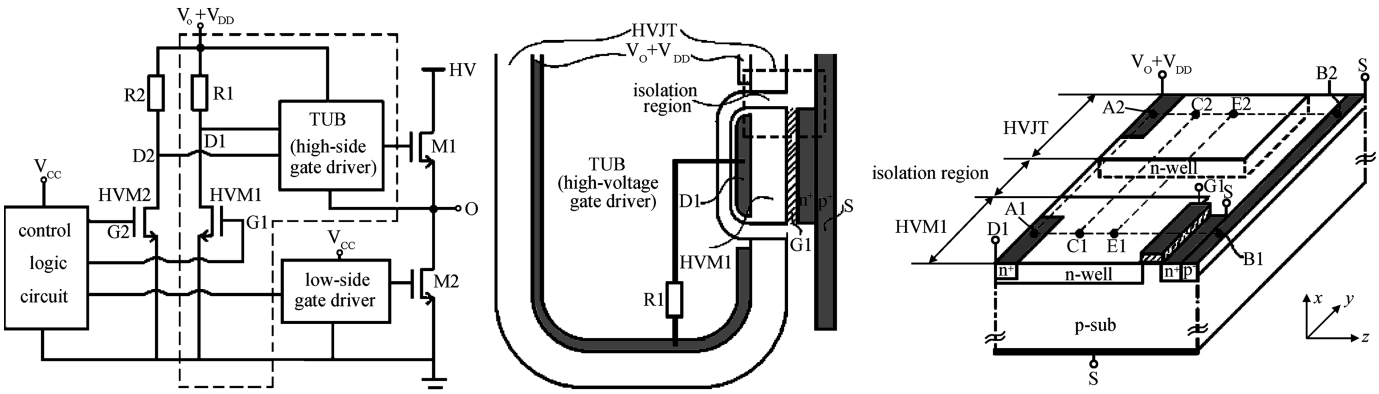
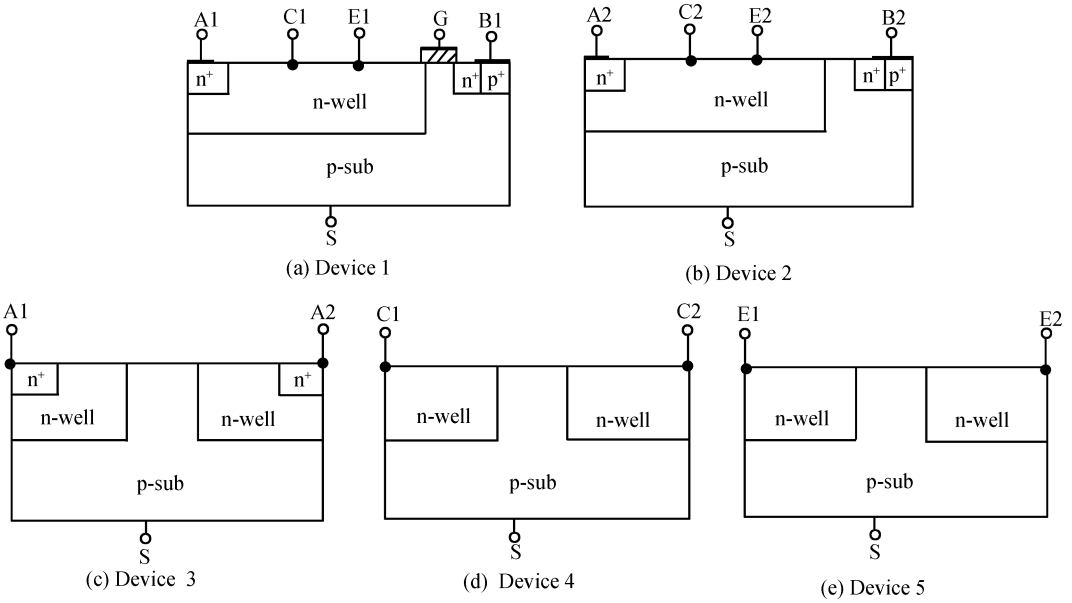


(a) Circuit structure (b) Local top view (c) Local 3D structure

Fig. 1. Structure of the high-voltage level-shifting circuit, where x, y and z are the coordinates used.



(a) Device 1 (b) Device 2

(c) Device 3 (d) Device 4 (e) Device 5

Fig. 2. Models of 2D devices of each region.

circuit is simulated by the quasi-3D simulation method. Finally, the results are compared with those using the full 3D simulator Davinci.

2. Numerical technique

In order to study the behavior of the currents of the high-voltage level-shifting circuit, a new quasi-3D analysis technique is proposed. The new quasi-3D simulation technique is carried out by combining 2D devices having cross-sections perpendicular to the z-axis and 2D devices having cross-sections perpendicular to the y-axis, where the axes are shown in Fig. 1(c), using CA-AAM of MEDICI[10].

First, the 3D structure of Fig. 1(c) is taken to be many 2D device structures. Two dashed lines, A_1B_1 and A_2B_2, parallel to coordinate z, and three dashed lines, A_1A_2, C_1C_2 and E_1E_2, parallel to coordinate y, are used to form five 2D devices, device 1, device 2, etc., shown in Fig. 2.

Device 1 is a 2D model of HVM1 shown in Fig. 1(c), where electrodes A_1 and B_1 are the drain D_1 and source S of HVM1 respectively. The mesh nodes C_1 and E_1 are defined as two electrodes in the mesh file for the quasi-3D simulation.

Device 2 is a 2D model of HVJT region shown in Fig. 1(c), where electrodes A_2 and B_2 are the cathode V_O+V_{DD} and anode S of the HVJT region. The mesh nodes C_2 and E_2 are defined as two electrodes in the mesh file for the quasi-3D simulation.

Device 3 is a 2D model of the region between A_1 and A_2 shown in Fig. 1(c), where the mesh nodes A_1 and A_2 are defined as two electrodes in the mesh file for the quasi-3D simulation.

Device 4 is a 2D model of the region between C_1 and C_2 shown in Fig. 1(c), where the mesh nodes C_1 and C_2 are defined as two electrodes in the mesh file for the quasi-3D simulation.

Device 5 is a 2D model of the region between E_1 and E_2 shown in Fig. 1(c), where the mesh nodes E_1 and E_2 are defined as two electrodes in the mesh file for the quasi-3D simulation.

The potentials of electrodes B_1, B_2 and S in Fig. 2 are connected to the ground.

Next, all of the 2D devices stated above are connected through CA-AAM of MEDICI, and the electrodes which have

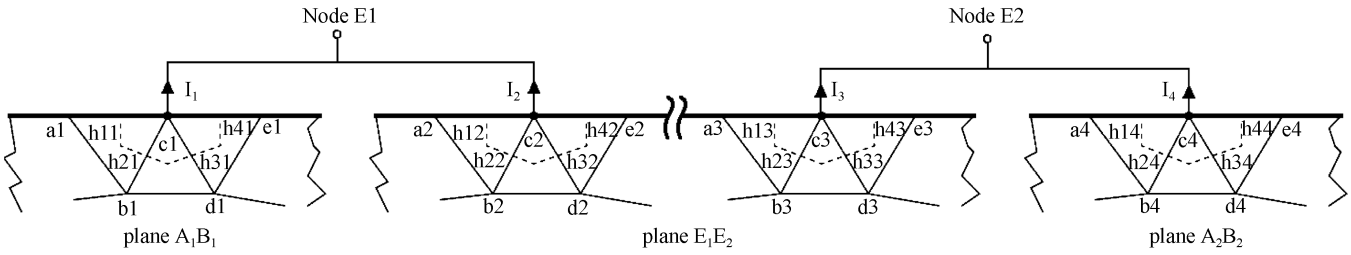


Fig. 3. Device to device connections.

the same names are connected together as a circuit node. The framework of the level-shifting structure for the quasi-3D simulation is then completed. In the same way, the framework of the high-voltage level-shifting circuit can have more 2D cross-sections perpendicular to the z-axis and the y-axis.

Finally, Kirchhoff's equations describing the circuit and the semiconductor equations describing the devices are solved as a coupled set, and 3D characters of the structure can be obtained. The device equations include Poisson's equation, equations of continuity and of current density. Using Kirchhoff's current law, equations are written at circuit nodes and are illustrated in the example shown in Fig. 3[16].

Circuit node E_1 is connected at one point of plane through A_1B_1 and at another point of plane through E_1E_2. Similarly, E_2 is with both the plane through A_2B_2 and the plane through E_1E_2. The current equations of node E_1 and E_2 are simply:

$$I_1 + I_2 = 0, \tag{1}$$

$$I_3 + I_4 = 0. \tag{2}$$

Obviously,

$$I_1 = J_{a1c1}h_{11} + J_{b1c1}h_{21} + J_{c1d1}h_{31} + J_{c1e1}h_{41}, \tag{3}$$

$$I_2 = J_{a2c2}h_{12} + J_{b2c2}h_{22} + J_{c2d2}h_{32} + J_{c2e2}h_{42}, \tag{4}$$

$$I_3 = J_{a3c3}h_{13} + J_{b3c3}h_{23} + J_{c3d3}h_{33} + J_{c3e3}h_{43}, \tag{5}$$

$$I_4 = J_{a4c4}h_{14} + J_{b4c4}h_{24} + J_{c4d4}h_{34} + J_{c4e4}h_{44}, \tag{6}$$

where terms J_x in Eqs. (3)–(6) are the current densities flowing out of the semiconductor surface，the subscript "x" refers to the two nodes of the indicated mesh lines in Fig. 3. Generally speaking, each J_x is the sum of the electron, hole, and displacement current densities and it in turn depends upon the potential, electron, and hole concentrations, the electron and hole carrier temperatures, and the lattice temperature at each of the circuit nodes. Therefore, current J_x depends upon device variables at device nodes a_x, b_x, c_x, d_x, and e_x. The dotted lines in Fig. 3 represent edges of volumes which are formed by bisectors of the sides of the triangles. These volumes are for the integration surrounding the electrode[16].

Thus, each common circuit node is due to a connection between two 2D devices, and they are perpendicular each to other. Also, the potential and current distribution at the circuit nodes can be decided together by these pairs of 2D devices. On the other hand, the potential and current distributions of the 2D devices are affected in turn by the common circuit nodes.

The basic numerical technique used is to write the circuit equation as well as the device equations as a coupled set and solve them with Newton-Raphson's method, and then the potential and current of the 3D structure can be obtained.

Before starting the quasi-3D simulation, it is important that every 2D device structure in Fig. 1(c) should first be analyzed by 2D device simulation, because convergence of a circuit containing several devices is usually as good as convergence of a single device[16].

3. Simulation results of the high-voltage level-shifting circuit structure

A simulation of the structure of the high-voltage level-shifting circuit shown in Fig. 1(c) with a breakdown voltage of 200 V of HVM1 has been done. The parameters of this structure are as follows: the doping concentration of the p-sub region is 2×10^{14} cm^{-3}; the doping concentration of the n-well layer is 2×10^{15} cm^{-3}; the n-well layer junction depth is 5 μm; the drift region length is 20 μm. Some numerical results of the distributions of the potentials along the dashed line A_1B_1, V_1, and along the dashed line A_2B_2, V_2, for different cases are shown in Fig. 6–9, both by the quasi-3D method and by Davinci.

Since the voltage difference between electrode D_1 of HVM1 and electrode $V_O + V_{DD}$ of HVJT is small under typical operation of the high-voltage level-shifting circuit, results for two cases are given in Fig. 5–8, namely, (a) $V_{D1} = V_O + V_{DD}$ = 100 V, and (b) V_{D1} = 100 V, $V_O + V_{DD}$ = 110 V. The gate to source voltages V_{GS} of HVM1 are all 6 V.

Due to the fact that the critical sizes of the structure in Fig. 1(c) are d_1, which is the width of the n^+ drain region and also the gate width of HVM1; d_2, which is the distance from the edge of the n^+ drain region of HVM1 to the isolation region; d_3, which is the width of the isolation region; d_4, which is the distance from the edge of the n^+ region of the HVJT to the isolation region; d_5, which is the width of the n^+ region of the HVJT, results for different values of such d are given in Fig. 4–7.

In Fig. 4, the values of d are $d_1 = 4$ μm, $d_2 = 2$ μm, $d_3 = 5$ μm, $d_4 = 2$ μm, $d_5 = 4$ μm. It can be seen that the values of V_1 from either the quasi-3D or Davinci are the same. This is also true for the values of V_2. In Fig. 4(a), the results of currents of the 2D devices perpendicular to the z-axis for different planes with z = 0 μm, 4 μm, 7 μm, 10 μm, 13 μm and 18 μm are

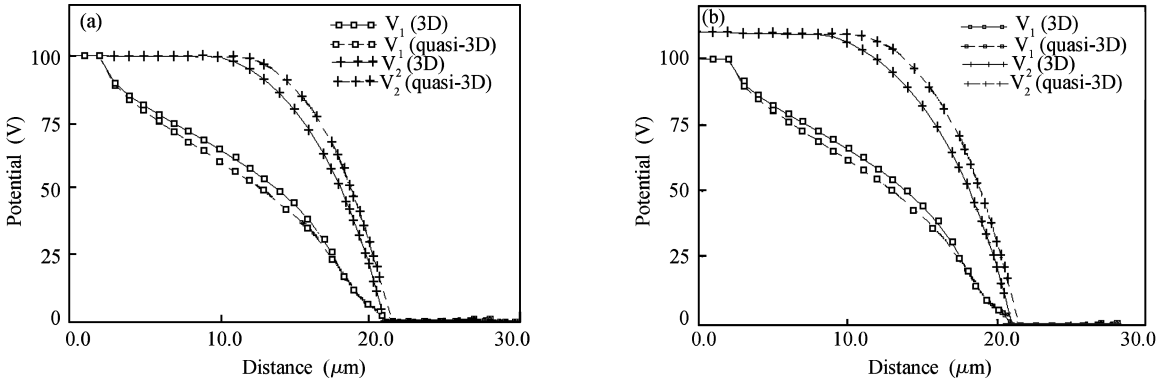


Fig. 4. Potential distributions of V_1 and V_2 by 3D and quasi-3D simulation when $d_1 = 4$ μm, $d_2 = 2$ μm, $d_3 = 5$ μm, $d_4 = 2$ μm, $d_5 = 4$ μm and $V_{GS} = 6$ V. (a) $V_{D1} = V_O + V_{DD} = 100$ V; (b) $V_{D1} = 100$ V, $V_O + V_{DD} = 110$ V.

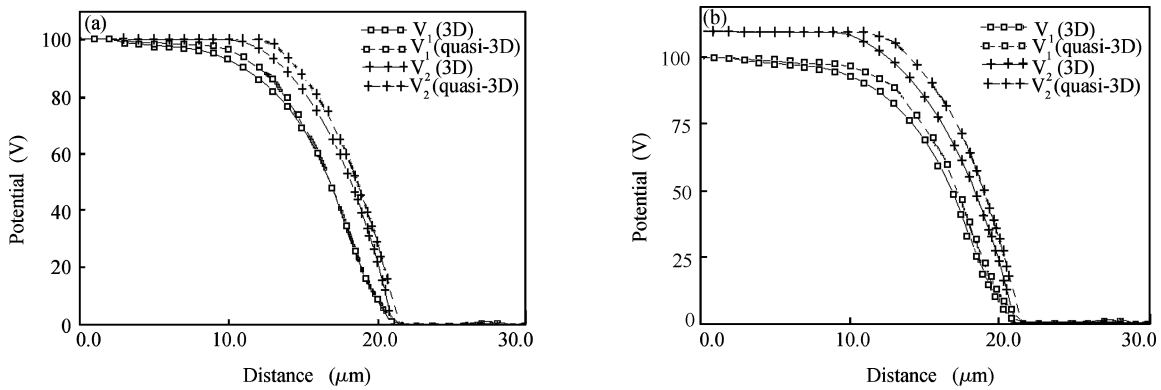


Fig. 5. Potential distributions of V_1 and V_2 by 3D and quasi-3D simulation when $d_1 = 4$ μm, $d_2 = 6$ μm, $d_3 = 5$ μm, $d_4 = 6$ μm, $d_5 = 4$ μm and $V_{GS} = 6$ V. (a) $V_{D1} = V_O + V_{DD} = 100$ V; (b) $V_{D1} = 100$V, $V_O + V_{DD} = 110$ V.

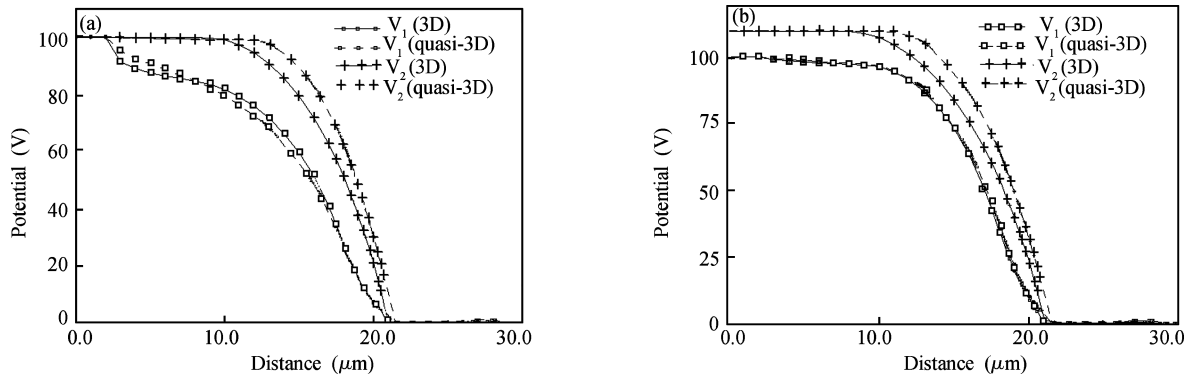


Fig. 6. Potential distributions of V_1 and V_2 by 3D and quasi-3D simulation when $d_1 = 4$ μm, $d_2 = 16$ μm, $d_3 = 5$ μm, $d_4 = 16$ μm, $d_5 = 4$ μm and $V_{GS} = 6$ V. (a) $V_{D1} = V_O + V_{DD} = 100$ V; (b) $V_{D1} = 100$V, $V_O + V_{DD} = 110$ V.

1.2234×10^{-11} A, 1.6567×10^{-11} A, 1.0632×10^{-5} A, 1.1733×10^{-5} A, 5.0131×10^{-6} A, and 2.5071×10^{-6} A respectively, where $z = 0$ is on a plane through point A in Fig. 1(c). The total current from HVM1 to the HVJT is 2.9885×10^{-5} A by the quasi-3D and 3.3466×10^{-5} A by Davinci. In Fig. 4(b), the result of the current of the 2D devices perpendicular to z-axis are 2.8878×10^{-6} A, 3.5791×10^{-6} A, 1.0167×10^{-5} A, 1.3791×10^{-5} A, 8.5610×10^{-6} A and 5.1951×10^{-6} A respectively, and the total current from HVM1 to the HVJT is 4.4181×10^{-5} A by quasi-3D and 4.530×10^{-5} A by Davinci.

Of course, the current with the values of d used for Fig. 4 cannot be ignored. Such a significant current is due to the distances between the electrodes being too small and therefore punch-through between the electrodes occurs. In order to see the influence of the distances between the electrode contact regions of the high voltage side and the isolation region, changes to values of d_2 and d_4 are made from the value 2 μm of Fig. 4 to 6 μm and 16 μm. The results are shown in Figs. 5 and 6, respectively. The results of current from HVM1 to the HVJT are both less than 1 nA and negligible. In addition, the results of changing the width of the isolation region, d_3, of 5 μm of Fig. 6 to 10 μm are shown in Fig. 7. The same conclusions can be obtained as from Fig. 5.

Note that in Fig. 4–7 only the potential distributions of V_1 and V_2 are presented. Actually, simulations of 10 2D devices have been done for the results. The 10 devices include four 2D devices perpendicular to the y-axis, namely, one through the line A_1B_1, another through the line A_1B_1, and still two others

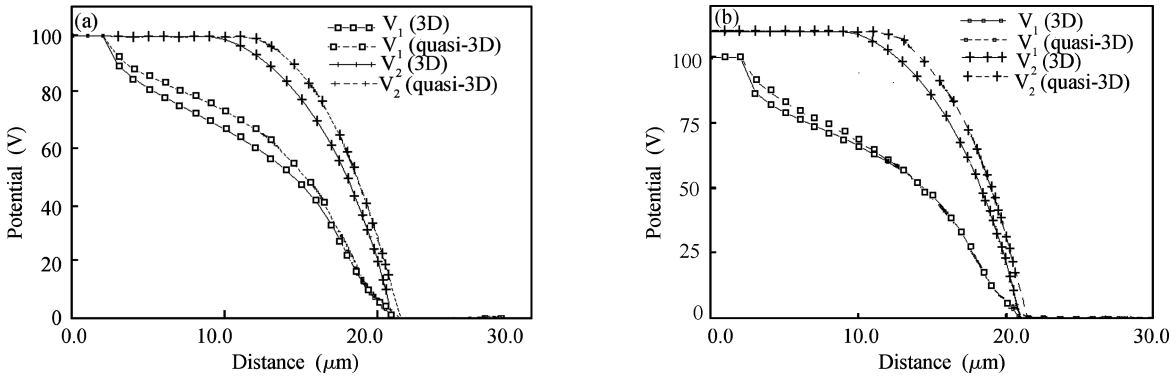


Fig. 7. Potential distributions of V_1 and V_2 by 3D and quasi-3D simulation when $d_1 = 4\ \mu$m, $d_2 = 6\ \mu$m, $d_3 = 10\ \mu$m, $d_4 = 6\ \mu$m, $d_5 = 4\ \mu$m, $V_{GS} = 6$ V. (a) $V_{D1} = V_O + V_{DD} = 100$ V; (b) $V_{D1} = 100$ V, $V_O + V_{DD} = 110$ V.

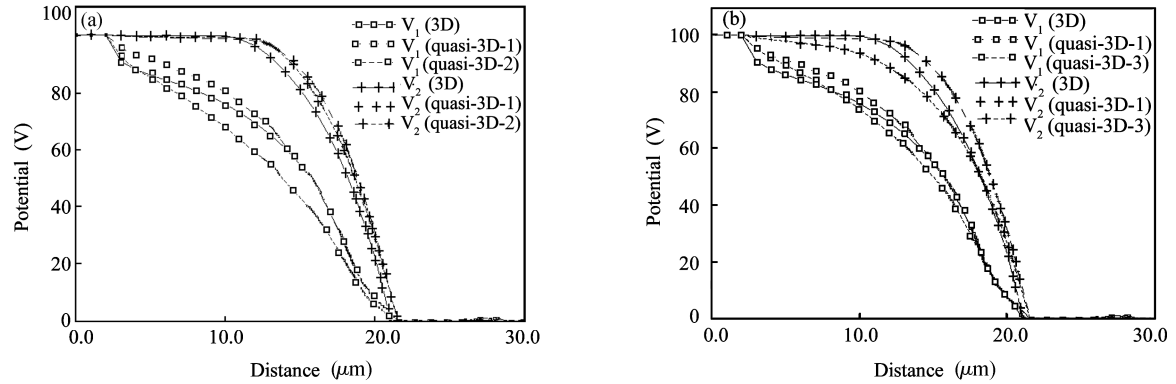


Fig. 8. Potential distributions of V_1 and V_2 by 3D and quasi-3D simulation when $d_1 = 4\ \mu$m, $d_2 = 6\ \mu$m, $d_3 = 10\ \mu$m, $d_4 = 6\ \mu$m, $d_5 = 4\ \mu$m, $V_{GS} = 6$ V and $V_{D1} = V_{D2} = 100$ V.

Table 1. Total CPU time and maximum values of voltage deviation by Davinci and the quasi-3D simulation under various conditions.

Case		Fig. 4	Fig. 5	Fig. 6	Fig. 7	Fig. 8	
						Quasi-3D-2	Quasi-3D-3
Total CPU time (min)	3D	135.81	154.81	152.14	165.81	160.09	160.09
	Quasi-3D	41.04	93.34	53.61	68.69	49.06	47.37
Max value of voltage deviation of the results of quasi-3D to 3D (V)		< 10	< 10	< 10	< 10	< 15	< 12

through two lines parallel to the line A_1B_1 and located close to the two edges of the isolation region but not in contact with the n^+-regions which are connected to the electrodes D_1 and $V_O + V_{DD}$. The 10 devices also include six 2D devices perpendicular to the z-axis, namely, one through the line A_1A_2, and the other five through five lines all parallel to the line A_1A_2 and passing both n-wells but without being in contact with the n^+-region.

In order to see the effect of the number of 2D devices on the results, the case of Fig. 7 is done again by using only four 2D devices perpendicular to the z-axis instead of six 2D devices. The results are shown with the mark "quasi-3D-2" in Fig. 8(a), where the results of Fig. 7 are shown with the mark "quasi-3D-1" for comparison. Further, the case of Fig. 7 is also done again by using only two 2D devices perpendicular to the y-axis instead of four 2D devices and the results are shown with the mark "quasi-3D-3" in Fig. 8(b).

From Fig. 8, it is verified that the greater number of 2D devices used, the more accurate the results can become.

Table 1 shows comparisons of the total CPU time by quasi-3D simulation and Davinci and the maximum values of voltage deviation of the results of quasi-3D to 3D for various cases. From the table, the total CPU time for simulation by quasi-3D is far less than that by the full 3D simulation Davinci.

4. Conclusions

In this paper, a new quasi-3D analysis technique has been proposed for the high-voltage level-shifting circuit. The quasi-3D simulation can be realized by many 2D devices with edges perpendicular to the semiconductor surface, where some of them have edges perpendicular to the edges of the remaining 2D devices, with the circuit analysis advanced application module of MEDICI. In comparison with the full 3D device simulation program, Davinci, the quasi-3D simulation method can give results for the potential and current distribution of the 3D high-voltage level-shifting circuit structure with appropriate accuracy and the total CPU time is significantly reduced.

The quasi-3D simulation method does not need a high-

end computer terminal and operates easily. It is expected that in addition to the structure of the high-voltage level-shifting circuit used in this paper, quasi-3D can also be used for other complex 3D structures.

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