An improved HCI degradation model for a VLSI MOSFET*

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Abstract: An improved hot carrier injection (HCI) degradation model was proposed based on interface trap generation and oxide charge injection theory. It was evident that the degradation behavior of electric parameters such as I_{dlin}, I_{dsat}, G_m and V_t fitted well with this model. Devices were prepared with 0.35 μm technology and different LDD processes. I_{dlin} and I_{dsat} after HCI stress were analyzed with the improved model. The effects of interface trap generation and oxide charge injection on device degradation were extracted, and the charge injection site could be obtained by this method. The work provides important information to device designers and process engineers.

Key words: HCI degradation model; interface traps; oxide charge
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1. Introduction

Hot carrier injection (HCI) is one of the most important reliability issues for modern MOSFET devices, especially in deep-submicron technology. As we all know, device characteristics such as linear drain current (I_{dlin}), saturated drain current (I_{dsat}), transconductance (G_m) and threshold voltage (V_t) shift after hot carrier injection. Traditionally, to evaluate the device degradation degree, a short time stress voltage was applied to the MOSFET and the time-dependant device degradation was plotted. Long term lifetime could be extrapolated using the degradation law[1, 2].

The power law (the Hu model, proposed by Hu in Berkeley University)[3] has been most widely used to obtain HCI lifetimes since the 1980s. It is popularly accepted nowadays by many IC foundries. Unfortunately, the power law could fit early degradation behavior well, but it could not characterize the saturation behavior after long time stress, which mostly observed in HCI degradation data. However, some other mixed laws which can cover this phenomenon were proposed in the literature[4, 5], but no single one could be regarded as a candidate for a traditional model to cover all technology.

In this paper, an improved HCI degradation model is proposed which can fit all degradation behavior along stress time for sub-micron device technology. This improved model is based on interface trap generation and oxide charge injection theory which occurs during the HCI process. The degradation data of electric characteristics fit well with this model. Fitting parameters are analyzed and process dependence is discussed in this paper. This model depicts the degradation of device characteristics exactly and provides an improved useful analyzed method in the reliability area.

2. Improved HCI degradation model

Impact ionization is created during HCI stress due to maximum channel transverse electric field at the drain side. According to the lucky electron model, some electrons obtain high energy and change advance path[6]. The re-directed electrons go toward the Si–SiO_2 interface, thus interface traps increase greatly and some electrons are injected into the oxide. A schematic diagram of the mechanism is shown in Fig. 1. This leads to mobility and saturated velocity decrease[7]. Therefore, device characteristic degradation is the synthesized effect of interface trap generation and oxide charge injection.

An improved HCI degradation model for sub-micron device technology, shown as Eq. (1), is proposed here based firstly on this theory.

$$\Delta y/y = \begin{cases} m_1 t^n + m_2 \ln t + m_3, & t \neq 0, \\ 0, & t = 0. \end{cases} \tag{1}$$

In this model, y is the device electric characteristic, t is the HCI stress time, n is the impact ionization coefficient, m_1 is the interface trap generation related parameter, m_2 is the ox-

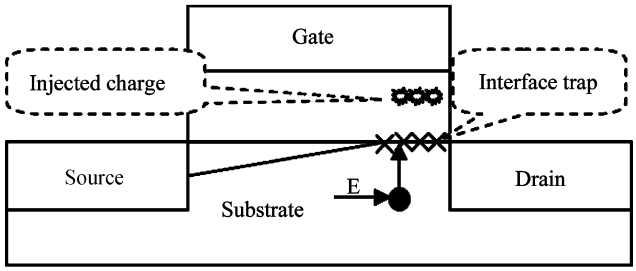

Fig. 1. Schematic diagram of HCI damage occurring in a device. Interface traps and injected charges are generated after HCI stress.

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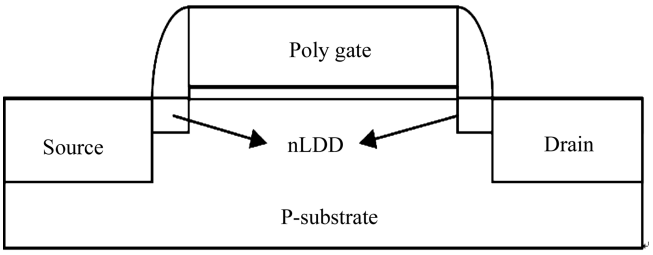

Fig. 2. Schematic diagram of the LDD nMOSFET prepared for the study.

ide charge injection related parameter, and m_3 is a constant.

Obviously, if $t \neq 0$, the model includes three parts. $m_1 t^n$ indicates the exponential device performance degradation with time. This part is the same as the traditional power law model which arises from the interface trap generation mechanism[7]. According to the oxide breakdown (time dependent dielectric breakdown, TDDB) model, the charges injected into the oxide are proportional to ln t [8]. So the second part of the model describes the degradation degree of device performance due to the oxide charge injection effect.

Compared to the traditional Hu model, this improved model includes the total device degradation process and makes it easy to analyze which the main factor during each HCI stress was. A detailed analysis will be discussed later in this paper. This method is more effective and helpful to device design and process improvement.

3. Experiment and data fitting

The devices used in this study were fabricated with a conventional LDD NMOS process of 0.35 μm technology. Channel length was 0.5 μm and width was 10 μm. The gate oxide thickness was 150 μm with a poly gate. A schematic diagram of the device prepared here is shown in Fig. 2. Two devices, A1 and A2, were prepared and HCI stress was applied for 13000 s. The procedure of HCI testing is described in detail in the JEDEC standards. The drain stress voltage ($V_{\rm dstr}$) is set to 5 V. The gate stress voltage ($V_{\rm gstr}$) is determined by sweeping $V_{\rm g}$ to find a $V_{\rm g}$ at the peak substrate current ($I_{\rm sub}$) ($I_{\rm submax}$ method) with a fixed $V_{\rm dstr}$ = 5 V. $I_{\rm dlin}$, $I_{\rm dsat}$, $G_{\rm m}$, and $V_{\rm t}$ were monitored during tests. These electric characteristics were measured with an Agilent 4156C and a Cascade S300 probe station.

Figure 3 shows the device's electric characteristic degradation with stress time. The data were plotted on a log–log scale plot as is traditional and were fitted with this improved model. According to the literature, in the traditional power law model, n is 0.5–0.75 for sub-micron devices[7]. Here, the impact ionization coefficient n was fixed at 0.5. It was obvious that the improved model fitted the test data perfectly for all these four electrical characters, even when the data tended to saturate during long test times as shown in the $I_{\rm din}$, $G_{\rm m}$ and $V_{\rm t}$ degradation plots. Table 1 lists the fitting parameter values of m_1, m_2 and m_3.

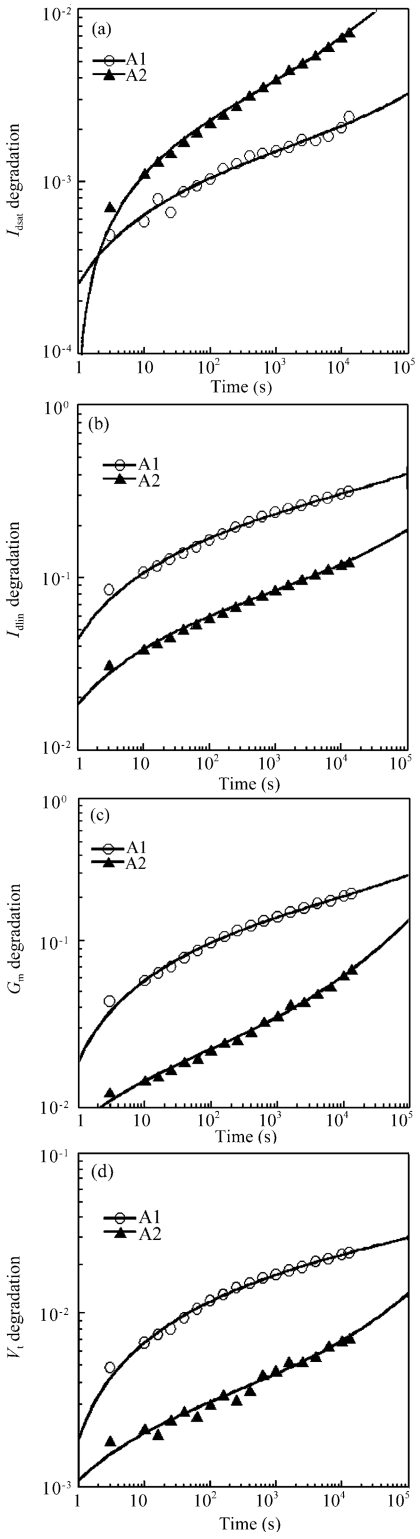

Fig. 3. Electrical parameter degradation data fitted with the improved model: (a) $I_{\rm dsat}$; (b) $I_{\rm dlin}$; (c) $G_{\rm m}$; (d) $V_{\rm t}$.

The fitting accuracy can be denoted by the correlation coefficient (R) whose definition is expressed as Eq. (2). Here, $X_{\rm i}$ is the calculated value, $\overline{X}$ is the mean of calculated values, $Y_{\rm i}$ is the tested value, and $\overline{Y}$ is the mean of tested values. It is obviously that the closer the value is to 1, the better the fit of the curve. As shown in Table 2, all the correlation coefficient values of the two devices were above 0.9. This means that the improved model fit the test data perfectly and could reveal the

Table 1. Fitting parameters of I_{dsat}, I_{dlin}, G_m and V_t.

Device	Fitting parameter	I_{dsat}	I_{dlin}	G_m	V_t
A1	m_1	3.397×10^{-6}	0.0001497	0.000124	2.627×10^{-6}
	m_2	0.000165	0.0271	0.01686	0.002097
	m_3	0.0002519	0.0442	0.01871	0.001903
A2	m_1	3.047×10^{-5}	0.0002341	0.0003133	2.282×10^{-5}
	m_2	0.0004191	0.008558	0.002536	0.0003857
	m_3	4.09×10^{-5}	0.01808	0.007611	0.001079

Table 2. Correlation coefficient of fitting the two devices with the improved model.

Device	A1	A2
I_{dsat}	0.9885	0.9994
I_{dlin}	0.9982	0.9991
G_m	0.9989	0.9984
V_t	0.9986	0.9914

reality of the device's physical behavior during HCI stress.

$$R=\frac{\sum_i (X_i-\overline{X})(Y_i-\overline{Y})}{\sqrt{\sum_i (X_i-\overline{X})^2}\sqrt{\sum_i (Y_i-\overline{Y})^2}}. \quad (2)$$

4. I_{dsat} and I_{dlin} degradation analyzed by the improved model

As mentioned above, the improved model includes two factors: interface trap generation and oxide charge injection. So the parameters m_1 and m_2 in the model revealed the proportion of the effect of the two mechanisms. We prepared five devices using 0.35 μm technology as above, named A, B, C, D and E, with 0.5 μm gate length, 10 μm gate width and 150 Å oxide thickness. HCI stress for 10000 s was applied under the condition of 5 V V_{dstr} by the I_{submax} method. The degradation data of I_{dlin}, I_{dsat} were tested and fitted with the improved model. The fitting parameter m_1 and m_2 values were extracted.

As shown in Fig. 4, for both m_1 and m_2, the value of I_{dlin} is 10 times larger than that of I_{dsat}. It is easy to understand that I_{dlin} describes all the degradation zone along the channel while I_{dsat} screens part of the damage in the pinch off area at the drain region. A schematic diagram is shown in Fig. 5. Otherwise, from Fig. 4, the m_1 value of I_{dlin} and I_{dsat} displays the same tendency, while the m_2 value shows a big difference. This can be explained by the fact that the degree of interface trap generation along the channel is consistent for these five devices and the main location is near the drain region.

The effect of oxide charge injection is more local than that of interface traps. As shown in Fig. 4(b), the m_2 value of I_{dlin} is almost the same between the five devices. This reveals the same degradation degree due to oxide charge injection of the five devices. The vibration of the m_2 value of I_{dsat} shows

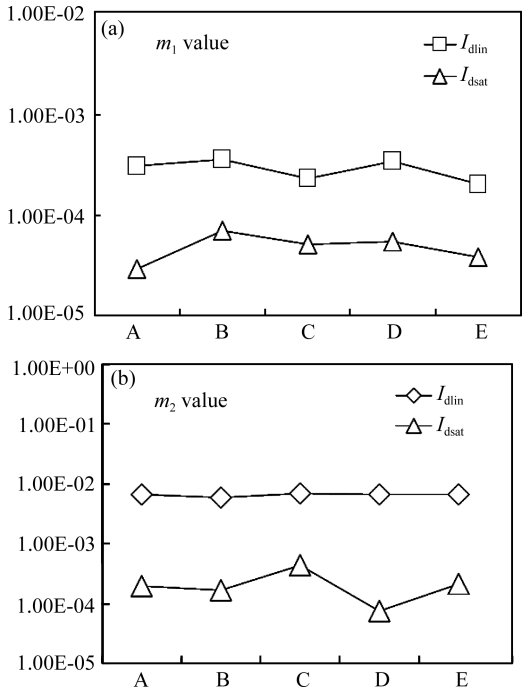

Fig. 4. m_1 and m_2 comparison of I_{dlin} and I_{dsat}: (a) m_1 value; (b) m_2 value.

that the injection location was different. The damage site of device C was nearer the channel center than the other devices while device D was nearest to the drain region. This phenomenon can be explained with Fig. 5; maximum channel transverse electric field occurred at the drain side. A hot electron went toward the Si/SiO_2 interface, and generated interface traps. Some of these electrons with high enough energies to mount the interface barrier could inject into the oxide. Therefore, the damage is local.

5. Effect of the process on improved model parameters

To study the effect of the LDD process on the two HCI degradation mechanisms, three devices named a, b, c were prepared with 0.35 μm technology and different LDD dosages. The dosage is: $a < b < c$. Channel length and width is 0.5 μm and 10 μm respectively. HCI stress was applied to these three devices for 10000 s with V_{dstr} of 5.5 V, and m_1, m_2 were extracted by the improved model for I_{dlin} and I_{dsat}.

Figure 6 shows the m_1 and m_2 parameters extracted from I_{dlin} and I_{dsat} of these three devices. It is obvious that for I_{dlin},

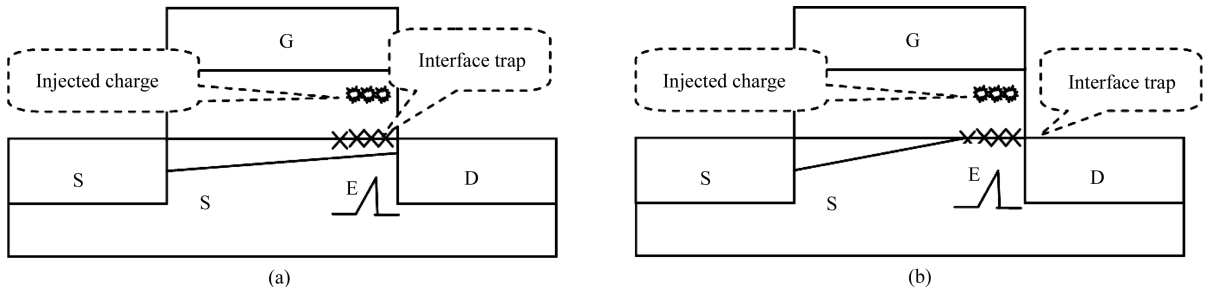

Fig. 5. Schematic diagram of the monitored area of I_{dlin} and I_{dsat} in the channel: (a) I_{dsat} monitored part of the damage, while the others were screened by the pinch off zone; (b) I_{dlin} monitored the whole damage in the channel.

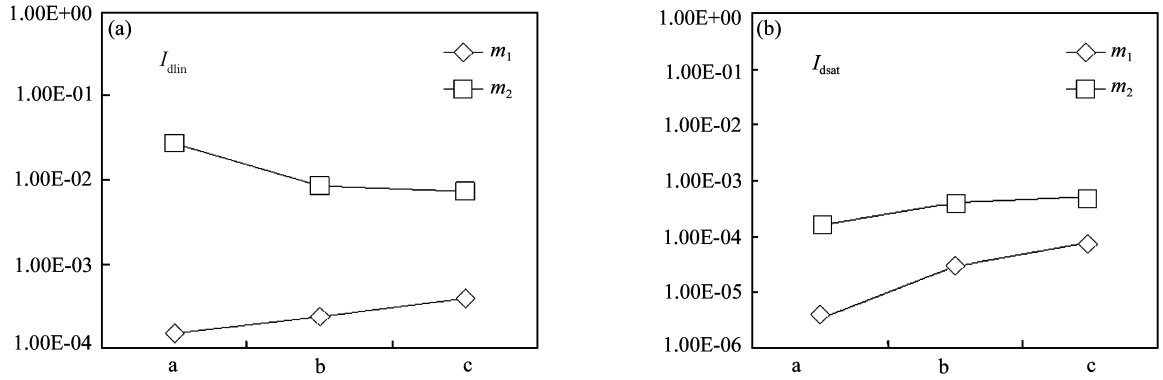

Fig. 6. m_1 and m_2 parameters with different LDD dosages: (a) I_{dlin}; (b) I_{dsat}.

the m_1 value increased with dosage while m_2 decreased. For I_{dsat}, both m_1 and m_2 increased. According to HCI degradation theory, impact ionization occurs at the maximum channel electric field. As the LDD dosage increases, the maximum electric field position would be driven to the channel. Therefore, the oxide charge injection site is also pushed to near the channel center. Here, the increased m_1 of both I_{dlin} and I_{dsat} means that the degree of interface trap generation was severe for the high LDD dosage device due to the position of maximum electric field near to the channel center. On the other hand, part of the oxide charge injection is screened by the pinch off area when device is operated at saturation state. Therefore, m_2 of I_{dsat} increased as shown in Fig. 6(b) because most of the damage resulting from oxide charge injection was screened for the high LDD dosage device. This is consistent with HCI theory.

6. Conclusion

An improved HCI degradation model for a VLSI MOSFET has been proposed in this paper. It reveals the physical nature of HCI degradation clearer than other methods. This improved model was developed built on interface trap generation and oxide charge injection theory. It fits HCI stress data accurately for I_{dlin}, I_{dsat}, G_m, and V_t, and lets us observe the degradation of device characteristics resulting from HCI stress directly. This method offers a convenient method to analyze the HCI degradation mechanism and provides important information to process engineers and device designers.

References

[1] JEDEC standard, foundry process qualification guidelines, JP001.01. JEDEC Solid State Technology Association, 2002

[2] JEDEC standard, procedure for measuring N-channel MOSFET hot carrier induced degradation under DC stress, JESD-28A. JEDEC Solid State Technology Association, 2001

[3] Hu C M, Lee P M, Ko P K. Relating CMOS inverter lifetime to DC hot-carrier lifetime in nMOSFETs. IEEE Electron Device Lett, 1990, 11(1): 39

[4] Chan V H, Chung J E. Two-stage hot carrier degradation and its impact on sub-micrometer LDD NMOSFET lifetime prediction. IEEE Trans Electron Devices, 1995, 42: 957

[5] Marchand B, Ghibaudo G, Balestra F, et al. An improved hot carrier degradation law for MOSFET lifetime prediction. Microelectron Reliab, 1998, 38(6–8): 1103

[6] Tam S, Ko P K, Hu C M. Lucky-electron model of channel hot-electron injection in MOSFET's. IEEE Trans Electron Devices, 1984, 31(9): 1116

[7] Hu C M, Tam S C, Hsu F C, et al. Hot-electron-induced MOSFET degradation-model, monitor, and improvement. IEEE J Solid-State Circuits, 1985, 20(1): 295

[8] Chen I C, Holland S E, Hu C M. Electrical breakdown in thin gate and tunneling oxide. IEEE Trans Electron Devices, 1985, 32(2): 413