A radiation-hardened-by-design technique for improving single-event transient tolerance of charge pumps in PLLs*

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Abstract: A radiation-hardened-by-design (RHBD) technique for phase-locked loops (PLLs) has been developed for single-event transient (SET) mitigation. By presenting a novel SET-resistant complementary current limiter (CCL) and implementing it between the charge pump (CP) and the loop filter (LPF), the PLL's single-event susceptibility is significantly decreased in the presence of SETs in CPs, whereas it has little impact on the loop parameters in the absence of SETs in CPs. Transistor-level simulation results show that the CCL circuit can significantly reduce the voltage perturbation on the input of the voltage-controlled oscillator (VCO) by up to 93.1% and reduce the recovery time of the PLL by up to 79.0%. Moreover, the CCL circuit can also accelerate the PLL recovery procedure from loss of lock due to phase or frequency shift, as well as a single-event strike.

Key words: charge pump; phase-locked loop; RHBD; single-event transient
DOI: 10.1088/1674-4926/30/12/125009 **EEACC:** 2570

1. Introduction

Radiation-induced single-event transient (SET) is caused by the strike of a single energetic particle. The energy deposited by a particle strike in a critical region of the device PN junction generates electron–hole pairs, which are transported and collected at the junction, resulting in undesirable circuit response. As technology feature sizes continue to decrease and operating frequencies increase, SETs come to dominate the radiation effects of mixed-signal integrated circuits (ICs) such as phase-locked loops (PLLs). Previous work has shown that a single particle striking in a PLL could deposit enough charge to change the PLL output significantly[1−5]. The charge pump (CP) is a critical module in PLLs, and is most sensitive to single-event transients[1−4]. Laser tests at Vanderbilt University have shown that the maximum number of erroneous (missing or additional) clock pulses in the output of the PLL due to strikes in CPs is at least one order of magnitude greater than that induced by strikes occurring in any other PLL module[2].

In recent years, various methods have been developed to mitigate SETs in CPs. Chung *et al.* demonstrated that a PLL with wider bandwidth settled and re-obtained lock faster from loss of lock due to SETs[4]. However, it is difficult to adjust the loop parameters to accurately cope with SETs in a single module of the PLL and it might have an impact on electrical performance, stability, noise and area. Alternatively, Loveless *et al.* replaced the vulnerable current-based charge pump with a SET-resistant tri-state voltage-switching charge pump and a low-pass filter (LPF)[3]. Then the PLL single-event susceptibility was considerably reduced, while simultaneously decreasing the lock-in time of the PLL. Nevertheless, the design of PLLs becomes more complex, as the charge pump and LPF should be re-designed and the loop parameters should be recalculated with the new expression. In addition, the unfixed CP current could result in an increased phase jitter and a nonlinear response in the acquisition period.

The purpose of this paper is to present a radiation-hardened-by-design (RHBD) technique applied to the charge pump for improving SET tolerance. Based on the SET failure mechanism, a novel SET-resistant complementary current limiter (CCL) is proposed and implemented to obtain a hardened PLL with little impact on the loop parameters in the absence of SETs in CPs. Then the circuit structure and the work mechanism of the CCL are discussed. Finally, the hardened effects of the CCL circuit are analyzed through transistor-level simulation. Compared with other hardened methods, this RHBD technique is easy to implement and has little impact on the PLL design and the design flow.

2. Single-event transients in charge pumps for phase-locked loops

2.1. General PLL circuit topology description

The main function of PLL is to generate a clock signal with a specific frequency. The general charge pump PLL (GPLL) investigated in this research, as shown in Fig. 1, consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), and a voltage-controlled oscillator (VCO).

* Project supported by the National Natural Science Foundation of China (Nos. 60836004, 60676010), the PhD Program of Ministry of Education of China (No. 20079998015), and the Program for Changjiang Scholars and Innovative Research Team in University of China.
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Received 8 June 2009, revised manuscript received 8 July 2009

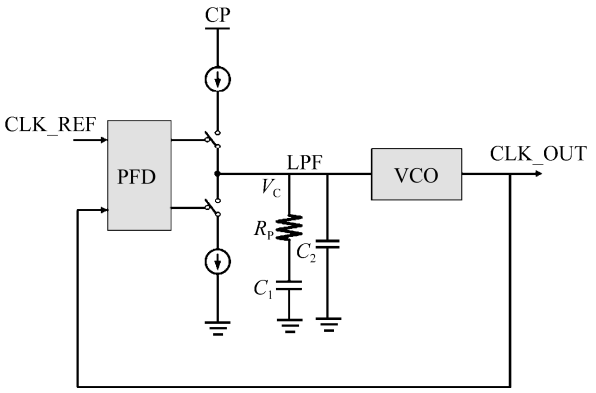

Fig. 1. Block diagram of the general charge pump PLL (GPLL).

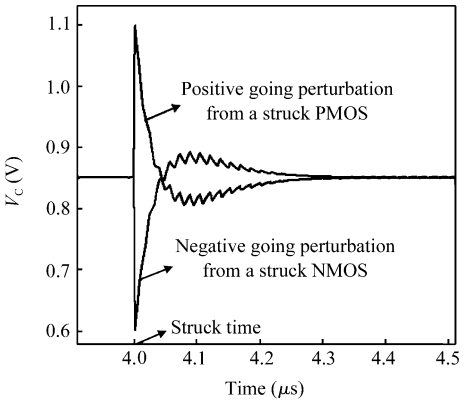

Fig. 2. V_C versus time for 1 GHz operation. Single-event strikes occur in the CP at 4 μs and span approximately 967 ns.

The output of the VCO is compared with the reference clock in PFD, and the tri-state phase detector generates an error signal. Then the charge pump converts the error signal pulses into analog current pulses which are integrated and converted to a control voltage value through the passive loop filter. Finally, this control voltage V_C drives the VCO to generate the output clock operating at a specific frequency.

2.2. Basic failure mechanisms of SETs in CPs

An instantaneous ion strike in the CP causes excess CP current, resulting in a large abrupt change of V_C to influence the whole loop. When the PLL system is in its in-lock condition, the current sources in the CP are in the "off" state and the sourcing or sinking current from CP to LPF is zero. A single-event strike in the last output switch (the most sensitive node) of the charge pump, which is also the input of LPF and VCO, may produce a fast positive-going (negative-going) current pulse from a struck PMOS (NMOS) on the LPF. For the fast current pulse, the current flows through the LPF resistance R_P, and the main LPF capacitor C_1, is effectively a short circuit. This creates a voltage drop across the resistance, which forms the peak V_C variation. When the current pulse ends, the current across the resistance becomes zero, and the loop filter voltage jumps to the capacitor voltage.

The voltage disturbance on the LPF can cause phase and frequency shift, signal distortion or even temporarily stop the output signal oscillation, resulting in the loss of PLL frequency lock. The PLL will eventually recover through loop feedback. For example, the whole change procedure of V_C is shown in Fig. 2, in which the last output switch of a CP was struck by a single particle at 4 μs, then V_C increased to the peak value and was ultimately restored to the final voltage after approximately 967 ns.

Single-event vulnerability of the charge pump strongly relies on two characteristics. One is that the excess current due to strikes in CPs is orders of magnitude greater than the CP current, which is induced by strikes occurring in any other PLL module and is limited by the current source transistors in the CP. The other is that the location hit by a particle is nearest to the LPF, which means SETs cannot be much dampened, eventually leading to the largest swing of V_C. It should be noted that the large excess current from the CP to the LPF is the critical mechanism. Therefore, this is an effective method to limit the excess current for mitigating the SET.

2.3. Modeling and analysis of SETs in CPs

As noted above, an instantaneous ion strike in the CP causes excess CP current, resulting in an abrupt change of V_C to influence the whole loop. Then V_C restores the final stable voltage after a recover procedure. Therefore, PLL behavior is obtained by observing VCO control voltage V_C, instead of phase error in this work. Based on the failure mechanism, a model for SET characterization had been built to investigate the effects of the SET current in CPs on PLL behaviors[6]. The transfer function[6] of control voltage $V_C(s)$, with respect to the single-event current $i(s)$, is derived as follows:

$$H(s) = \frac{V_C(s)}{i(s)} = \frac{\dfrac{1}{C_1}s(R_P C_1 s + 1)}{s^2 + \dfrac{I_P K_{VCO}}{2\pi C_1}R_P C_1 s + \dfrac{I_P K_{VCO}}{2\pi C_1}}$$

$$= \frac{\dfrac{1}{C_1}s(R_P C_1 s + 1)}{s^2 + 2\omega_n \zeta s + {\omega_n}^2}, \quad (1)$$

where I_P and K_{VCO} are the charge pump current and the VCO gain, respectively. The natural frequency ω_n and the damping ratio ζ, are

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}, \quad \zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_1 K_{VCO}}{2\pi}}. \quad (2)$$

Equation (1) reveals the frequency domain properties of V_C with respect to the SET current. It is clear that the stable gain of $H(s)$ is R_P, implying that low frequency SET currents will be more or less filtered out, whereas those with frequencies greater than the bandwidth will be amplified by R_P. Therefore, decreasing R_P can diminish the V_C disturbance to improve SET tolerance.

3. SET hardened PLL with proposed complementary current limiter

3.1. SET hardened PLL circuit topology description

Although decreasing the resistance R_P, can simply achieve an improvement in SET susceptibility, it will result

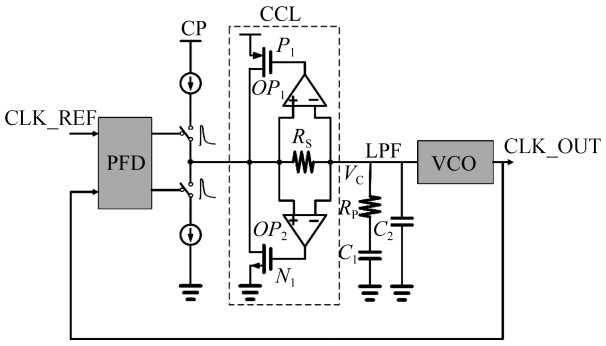

Fig. 3. SET hardened PLL (SHPLL) with proposed complementary current limiter.

in a decrease of the damping ratio ζ, to increase ringing and overshoot in the loop's transfer characteristics, thus leading to increased jitter and unstable PLL operation. An RHBD complementary current limiter (CCL) can be used to harden CP without reducing ζ. This CCL circuit is composed of a sensing resistance (R_S), a pair of complementary operational amplifiers (OP_1 and OP_2) and a pair of complementary SET current-limiting transistors (N_1 and P_1), as shown in Fig. 3. A SET hardened PLL (SHPLL) can be easily established by implementing a CCL circuit between the CP and the LPF.

In order to dampen SETs, the CCL circuit turns on the corresponding transistor (N_1 or P_1) to limit the excess current for compensating V_C after sensing the single-event current and activating the corresponding OP. To describe the PLL behavior clearly, the work mode of SHPLL in this research is classified into two types, the normal mode and the abnormal mode, depending on whether the SET current is greater than $2I_P$ ($2I_P$ is a margin to keep the CCL circuit from falsely switching.). Only the single-event occurring in the CP can drive the PLL into its abnormal mode. Therefore, the CCL is active only in the abnormal mode to reduce the gain of V_C, whereas it is inactive in the normal mode to keep the loop parameter unchanged. The PLL behaviors will be discussed in detail in the next two sections.

3.2. SET hardened PLL in the normal mode

The CCL circuit is inactive if the CP is not hit by a single-event strike or if the SET current is less than $2I_P$. Therefore, the CCL circuit should be only sensitive to the SET current, instead of the CP current. The DC offset voltages of the operational amplifiers are intended to be set as $\pm 2I_P R_S$. Thus a pair of operational amplifiers and a pair of current-limiting transistors remain in the "off" state in the normal mode. Compared with the original LPF of GPLL shown in Fig. 4(a), the only difference of the LPF of SHPLL in normal mode is the serial resistance R_S, as shown in Fig. 4(b). Since the CP can be taken as a current source with large inner impedance, if R_S is far enough below the impedance not to affect the fixed current I_P, the transfer function of the LPF in the normal mode will be the same as the original one. As a result, the CCL circuit has little influence on the PLL in the normal mode by choosing an appropriate R_S.

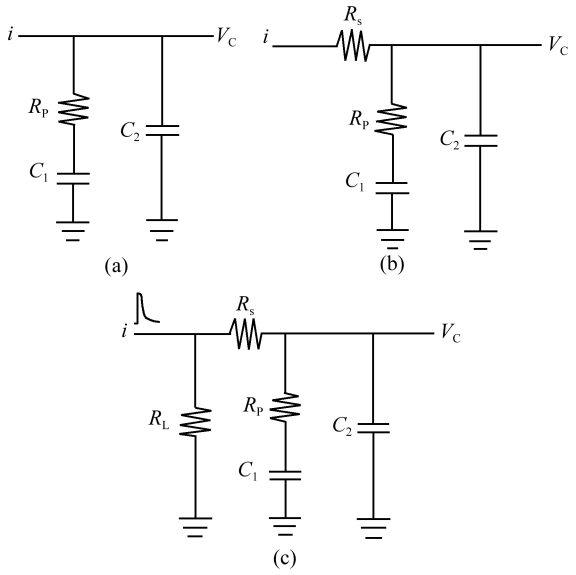

Fig. 4. (a) Original LPF structure of GPLL; (b) Equivalent LPF structure of SHPLL in the normal mode; (c) Equivalent LPF structure of SHPLL in the abnormal mode.

3.3. SET hardened PLL in the abnormal mode

When a single-event strike with an induced current greater than $2I_P$ occurs in CPs, the hardened PLL goes into the abnormal mode. In this mode, the resistance R_S senses the SET current and converts it to a voltage signal to activate OP_1 or OP_2 according to the polarity of the current pulse. Then OP_1 or OP_2 will turn on P_1 or N_1 and generate a compensative current to limit the SET current. Not until the current is reduced to less than $2I_P$ will the CCL shut down P_1 or N_1 and the PLL go back to the normal mode.

The CCL circuit does not introduce new vulnerable nodes. If a single-event strike hits the CCL circuit, leading to some impacts on the PLL, the mechanism should be that P_1 or N_1 is falsely turned on by the SET responses. Assuming that P_1 (N_1) is on due to a strike, it will source (sink) current to (from) V_C, then OP_2 (OP_1) will activate N_1 (P_1) to introduce a new sinking (sourcing) current to keep V_C constant. Furthermore, simulation results of SHPLL indicate that the peak perturbations of V_C in the CCL circuit are smaller than those in the CP.

In the abnormal mode, the current-limiting transistor can be simplified as a current-limiting resistance R_L. Therefore, the equivalent LPF can be achieved as shown in Fig. 4(c), and the transfer function of the LPF becomes

$$F(s) = \frac{R_L (R_P C_1 s + 1)}{(R_L + R_S + R_P) C_1 s + 1}. \tag{3}$$

Using Eq. (3), the new transfer function of the PLL can be obtained as

$$H(s) = \frac{V_C(s)}{i(s)} = \frac{R_L s(R_P C_1 s + 1)}{(R_L + R_S + R_P) C_1 s^2 + \left(1 + R_L R_P \dfrac{I_P}{2\pi} C_1 K_{VCO}\right) s + \dfrac{R_L I_P K_{VCO}}{2\pi}}. \tag{4}$$

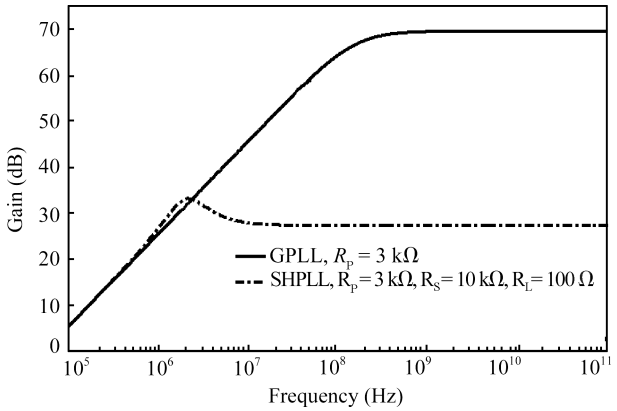

Fig. 5. Gain–frequency curves for GPLL and SHPLL.

According to Eq. (4), it can be concluded that the stable gain of V_C becomes $[R_L/(R_L+R_S+R_P)]R_P$, which is absolutely less than R_P. If the value of R_L is set to be far below the sum of R_S and R_P, the high frequency SET current can be largely mitigated. Figure 5 shows that the gain of V_C with respect to the SET current for SHPLL can be reduced to several orders of magnitude lower than that for GPLL. The maximum decrease of the gain is approximately 138 times lower, which cannot be achieved by adjusting R_P. As a result, the CCL circuit can effectively eliminate the voltage perturbation on V_C due to the decrease of the gain and the bandwidth.

Obviously, the larger R_S and smaller R_L can achieve a significant improvement in SET susceptibility, but design tradeoffs such as stability, performance and area must be considered. For example, decreasing R_L can increase the compensation current to improve the SET tolerance. However, it will increase the sizes of P_1 and N_1 so much that they will occupy a bigger area and slow down the response of the operational amplifier. Moreover, increasing R_S can greatly dampen the SET current and make the operational amplifier more sensitive to the SET current. Similarly, larger R_S can also have negative effects on PLLs. If R_S is increased near to the inner resistance of the current source, it would have an impact on the stability of I_P. On the other hand, larger R_S can decrease the response speed of the loop.

4. Simulation setup

To confirm the hardened effects of the PLL, complete schematics and layouts of two PLLs (GPLL and SHPLL) were designed in a 180 nm CMOS process. The only difference between them is that SHPLL implements a CCL circuit between the CP and the LPF. The layout of SHPLL occupying an area of $380 \times 130\ \mu m^2$ is displayed in Fig. 6.

In order to investigate the single-event transient on a PLL system, transistor-level simulations were performed on each individual PLL circuit using the Synopsys circuit simulator HSPICE. Several important analog blocks such as the CCL and the VCO were modeled by layout to achieve better accuracy. In the simulation, charge collections from heavy-ion strikes were simulated using a current pulse[4]. The single-event pulse was injected into the expected node after the PLL system was in its in-lock condition. The PLL circuits were simulated at 700 MHz, 800 MHz, 900 MHz, and 1 GHz. The peak voltage perturbations of V_C (ΔV_C) were recorded for all cases. Moreover, the outputs of these PLLs were recorded in order to examine the settling time of control voltage disturbance t_s during which V_C recovered to its final value.

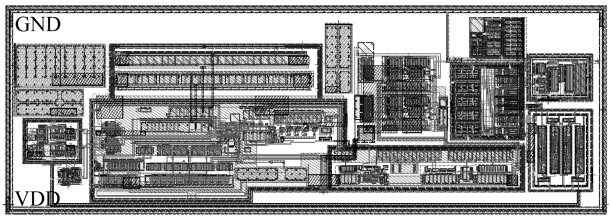

Fig. 6. Layout view of SHPLL.

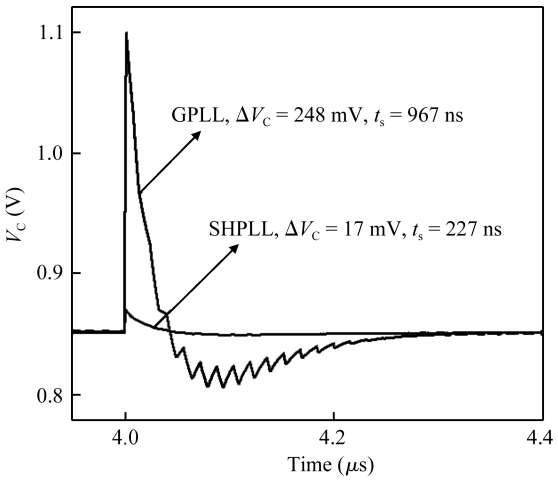

Fig. 7. V_C versus time for 1 GHz operation for GPLL and SHPLL.

5. Circuit simulation results and analysis

The simulation results prove that the CCL circuit can effectively reduce the control voltage disturbance and the recovery time due to single-event strikes. The voltage perturbations and the recovery time resulting from a strike in the CP for GPLL and SHPLL operating at 1 GHz are shown in Fig. 7. The peak voltage perturbation of V_C from a strike in GPLL is 248 mV, while it is only 17 mV in SHPLL, resulting in approximately 93.1% improvement. In addition, the recovery time for SHPLL was 227 ns as compared to 967 ns for GPLL, leading to a 76.5% improvement.

Furthermore, the simulation results also prove that the hardening effects are independent of the operation frequency. The peak V_C perturbations and the recovery times achieved at different frequencies (700 MHz, 800 MHz, 900 MHz and 1 GHz) are shown in Fig. 8. The improvements of the peak V_C perturbations are almost 93.0%, while the improvements of the recovery time vary over a small range from 76.2% to 79.0%.

The improved hardness of SHPLL stems from the resistance R_S by preventing the deposited charge from disturbing V_C. This spike of V_C is significantly dampened by the low pass filter response. However, a serial resistance is not enough for a

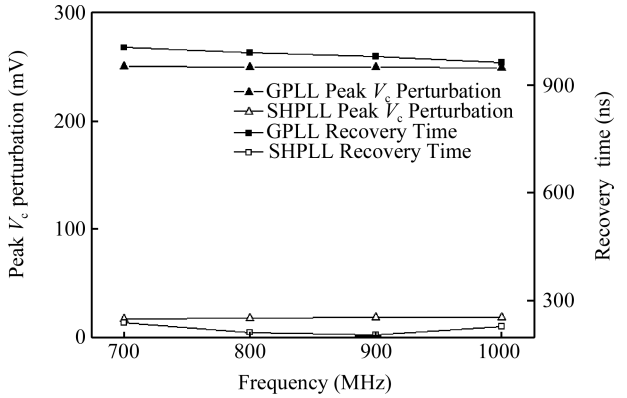

Fig. 8. Peak V_C perturbation and recovery time for different frequency operations for GPLL and SHPLL.

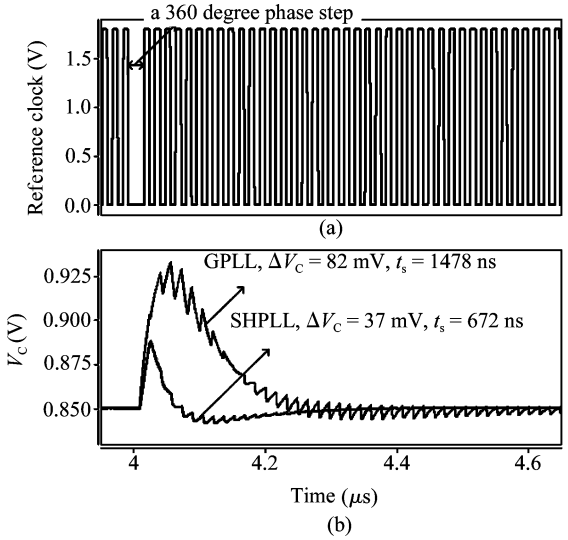

Fig. 9. (a) Reference clock with a 360° phase step; (b) V_C versus time for phase steps for GPLL and SHPLL.

SET hardened PLL, since the sensing resistance could dampen the SET current while simultaneously slowing down the settling speed of the loop. Another mechanism is necessary to improve the speed of the loop response. Additionally, the CLL circuit provides a current-limiting mechanism to meet this requirement. With the CCL circuit, another current path is established which is not limited by the current source transistors in the CP, in order to transfer a large amount of charge while the operational amplifier is open, and the voltage perturbation of V_C and the recovery time are decreased.

Finally, the CCL circuit can also assist PLLs to achieve a fast recovery procedure from the loss of lock due to phase or frequency shift, as well as a single-event strike. After introducing a 360 ° phase step into the reference clock, the two PLLs, GPLL and SHPLL, are driven into the state of loss of lock, as shown in Fig. 9. These two curves show that ΔV_C in GPLL is 82 mV, while the ΔV_C in SHPLL is 37 mV, resulting in approximately 54.9% improvement. Additionally, t_s for SHPLL is 672 ns as compared to 1478 ns for GPLL, leading to a 54.5% improvement. In contrast, the improved performance of SHPLL derives only from resistance R_S, because the CCL circuit is not active under the normal charge pump current I_P.

6. Conclusion

An RHBD technique for PLLs has been proposed for SET mitigation. The analysis of the effects of the SET current on the PLL behaviors demonstrates that reducing the gain of the control voltage can improve the SET performance. By presenting a novel SET-resistant circuit complementary current limiter and implementing it between the CP and the LPF, the PLL single-event susceptibility is considerably reduced in the presence of SETs in CPs, whereas it has little impact on the loop parameters in the absence of SETs in CPs.

Transistor-level simulations were performed using the 180 nm commercial CMOS process with single-event strikes represented by the current pulse model. The CCL circuit could significantly reduce the voltage perturbation on the input of the VCO by up to 93.1% and reduce the recovery time by up to 79.0%. In addition, the CCL circuit could also accelerate the recovery procedure of the PLL from loss of lock due to phase or frequency shift, as well as a single-event strike. Furthermore, this RHBD technique with SET current sensing and limiting mechanism could be readily applied to other similar circuit topologies to improve the SET tolerance.

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