A bootstrapped switch employing a new clock feed-through compensation technique*

Wu Xiaofeng(吴笑峰)[1,2,†], Liu Hongxia(刘红侠)[1], Su Li(苏立)[3], Hao Yue (郝跃)[1], Li Di(李迪)[1], and Hu Shigang(胡仕刚)[1]

(1 School of Microelectronics, Xidian University, Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, China)

(2 School of Information and Electrical Engineering, Hunan University of Science and Technology, Xiangtan 411201, China)

(3 NXP Semiconductors (Shanghai) Ltd, Shanghai 200070, China)

Abstract: Nonlinearity caused by the clock feed-through of a bootstrapped switch and its compensation techniques are analyzed. All kinds of clock feed-through compensation configurations and their drawbacks are also investigated. It is pointed out that the delay path match of the clock boosting circuit is the critical factor that affects the effectiveness of clock feed-through compensation. Based on that, a new clock feed-through compensation configuration and corresponding bootstrapped switch are presented and designed optimally with the UMC mixed-mode/RF 0.18 μm 1P6M P-sub twin-well CMOS process by orientating and elaborately designing the switch MOSFETs that influence the delay path match of the clock boosting circuit. HSPICE simulation results show that the proposed clock feed-through compensation configuration can not only enhance the sampling accuracy under variations of process, power supply voltage, temperature and capacitors but also decrease the even harmonic, high-order odd harmonic and THD on the whole effectively.

Key words: bootstrapped switch; clock feed-through compensation; delay path match

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1. Introduction

Track-and-hold circuits are a bottleneck in the design of high speed and high resolution A/D converters. The sampling switch is a vital component of a track-and-hold circuit and its accuracy and speed directly determine the performance of the whole track-and-hold circuit to a certain extent. At present, with the deep sub-micrometer and nanometer technology, bootstrapped switches are frequently used to reduce the on-resistance and nonlinearity of the switch[1−5]. However, the clock feed-through error introduced by the bootstrapped switch is dependent on input signal. Unlike the corresponding error caused by NMOS or CMOS switches, that error cannot be cancelled out by employing a fully differential structure. Lee[6−8] adopted a dummy switch that introduces a clock feed-through error which has an opposite phase and equal amplitude compared with that brought by the main switch to reduce the switch nonlinearity. But in that architecture, the change of the gate voltage of the dummy switch MOSFET needs some current which can only come from the sampling capacitor; obviously, this severely deteriorates the sampling accuracy. Reference [9] presented a new clock feed-through compensation topology. However, like the other configurations, the delay between the variation of the gate voltage of the main switch in the bootstrapped switch and the control clock of the dummy switch was not considered. This makes the clock feed-through compensation always precede the clock feed-through introduced by the main switch; therefore, the actual compensation effect is not good. Movahedian[10] also presented a clock feed-through compensation topology. The topology can resolve the above problem theoretically; however, the auxiliary track-and-hold circuit and the main switch use the same clock boosting circuit, which results in a matching issue of the time constant between the clock feed-through caused by the main switch and that caused by the dummy one. For that reason, the compensation topology cannot have the ideal effect. In this paper, firstly, the fundamental principles and the existing problems with several kinds of clock feed-through compensation configuration are analyzed. Then, an improved clock feed-through compensation configuration version based on that presented in Ref. [10] is proposed. In addition, the corresponding bootstrapped switch is also designed with optimization.

2. Analysis of clock feed-through compensation topologies

2.1. Clock feed-through of the bootstrapped switch and its impact

Figure 1 shows the clock feed-through in an MOS switch.

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† Corresponding author. Email: willow_wxf@hotmail.com

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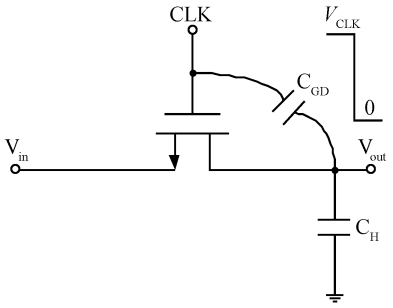

Fig. 1. The clock feed-through of a MOS switch.

Because the gate–drain parasitic capacitance C_{GD} and the sampling capacitance C_H form a capacitive voltage divider, when the gate clock signal goes from a high level V_{CLK} to "0" (low level, approximately equal to 0 V), the transition of the gate voltage is coupled to $C_H$through C_{GD}, which results in clock feed-through. Clock feed-through changes the voltage stored on C_H by an amount equal to

$$\Delta V = -V_{CLK}\frac{C_{GD}}{C_{GD}+C_H}. \tag{1}$$

This equation indicates that for a simple MOS switch (a CMOS switch can be analyzed similarly), the feed-through is independent on input signal, so the influence of the clock feed-through introduced by C_{GD} on the sampling output is linear. An offset thus appears which is directly proportional to the clock signal voltage V_{CLK}. Fortunately, the fully differential structure can be used to cancel out the offset. But for a bootstrapped switch, clock feed-through will introduce signal dependent error. Figure 2 shows the illustration of the clock feed-through of a bootstrapped switch. In this figure, when the gate voltage of the switch drops from $V_{inp(n)} + V_C$ to 0 (where $V_{inp(n)}$ is the input signal and V_C is the voltage across the boosting capacitance at the end of the tracking phase), the switch turns off, and the gate voltage variation is coupled to the sampling output terminal $V_{outp(n)}$ via the gate–drain parasitic capacitance $C_{GD\_P(N)}$. The coupling causes voltage variation which can be expressed as

$$\Delta V_{btst\_p(n)} = -(V_{inp(n)} + V_C)\frac{C_{GD\_P(N)}}{C_{GD\_P(N)} + C_{H\_p(n)}}, \tag{2}$$

and the change in the differential sampling output signal caused by the above voltage change appears as (because the circuit is symmetrical, therefore, $C_{GD\_P} = C_{GD\_N}$ and $C_{H\_p} = C_{H\_n}$)

$$\begin{aligned}\Delta V_{btst\_diff} &= \Delta V_{btst\_p} - \Delta V_{btst\_n}\\ &= -(V_{inp} - V_{inn})\frac{C_{GD\_P(N)}}{C_{GD\_P(N)} + C_H}\\ &= -V_{in}\frac{C_{GD}}{C_{GD}+C_H}.\end{aligned} \tag{3}$$

Equation (3) indicates that the clock feed-through caused by the gate–drain parasitic capacitance of the switch transistor in the bootstrapped switch brings some error to the differential sampling output signal and the error is directly proportional to the differential input signal when the switch size is constant. Because the sampling capacitor is a MIM capacitor, its value exhibits voltage coefficients due to space charge generated between the electrodes (temperature variation also contributes to the nonlinearity through corresponding coefficients; this effect will be neglected here for simplicity). Therefore, the C_H can be approximately expressed by a second order polynomial as below:

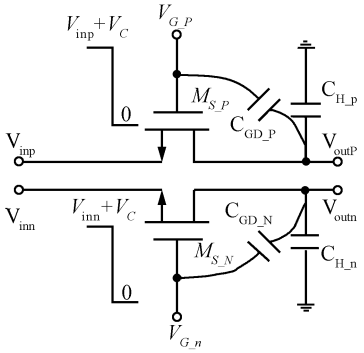

Fig. 2. The clock feed-through of a bootstrapped switch.

$$C_H(V_{out}) = C_{H0}(1 + VC1 \times V_{out} + VC2 \times V_{out}^2). \tag{4}$$

In Eq. (4), VC1 and VC2 are first and second voltage coefficients; in this process, they are 14.62 ppm/V and 9.68 ppm/V^2 respectively. C_{H0} is the nominal value of C_H. Owing to the fact that VC1 and VC2 are very small and the differential sampling output voltage on C_H contains less third order harmonic, we can let $V_{out} \approx V_{in} = \sin\omega t$ when substituting Eq. (4) into Eq. (3). Now, Equation (3) can be expanded as

$$\begin{aligned}&\Delta V_{btst\_diff} = -V_{in}\frac{C_{GD}}{C_{GD}+C_H}\\ &= -\sin(\omega t)\frac{C_{GD}}{C_{H0}[1 + C_{GD}/C_{H0} + VC1\sin(\omega t) + VC2\sin^2(\omega t)]}\\ &\cong -\sin(\omega t)\frac{C_{GD}}{C_{H0}}[1 - C_{GD}/C_{H0} - VC1\sin(\omega t) - VC2\sin^2(\omega t)]\\ &= \frac{C_{GD}VC1}{2C_{H0}} + \left[-\frac{C_{GD}}{C_{H0}} + \frac{3C_{GD}VC2}{4C_{H0}} + (\frac{C_{GD}}{C_{H0}})^2\right]\sin(\omega t)\\ &-\frac{C_{GD}VC1}{2C_{H0}}\cos(2\omega t) - \frac{C_{GD}VC2}{4C_{H0}}\sin(3\omega t).\end{aligned} \tag{5}$$

In Eq. (5), the approximation formula $1/(1 + x) \approx 1 - x$ is applied because $C_{GD} \ll C_{H0}$ and VC1, VC2 are very small. From the analysis above, we can see that because of the nonlinearity of the sampling capacitor, clock feed-through of the bootstrapped switch introduces a nonlinear error in which the second harmonic is dominant. In addition, the derivation of Eqs. (3) and (5) is based on differential circuits, and it shows that the error cannot be cancelled out by just employing differential structure. Moreover, the larger the switch size and the greater the amplitude of the input signal, the more evident the nonlinearity is. For these reasons, in the design of a high speed

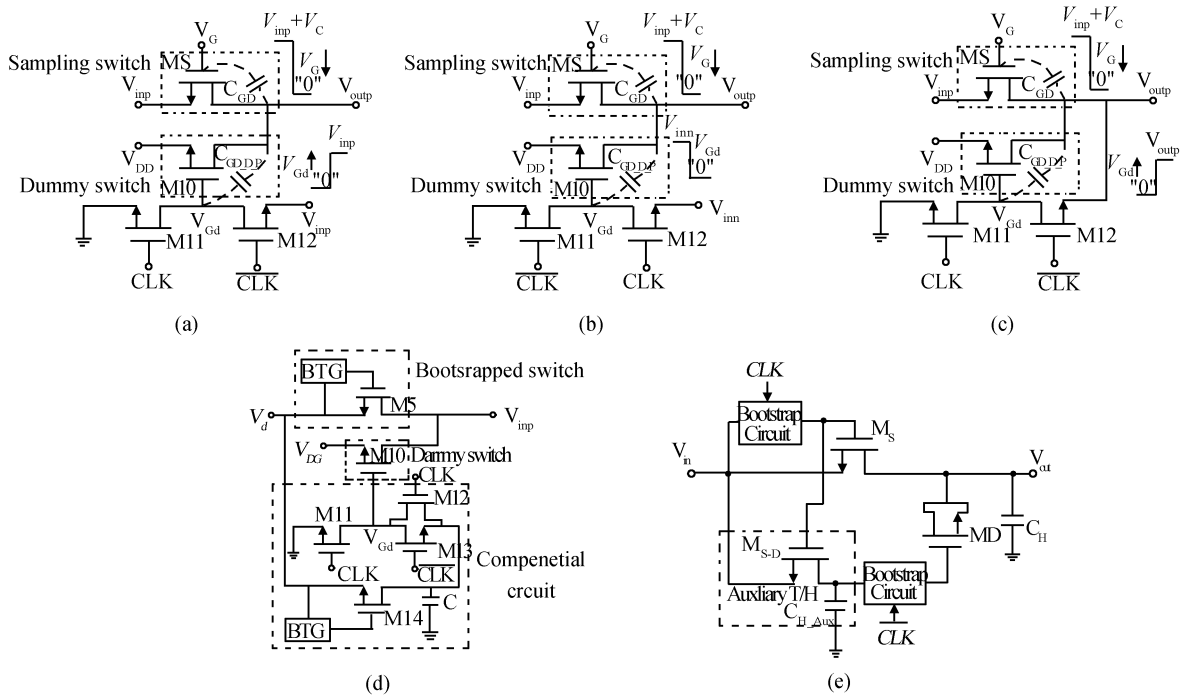

Fig. 3. Five kinds of clock feed-through compensation architecture.

and high accuracy bootstrapped switch, clock feed-through becomes a key factor that restricts the improvement of the linearity of this kind of switch.

2.2. Feed-through compensation configurations and their shortcomings

The fundamental principle of clock feed-through compensation is as follows: when the clock signal transits from high to low, at the node affected by clock feed-through, adding a transient compensation voltage with opposite phase and equal amplitude compared with ΔV cancels out the influence caused by the main clock feed-through. In general, the transient compensation voltage is still generated by clock feed-through and implemented by a dummy switch. There are several kinds of clock feed-through compensation architectures. Figure 3 gives five kinds of configuration (only the non-inverting input part of the differential topology is shown). In Fig. 3(a), the size of the dummy transistor M10 is the same as that of the main switch transistor MS. When CLK goes from high to low, the gate voltage of M10 will transit from 0 to $V_{\rm inp}$. The influence of the clock feed-through caused by the dummy transistor M10 on the voltage at node $V_{\rm outp}$ can be expressed as

$$\Delta V_{\rm outp\_dummy} = V_{\rm inp}\frac{C_{\rm GD\_D\_P}}{C_{\rm GD\_D\_P} + C_{\rm H}}. \tag{6}$$

For a fully differential structure, the influence of the introduced clock feed-through compensation on the differential output signal can be expressed as (for a symmetrical circuit, $C_{\rm GD\_D\_P} = C_{\rm GD\_D\_N} = C_{\rm GD\_D}$)

$$\begin{aligned}\Delta V_{\rm out\_dummy\_diff} &= \Delta V_{\rm outp\_dummy} - \Delta V_{\rm outn\_dymmy}\\ &= (V_{\rm inp} - V_{\rm inn})\frac{C_{\rm GD\_D\_P(N)}}{C_{\rm GD\_D\_P(N)} + C_{\rm H}}\\ &= V_{\rm in}\frac{C_{\rm GD\_D}}{C_{\rm GD\_D} + C_{\rm H}}.\end{aligned} \tag{7}$$

Comparing Eq. (3) and Eq. (7), it follows that, as the size of the dummy transistor M10 equals that of the main switch transistor MS, $C_{\rm GD\_D} = C_{\rm GD}$, at the sampling output terminal, the dummy transistor introduces a transient compensation voltage which has an equal amplitude and opposite phase compared with that described in Eq. (3), which counteracts the influence of the main switch clock feed-through on the sampling output. The topology in Fig. 3(b) is basically similar to the one in Fig. 3(a). The difference between them is that the gate voltage of the transistor M10 transits from $V_{\rm inn}$ to 0 when the clock signal CLK goes from high to low. The influence of the clock feed-through caused by M10 on the voltage at node $V_{\rm outp}$ appears as

$$\Delta V_{\rm outp\_dummy} = -V_{\rm inn}\frac{C_{\rm GD\_D\_P}}{C_{\rm GD\_D\_P} + C_{\rm H}}. \tag{8}$$

For fully differential topology, it can be expressed as (for a symmetrical circuit, $C_{\rm GD\_D\_P} = C_{\rm GD\_D\_N} = C_{\rm GD\_D}$):

$$\begin{aligned}\Delta V_{\rm out\_dummy\_diff} &= \Delta V_{\rm outp\_dummy} - \Delta V_{\rm outn\_dymmy}\\ &= [-V_{\rm inn} - (-V_{\rm inp})]\frac{C_{\rm GD\_D\_P(N)}}{C_{\rm GD\_D\_P(N)} + C_{\rm H}}\\ &= V_{\rm in}\frac{C_{\rm GD\_D}}{C_{\rm GD\_D} + C_{\rm H}}.\end{aligned} \tag{9}$$

Equation (9) indicates that this topology also can theoretically cancel out the error introduced by the clock feed-through of the main switch. The similarity between the configuration in Fig. 3(c) and that in Fig. 3(a) is high. If the signal voltage across the on-resistance of the main switch transistor MS is not included, $V_{\rm outp}$ can be thought to be equal to $V_{\rm inp}$. Therefore, in Fig. 3(a), as long as the drain of M12 is connected with $V_{\rm outp}$,

then Figure 3(a) is transformed to Fig. 3(c). The influence of the clock feed-through compensation on the differential output signal is similar to Eqs. (7) and (9).

The above three kinds of compensation structure theoretically reduce the nonlinearity caused by the clock feed-through, but they have respective flaws and common ones. Concretely, in Fig. 3(a), when CLK is low, MS is off and M12 is on. Although M10 is always off, the input signal $V_{\mathrm{inp(n)}}$ can be coupled to the sampling output terminal through M12 and the parasitic capacitor $C_{\mathrm{GD\_D\_P(N)}}$ of M10, which will affect the voltage at the sampling capacitor C_{H}. As for Fig. 3(b), when CLK is high, the MS is on, and the circuit is in the tracking phase; at the same time, M12 is on, and the inverting input signal V_{inn} can be coupled to the output terminal through M12 and the parasitic capacitor $C_{\mathrm{GD\_D\_P(N)}}$ of M10. Because the coupled signal and the signal through MS are inversed, that will reduce the signal magnitude at the sampling capacitor C_{H} and deteriorate the dynamic and static performance of the circuit. Moreover, for the above two configurations, the higher the frequency of the input signal is, the lower the impedance of $C_{\mathrm{GD\_D\_P(N)}}$ is and the more serious the influence of input signal on the sampling capacitor C_{H} via the $C_{\mathrm{GD\_D\_P(N)}}$ is. The structure in Fig. 3(c) solves the above problems, but it introduces new interference, because when CLK becomes low, the current for the gate voltage variation of the dummy transistor M10 comes from the charge stored at the sampling capacitor, which results in charge sharing between C_{H} and the gate parasitic capacitance $C_{\mathrm{G\_D}}$ of M10 and then severely affects sampling accuracy. In addition, the above three topologies have a common drawback: if the amplitude of the input signal is close to the power supply voltage V_{DD}, M12 will not turn on, and the clock feed-through compensation circuit will fail. Reference [9] presented a clock feed-through configuration as shown in Fig. 3(d). The sizes of MS, M10 and M14 are equal. BTG represents the clock boosting circuit. The compensation idea originates from Fig. 3(c).The capacitance C and the transistor M14 make up an auxiliary track-and-hold circuit. The voltage for compensating the clock feed-through is supplied by capacitance C instead of C_{H}, and this topology theoretically implements the clock feed-through compensation without degradation of accuracy. Moreover, the CMOS switches M12 and M13 will turn on even if the amplitude of the input signal is close to V_{DD} to ensure that the compensation circuit works normally. However, the fluctuation of technology, temperature and the value of capacitance C leads to low robustness of the circuit. The configurations in Fig. 3(a) to Fig. 3(d) suffer from a common shortcoming. Due to the inner delay of the clock boosting circuit, the variation of the gate voltage of M10 lags behind that of the clock signal CLK. This indicates that the clock feed-through introduced by the dummy transistor for compensation precedes the clock feed-through of the main switch. Consequently, the compensation effect of these configurations is very limited. Movahedian[10] presented a configuration that is free of this problem; the circuit is shown in Fig. 3(e). When CLK is high, the sampling capacitor C_{H} and $C_{\mathrm{H\_Aux}}$ sample the input signal through the main switches MS and MS_D respectively. The voltage at C_{H} and that at CH_Aux is equal at the end of sampling. When CLK transits from high to low, $\overline{\mathrm{CLK}}$ will change in an opposite direction and the dummy switch MD will introduce clock feed-through with equal amplitude and opposite phase compared with that caused by the main switch. Like the circuit in Fig. 3(d), the voltage which compensates the clock feed-through is provided by the capacitor CH_Aux instead of C_{H}, which does not affect the sampling accuracy. Unfortunately, although the dummy switch MD is not directly controlled by the clock $\overline{\mathrm{CLK}}$, MS and MS_D use the same clock boosting cell, which will increase the gate parasitic capacitance of MS and MS_D, making the capacitance on the gate of MS be unequal to that of MD and finally leading to de-synchronization between the two paths of clock feed-through, thus decreasing the effectiveness of the compensation. More seriously, the increased gate parasitic capacitance of MS and MS_D will increases their on-resistances and brings more third-order harmonic[11]. Therefore, this compensation configuration will not give a favorable effect.

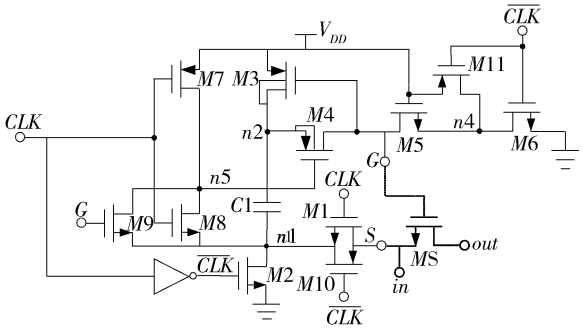

Fig. 4. Clock boosting circuit used in the paper.

3. Bootstrapped switch employing new clock feed-through compensation

Figure 4 gives the clock boosting circuit used in this paper. It works as follows: when the clock signal CLK is low, the CMOS switches M1, M10 are off and M2 is on. Simultaneously, the voltage at node n2 goes low. Because M7 is on and the voltage at node n5 is high, M4 is off. So the voltage variation of node S which is connected to the source of the main switch transistor will not change the voltage at the inner nodes of the clock boosting circuit. Meanwhile, M5 and M6 are on; the charge at the node G is discharged via the on-resistances R_{on5} of M5 and R_{on6} of M6. The discharging time constant is the product of the parasitic capacitor C_{pG} at node G and (R_{on5}+R_{on6}). Soon after this, the voltage of node G becomes low. M3 starts to be on. V_{DD} charges the capacitor C1 through the on-resistance R_{on2} of M2 and R_{on3} of M3.The charging time constant is the product of C1 and $R_{\mathrm{on2}} + R_{\mathrm{on3}}$. For a short time, the voltage at C1 is charged to $V_{\mathrm{DD}} - V_{\mathrm{DS3}} - V_{\mathrm{DS2}}$. When CLK is high, M5 and M6 are off, M1 and M10 are on, and M2 is off. The node voltage at n1 tracks the variation of that at node S. If the charge sharing caused by the parasitic capacitance at node n2 is neglected, the voltage at

node n2 is $V_S + V_{DD} - V_{DS3} - V_{DS2}$. M8 and M4 are on at this time, the voltage at node G will be close to the voltage at node n2, and M3 is off, which makes the voltage between the node S and the node G become approximately $V_{DD} - V_{DS3} - V_{DS2}$ and gate voltage boosting is implemented. Considering the reliability of the circuit, M9 is added to ensure that the voltage across the gate-source of M4 does not exceed V_{DD} when M4 is on; M5 is also used to ensure that V_{GD} and V_{DS} of M6 do not exceed V_{DD} when CLK is low. M11 is utilized in the circuit as adopted in Ref. [12] to reduce charge leakage at node G when CLK is high.

The above analysis indicates that whether the clock signal CLK goes from high to low or vice versa, it needs a delay to make the voltage at node G track the variation of the CLK. In short, the speed of the voltage at the node G transiting from high to low depends on the on-resistances of M5 and M6 and the parasitic capacitance at node G, while the speed of the voltage at the same node varying from low to high depends on the on-resistances of CMOS switches M1 and M10, the on-resistance of PMOS switch M4, the impedance of the input signal source (input signal is connected to the node S as shown in Fig. 4) and on the boosting capacitance C1. When the voltage at node G changes from high to low, it is the delay that causes the compensation effect of the several kinds of clock feed-through compensation configuration in Fig.3 to be very limited. Obviously, this is because the clock feed-through introduced by the dummy transistor M10 precedes that caused by the main switch MS. It is natural to associate that postponing the occurrence of the clock feed-through brought by the dummy switch can synchronize it with that introduced by the main switch. The simplest solution is to add some buffers to the clock signal CLK controlling M12 in Figs. 3(a) to Fig. 3(c) or to the CLK ($\overline{\text{CLK}}$) controlling M12 and M13 in Fig. 3(d) for delay. But the scheme has two drawbacks. First, for particular temperature, corner and power supply voltage, although the buffer circuit can be adjusted to ensure synchronization between the two paths of clock feed-through, as long as the above conditions change, the synchronization will not be satisfied because their delay paths are different and different delay paths lead to different variation modes with the fluctuation of temperature, technology and power supply voltage. Secondly, in general, the buffer circuit consists of even inverters connected in series and the delay of a single inverter is mostly picoseconds. From the following simulation results, it is seen that the delay caused by the on-resistances of M5, M6 of the clock boosting circuit and the parasitic capacitance at node G is much greater than that introduced by a single inverter. In other words, in order to implement the delay, the number of the inverters required for the buffer is large, which increases the area of the circuit. The method of adding MOS capacitors between the inverters to increase the delay time and to reduce the number of the inverters is plausible for its high capacitance density, but the value of the capacitor greatly influences the delay of the buffer and it depends on the bias voltage on the MOS capacitor, which means that the delay will be very sensitive to power supply voltage. In sum, we should seek a delay path match solution from the clock boosting circuit itself.

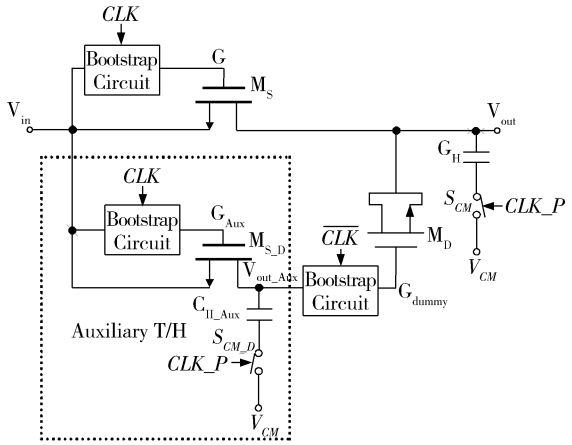

Fig. 5. Bootstrapped switch presented in the paper.

This paper presents an improved version of the clock feed-through configuration described in Ref. [10]; it is shown in Fig. 5. When the CLK is high, CLK_P is also high. Both the main switch MS and the main switch MS_D of the auxiliary track-and-hold circuit are on. V_{out} and V_{out_Aux}both track the difference between the input signal and input common mode voltage V_{CM}. When CLK_P becomes low, the switch SCM and SCM_D are off, bottom plate sampling is implemented and it basically cancels out the nonlinearity introduced by the charge injection of the switch MS and MS_D. Then CLK becomes low and the gate voltage of the main switch changes from $V_{in}+V_C$ to 0. At the same time, $\overline{\text{CLK}}$ varies from low to high, and the gate voltage of the dummy transistor MD (its length is the same as that of MS, and its width is half that of MS transits from 0 to $V_C + kV_{out\_Aux}$. Here, k represents the attenuation factor of V_{out_Aux} caused by the charge sharing between the parasitic capacitance at the internal node n1, n2 and G of the clock boosting circuit and the capacitor C_{H_Aux}. If the on-resistances of M1, M10 and M4 are ignored, the attenuation can be thought of as linear, and k is less than (but close to) 1. Considering the clock feed-through of MS_D, V_{out_Aux} can be expressed as

$$V_{out\_Aux} = V_{in} - (V_{in} + V_C)\frac{C_{GD\_Aux}}{C_{GD\_Aux} + C_{H\_Aux}}$$

$$= V_{in}\frac{C_{H\_Aux}}{C_{GD\_Aux} + C_{H\_Aux}} - V_C\frac{C_{GD\_Aux}}{C_{GD\_Aux} + C_{H\_Aux}}. \quad (10)$$

The influence of the clock feed-through caused by the parasitic capacitance $C_{GD\_D\_P(N)}$ of the dummy transistor MD on the single end output voltage appears as $(V_C+kV_{out\_Aux\_P(N)})[C_{GD\_D\_P(N)}/(C_{GD\_D\_P(N)}+C_H)]$. After utilizing the differential structure, the influence becomes (for a symmetrical circuit, $C_{GD\_D\_P} = C_{GD\_D\_N} = C_{GD\_D}$, in addition, $C_{GD\_D} = C_{GD}$)

$$V_{comp\_diff} = kV_{out\_Aux}\frac{C_{G-D\_D}}{C_{GD\_D} + C_H}$$

$$= k\frac{V_{\text{in}}C_{\text{H\_Aux}} - V_{\text{C}}C_{\text{GD\_Aux}}}{C_{\text{GD\_Aux}} + C_{\text{H\_Aux}}}\frac{C_{\text{GD}}}{C_{\text{GD}} + C_{\text{H}}}. \quad (11)$$

From Eq. (11), it follows that MD brings a transient compensation voltage to the sampling output terminal, and the voltage has approximately equal amplitude and opposite phase compared with that described in Eq. (3). With the exertion of the two paths of clock feed-through, their influence on the differential output voltage can be expressed as shown in Eq. (12) (with the same simplification and approximation method as employed in Eq. (5)). Equation (12) indicates that as long as k approaches 1 and $C_{\text{GD\_Aux}} \ll C_{\text{H\_Aux0}}$, the total error introduced by two paths of clock feed-through will approach 0 and the ideal clock feed-through compensation effect will be achieved. For the first requirement, $C_{\text{H\_Aux}}$ should be large enough compared with the parasitic capacitances at the internal node n1, n2 and G of the clock boosting circuit. As for the second requirement, it means that $C_{\text{H\_Aux}}$ should not be too large. This is because in order to achieve the same static sampling accuracy with the main track and hold circuit, the time constant

$$\begin{aligned}\Delta V &= \left(\frac{kC_{\text{H\_Aux}}}{C_{\text{GD\_Aux}} + C_{\text{H\_Aux}}} - 1\right)\frac{C_{\text{GD}}}{C_{\text{GD}} + C_{\text{H}}}V_{\text{in}} \\ &\quad - \frac{kV_{\text{C}}C_{\text{GD\_Aux}}}{C_{\text{GD\_Aux}} + C_{\text{H\_Aux}}}\frac{C_{\text{GD}}}{C_{\text{GD}} + C_{\text{H}}} \\ &\cong \frac{C_{\text{GD}}\text{VC1}(1-k)}{2C_{\text{H0}}} + \frac{C_{\text{GD}}}{2C_{\text{H0}}}\left\{2k\frac{C_{\text{GD\_Aux}}}{C_{\text{H\_Aux0}}}V_{\text{c}}\right. \\ &\quad \left.\times\left(\frac{C_{\text{GD\_Aux}}}{C_{\text{H\_Aux0}}} + \frac{C_{\text{GD}}}{C_{\text{H0}}} + \text{VC2} - 1\right) + 2k\frac{C_{\text{GD\_Aux}}}{C_{\text{H\_Aux0}}}\text{VC1}\right\} \\ &\quad + \left\{\left[-\frac{C_{\text{GD}}}{C_{\text{H0}}} + \frac{3C_{\text{GD}}\text{VC2}}{4C_{\text{H0}}} + \left(\frac{C_{\text{GD}}}{C_{\text{H0}}}\right)^2\right](1-k) - k\frac{C_{\text{GD}}}{C_{\text{H0}}}\frac{C_{\text{GD\_Aux}}}{C_{\text{H\_Aux0}}}\right\} \\ &\quad \times\sin\omega t - \left[\frac{C_{\text{GD}}\text{VC1}}{2C_{\text{H0}}}(1-k) + k\frac{C_{\text{GD}}}{C_{\text{H0}}}\frac{C_{\text{GD\_Aux}}}{C_{\text{H\_Aux0}}}(\text{VC1} + \text{VC2}V_{\text{C}})\right] \\ &\quad \times\cos 2\omega t - \frac{C_{\text{GD}}\text{VC2}}{4C_{\text{H0}}}(1-k)\sin 3\omega t, \end{aligned} \quad (12)$$

of the auxiliary track and hold circuit (i.e. the product of the on-resistance of MS_D and $C_{\text{H\_Aux}}$) should be small enough, which means that the width of MS_D will increase correspondingly and obviously, $C_{\text{GD\_Aux}}$ will increase therewith. In addition, for nonlinearity distortion, Equation (12) also shows that the term $C_{\text{GD\_Aux}}/C_{\text{H\_Aux0}}$ mainly exerts its influence on the second harmonic and the third harmonic is independent of it. Moreover, in Eq. (12), CGD_Aux/CH_Aux0 has a direct influence on dc offset. For the term $C_{\text{GD}}/C_{\text{H0}}$, it has a very important impact on the distortion introduced by clock feed-through as shown in Eqs. (5) and (12). Unfortunately, the selection of C_{H} depends on the noise budget of the system and C_{GD} rests with the sampling speed, accuracy and C_{H}; therefore, for clock feed-through and its compensation circuits, the ratio $C_{\text{GD}}/C_{\text{H0}}$ does not belong to the available variables. In sum, selecting appropriate $C_{\text{H\_Aux}}$ and designing the clock boosting cell carefully to reduce the parasitic capacitance at the node n1, n2 and G, the proposed compensation configuration can basically cancel out the influence of the clock feed-through introduced by the main switch transistor MS. In this paper, $C_{\text{H\_Aux}}$ is 0.22 pF and the W/L of MS_D is 30 μm / 0.18 μm. Moreover, for the clock boosting circuit in Fig. 4, the slope of the rising edge of the clock feed-through caused by MD can be adjusted by choosing the sizes of M1, M10 and M4 whereas the slope of the falling edge of the clock feed-through introduced by the main switch Ms can be adjusted by selecting the sizes of M5, M6 and M4. By fitting the two regulation processes together, the delay synchronization between the two paths of clock feed-through is satisfied.

4. Simulation results and analysis

The proposed clock feed-through compensation configuration is designed optimally and simulated through HSPICE with the UMC mixed-mode / RF 0.18 μm 1P6M P-sub twin-well CMOS process. In order to evaluate the compensation effect, two sets of simulations are performed, one is static performance and the other is dynamic performance. For the static performance, a differential DC input voltage of 0.5 V is injected to check the impact of the clock feed-though compensation on the accuracy of the differential sampling output signal. For the dynamic performance, the influence of the clock feed-though compensation on the switch is evaluated by applying a sinusoidal signal of 1 V_{pp} to the bootstrapped switch, and then doing FFT for the sampling output signal. It is worth mentioning that the voltage difference between the top plate and bottom plate of the sampling capacitor C_{H} is chosen to be the output and all the capacitors are implemented by the MIM capacitor.

Figure 6 gives the internal delay of the clock boosting circuit in Fig. 4 and the clock feed-through compensation configuration in Fig.5. The simulation parameters are as follows: the input clock signal frequency is 49.9712 MHz, the power supply voltage is 1.8 V, the temperature is 70 °C, the process corner is TT, the input common mode voltage V_{CM} is 0.9 V, C_{H} is 1.2 pF, $C_{\text{H\_Aux}}$ is 0.22 pF and the input is a 0.5 V differential DC signal. From the figure, the variation of the gate voltage V(g) at the main switch transistor MS lags behind that of the clock signal V(p1) (i.e. CLK in Fig. 4). Compared with the rising edge and the falling edge of V(p1), the rising edge and the falling edge of V(g) delay 218.12 ps and 232.39 ps respectively, which is in accordance with the previous theoretical analysis. In addition, Figure.6 also shows the contrast between the gate voltage V(g_dummy) of the dummy transistor MD and that of the main switch transistor MS (all in Fig. 5). Because the transition of V(g_dummy) from low to high is used as feed-through compensation, the rising edge of V(g_dummy) and the falling edge of V(g) can basically simultaneously appear by adjusting the size of M1, M10 and M4 in the clock boosting cell. From Eq. (11), we can conclude that because the amplitude of the clock feed-through brought by the dummy transistor MD is less than that introduced by MS, this design intentionally enables the rising edge of V(g_dummy) to slightly precede the falling edge of V(g).

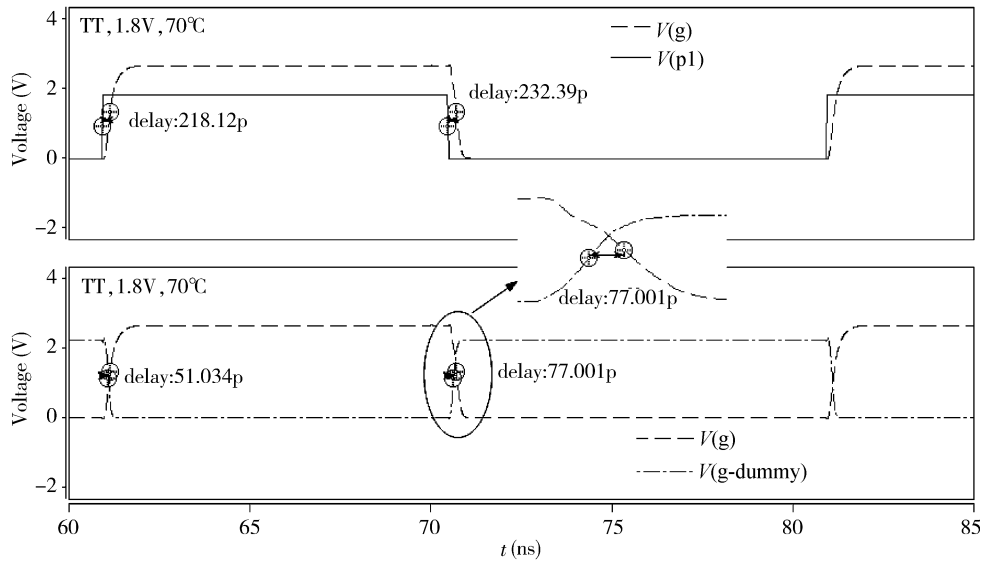

Fig. 6. Internal delay of the clock boosting circuit and the proposed clock feed-through compensation circuit.

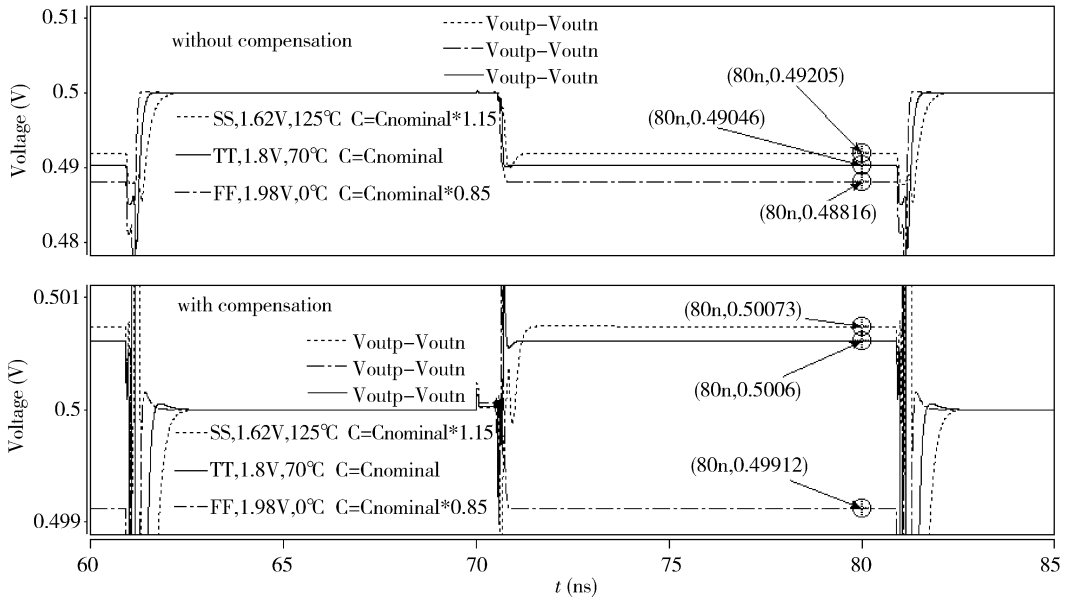

Fig. 7. Comparison of the static performance of the output voltage without clock feed-through and with the proposed compensation configuration.

Figure 7 is a comparison of the static performance of the output voltage without the clock feed-through compensation and with the compensation configuration presented in this paper. This figure indicates that with the proposed clock feed-through compensation, the differential output voltage hold error does not exceed 0.88 mV at different corners, power supply voltages, temperature and sampling capacitances. Even under the worst conditions (FF, 1.98 V, 0 °C, all capacitance is 85% of the nominal value), the influence of clock feed-through on the differential output voltage is only 7.43% of that without compensation. All the above simulation results show that the effect of this proposed clock feed-through compensation configuration is very obvious and it also has very good robustness.

Figure 8 shows the static performance of the differential output voltage of bootstrapped switches with several different clock feed-through compensation configurations. The simulation conditions are listed in the figure (in this simulation, the C in Fig. 3(d) and the $C_{\text{H\_Aux}}$ in Fig. 3(e) and Fig. 5 are 0.22 pF). From the figure, it can be concluded that the effect of the clock feed-through compensation configuration in Fig. 3(d) is very limited. The influence of the clock feed-through caused by the main switch on the differential output voltage is only reduced to 67.2% of that of bootstrapped switch without compensation. Because in the compensation architecture in Fig. 3(e), MS and MS_D use the same clock boosting circuit, the parasitic capacitance at the gate of the main switch MS is more than that of the dummy switch MD, which results in delay path mismatch between them and enables the falling edge of V(g) in MS to lag behind the rising edge of V(g) in MD. In other words, the clock feed-through introduced by MD precedes that caused by the main switch transistor MS, which makes output voltage exceed the ideal value 7.13 mV. For the topology presented in

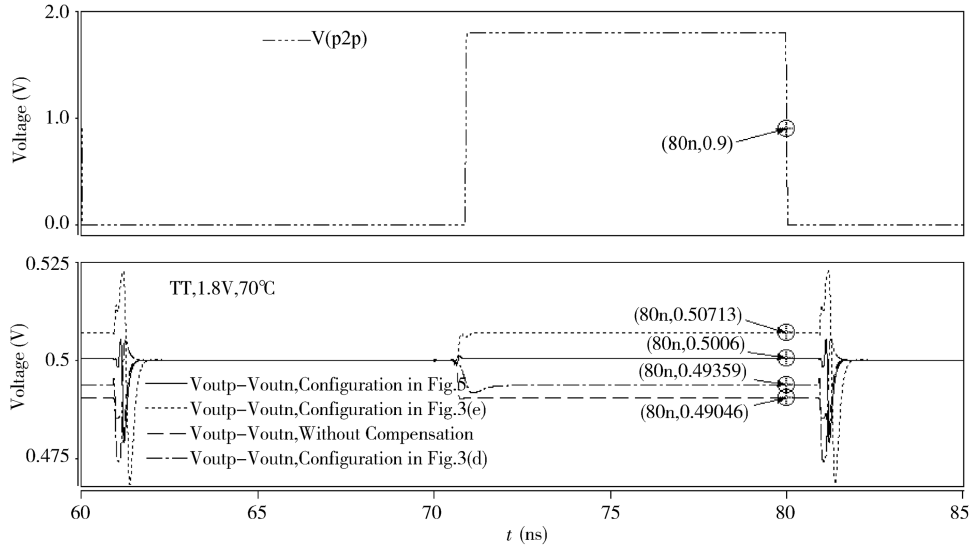

Fig. 8. Static performance of several different kinds of clock feed-through compensation configuration.

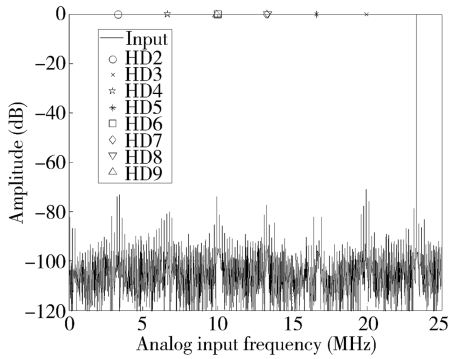

Fig. 9. FFT of the differential output voltage of the bootstrapped switch without clock feed-through compensation.

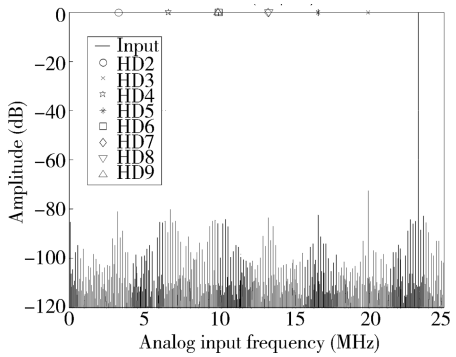

Fig. 10. FFT of the differential output voltage of the bootstrapped switch with the clock feed-through compensation configuration in Fig. 3(d).

this paper, the main switch transistor MS and that in the auxiliary track-and-hold circuit themselves employ a clock boosting cell, and the parasitic capacitance at the gate of the main switch MS equals that of the dummy switch MD. So long as the sizes of M1, M10, M4, M5, and M6 in the clock boosting circuit as shown in Fig. 4 are appropriately designed, their delay path match can be achieved. Therefore, the compensation effect is the best, as shown. Shown in Fig. 9 to Fig. 12 are the FFT of the differential output voltages of the bootstrapped switches without and with the clock feed-through compensation configurations shown in Fig. 3(d), Fig. 3(e) and Fig. 5.

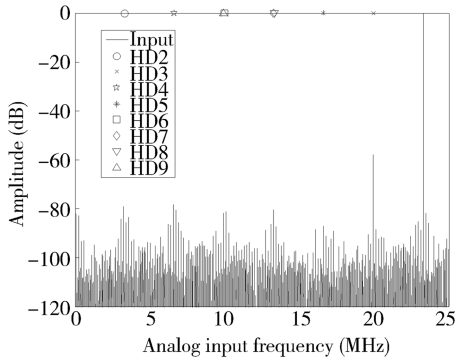

Fig. 11. FFT of the differential output voltage of the bootstrapped switch with the clock feed-through compensation configuration in Fig. 3 (e).

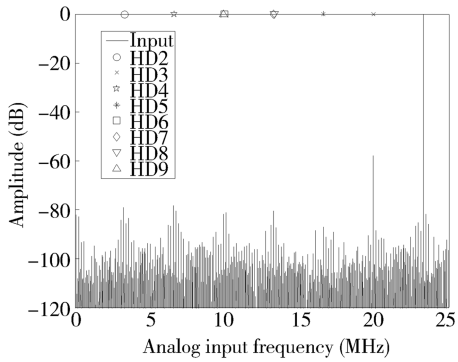

Fig. 12. FFT of the differential output voltage of the bootstrapped switch with the clock feed-through compensation configuration in Fig. 5 (proposed).

The simulation conditions are as follows: the input signal is a 1 V_{pp}, sinusoidal signal with 0.9 V bias voltage and its frequency is 23.3142 MHz. The input clock signal frequency is 49.9712 MHz (coherent sampling). The power supply voltage is 1.8 V, the temperature is 70 °C, the process corner is TT, the input common mode voltage V_{CM} is 0.9 V, C_H is 1.2 pF, C in Fig. 3(d) and the C_{H_Aux} in Fig. 3(e) and Fig. 5 are 0.22 pF. The simulation results of the 4096 point FFT of the output voltage are shown in Table 1. From this table, we can see that

Table 1. Comparison of the dynamic performance of output voltage without and with different compensation configurations.

Performance index	Without compensation	With compensation in Fig. 3(d)	With compensation in Fig. 3(e)	With compensation in Fig. 5 (proposed)
SNDR (dB)	62.7749	68.0662	57.782	67.3192
SNR (dB)	64.1219	70.3332	68.8186	71.0595
ENOB (bit)	10.1354	11.0143	9.306	10.8902
SFDR (dB)	71.1472	72.901	58.1879	69.8721
THD (dB)	−68.5155	−71.9739	−58.1383	−69.7046

Table 2. Comparison of the harmonic components of the output voltage with different compensation configurations.

Harmonic order number	Without compensation (dB)	With compensation in Fig. 3(d) (dB)	With compensation in Fig. 3(e) (dB)	With compensation in Fig. 5 (dB) (proposed)
2nd	–94.9593	–114.4275	–108.3728	–107.5870
3rd	–71.1472	–72.90095	–58.18791	–69.8721
4th	–92.1101	–110.21	–106.7192	–108.4851
5th	–91.3119	–82.70641	–87.36827	–93.9698
6th	–90.8544	–114.6869	–104.6826	–109.6861
7th	–77.4240	–83.5349	–80.44245	–100.3123
8th	–94.1876	–108.292	–106.7331	–100.7123
9th	–73.6661	–86.24015	–81.88224	–84.6512

SNR increases after adopting the clock feed-through compensation This is because with the compensation configurations in Fig. 3(e) or Fig. 5, the source and drain of the dummy transistor are shorted and its gate g_dummy is connected to the ground in the track phase, which forms a capacitor. Similarly, in Fig. 3(d), the gate is connected with ground; the C_{GD} of M10 is parallel connected with the sampling capacitor in the track phase. The capacitors and the sampling capacitor C_H sample the input signal together, which is equivalent to increasing the sampling capacitor. From Table 1, we also observe that the third-order harmonic of the input signal is still the main source of the nonlinear distortion of the circuit whether the clock feed-through compensation topologies are used or not. As analyzed in section 2.2, with the compensation topology in Fig. 3(e), the three-order harmonic increases obviously, and all the dynamic performance deteriorates except SNR. In contrast, the compensation configuration in Fig. 3(d) can improve the dynamic characteristics overall. As for the topology in Fig. 5, only SFDR decreases a little after utilizing the compensation. This is because under the test conditions, the third order harmonic originates mainly from the body-bias effect instead of clock feed-through, so the compensation has little effect on the improvement of this harmonic. In addition, the voltage which compensates the clock feed-through is provided by the capacitor C_{H_Aux}, and this voltage contains considerable second order harmonic because of the clock feed-through of MS_D; when we use it as a compensation voltage, the second order harmonic will multiply with the fundamental (this can also be explained as was done for Eq. (5)) to produce some more third order harmonic. Table 2 is a comparison of the harmonic components of the output voltage with different compensation configurations. From this table, it can be concluded that the clock feed-through compensation mainly reduces the even harmonic and its effect on the high-order odd harmonic distortion is better than that on the low-order ones. The first result accords with the explanation of Eq. (5), i.e. clock feed-through brings more even order harmonics. The second result still results from the fact that low-order odd harmonics arise mainly from the body-bias effect, whereas clock feed-through has less effect on them. However, for the generation of the high-order odd harmonic, the body-bias effect and clock feed-through contribute an almost comparable amount of nonlinearity; the effectiveness of the clock feed-through compensation emerges.

On the whole, from the static performance improvement, the proposed clock feed-through compensation configuration in this paper is excellent, the topology in Fig. 3(e) comes next, and the configuration in Fig. 3(d) is in last place. As for the dynamic performance enhancement, the circuit given in Fig. 3(d) and the proposed one are comparable, whereas the configuration in Fig. 3(e) is even poorer than the bootstrapped switch without feed-through compensation. In sum, using the presented clock feed-through compensation topology not only increases the sampling accuracy effectively but also decreases the even harmonic (which means that the requirement for the bootstrapped switch match can be reduced); in addition, the anti-jamming ability to the high-order odd harmonic is also improved and THD is reduced to a certain extent.

5. Conclusion

All the above theoretical analyses and simulation results indicate that the clock feed-through compensation configuration presented in this paper can not only increase the sampling accuracy under variations of process, power supply voltage, temperature and capacitors but also lower the even harmonic

distortion, that of the high-order odd harmonic and THD effectively. The switch employing the clock feed-through compensation technique proposed in the paper can be widely applied in the design of low voltage and high speed sampling-data circuits.

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