Study and analysis of coefficient mismatch in a MASH21 sigma–delta modulator*

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Abstract: The quantization noise leakage of the first stage in a MASH21 sigma–delta modulator is analyzed. The results show that the finite DC gain of the opamp is the main reason for noise leakage, and finite GBW and SR only generate harmonic distortion. The relationship between DC gain and leakage is modeled and conclusions on design criteria are reached. As an example, a MASH21 modulator for a digital audio application is realized. This modulator, fabricated in an 0.18 μm mixed signal process, achieves an SNDR of 91 dB with 1.8 V supply, which verifies the analysis and design criteria.

Key words: mismatch; leakage; modeling; sigma–delta; modeling; DC gain
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1. Introduction

Rapid development of the integrated circuit process, especially the digital process, has dramatically improved chip density and calculation capability. These improvements will lead to a higher requirement for data converters. A sigma–delta[1, 2] data converter uses oversampling and noise shaping to reduce inband quantization noise. These two techniques also make the converter less sensitive to process mismatch. Sigma–delta converters have been extensively applied in low-frequency mid-frequency fields[3], and they are being used more and more in many low power multi-mode communication systems[4, 5].

Sigma–delta modulators can be divided into two groups: single loop and cascaded modulators. A cascaded modulator is also known as a MASH (multi stage noise shaping) modulator[6, 7]. It is made up of low order single loop ones. Idle tones can never be eliminated in single loop modulators[7]; when input frequency is extremely high or low, the idle tones may block the wanted signal. The MASH structure can avoid this effect inherently, which is a big advancement in digital audio applications. For MASH modulators, the matching requirement between analog and digital is more stringent, and a large mismatch can lead the former stage's quantization noise (E_1) to leak to the output[7–9].

In this paper, a mismatch analysis is given, starting from system analysis of a MASH modulator. The study shows that a mismatch of only 4 coefficients can cause E_1 leakage. Integrator transient behavior is modeled with MATLAB; simulation shows that finite DC_GAIN of the opamp is the biggest reason for E_1 leakage, and the finite GBW of the opamp generates harmonic distortion only. A digital audio MASH21 modulator is designed to verify the analysis results.

2. System analysis of E_1 leakage

Figure 1 shows a feedback MASH21 modulator, which has three coefficients. When the oversampling ratio (OSR) is 128 and the reference voltage is ± 1.8 V, simulation shows that $B = 2.5$, $\lambda = 1$, $\beta = 0.25$ make the modulator perform best on SNR, overload level and idle tone[8]. The following analysis will be on the basis of these coefficients.

The modulator output in Fig. 1 can be expressed as

$$Y_1 = X_1 \cdot \mathrm{STF1_a} + E_1 \cdot \mathrm{NTF1_a}, \tag{1}$$

$$Y_2 = [(Y_1 - E_1) - \lambda_a Y_1]\beta_a \cdot \mathrm{STF2_a} + E_2 \cdot \mathrm{NTF2_a}, \tag{2}$$

$$Y_3 = Y_1 H_1 + Y_2 H_2. \tag{3}$$

The digital noise cancellation networks H_1 and H_2 are expressed as

$$H_1 = \beta_d \cdot \mathrm{STF2_d} \cdot [1 + (\lambda_d - 1) \cdot \mathrm{NTF1_d}], \tag{4}$$

$$H_2 = \mathrm{NTF1_d}. \tag{5}$$

When the analog TF and digital TF match perfectly, E_1 can be totally removed at the output of the modulator, and Y_3 only contains E_2.

When B has a mismatch, E_1's TF can be expressed as

$$\mathrm{STF2_a} \cdot \beta \cdot \mathrm{NTF1_a} - \mathrm{DTF2_d} \cdot \beta \cdot \mathrm{NTF1_d}. \tag{6}$$

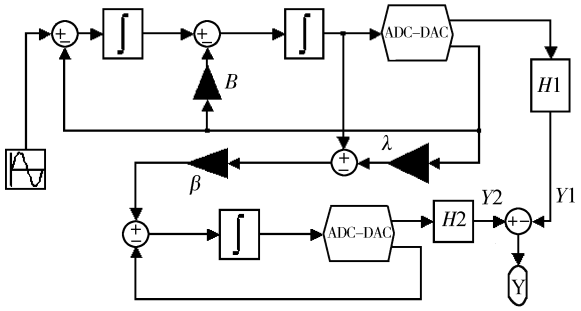

Fig. 1. Feedback MASH21 modulator.

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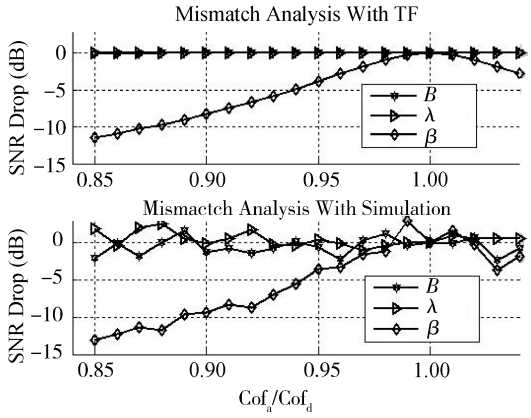

Fig. 2. Mismatch effect in MASH21.

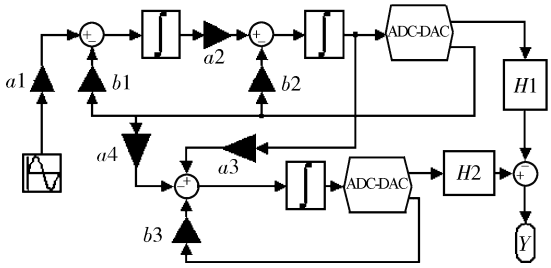

Fig. 3. Scaled MASH21 modulator.

$\mathrm{NTF1_a}$ and $\mathrm{NTF1_d}$ are the TF of the first stage in the analog and digital domains. This shows that E_1 is still shaped by third order.

When λ has a mismatch, E_1's TF can be expressed as

$$\mathrm{NTF1}^2 \cdot \mathrm{STF2} \cdot \beta \cdot (\lambda_\mathrm{d} - \lambda_\mathrm{a}). \tag{7}$$

This shows that E_1 is shaped by fourth order.

When β has a mismatch, E_1's TF can be expressed as

$$\mathrm{NTF1} \cdot \mathrm{STF2} \cdot (\beta_\mathrm{d} - \beta_\mathrm{a}). \tag{8}$$

This shows that E_1 is only shaped by second order, so mismatch of β causes the most severe leakage.

Figure 2 is the leakage effect obtained from TF analysis and an ideal modulator simulation with MATLAB. The horizontal axis is the mismatch between analog and digital. From the charts, it can be seen that these two results are in good agreement.

The integrator output in Fig. 1 will be 10 V, so it needs to be scaled down to make sure it stays in the saturation range of the opamp. The scaled modulator is shown in Fig. 3.

The unscaled and scaled modulators have relationships that are expressed as

$$B = \frac{b_2}{a_2 b_1},\ \beta = \frac{b_1 a_2 a_3}{b_3},\ \lambda = \frac{a_4}{b_1 a_2 a_3}. \tag{9}$$

The scaled modulator's integrator output is limited at 1.2 V. The mismatch result for the scaled modulator is shown in Fig. 4.

Figure 4 shows that only b_1, a_2, a_3 and b_3's mismatches can cause as big a leakage as shown in Fig. 2. In Eq. (9), it can be seen that these parameters are all related to β. Thus, the scaling process has been proved correctly.

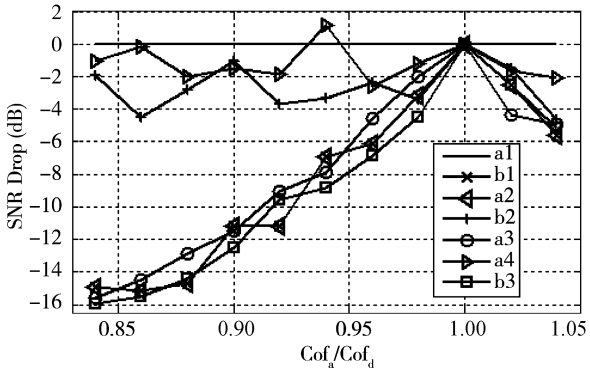

Fig. 4. Mismatch result of scaled MASH21.

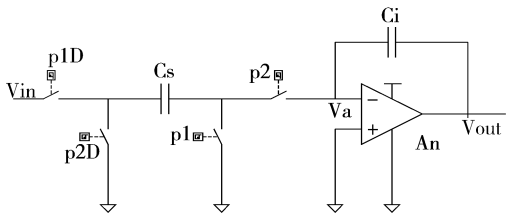

Fig. 5. Switched capacitor delay integrator.

3. Circuit modeling analysis of the mismatch

The integrator is the modulator's core block. Figure 5 shows a switched capacitor implementation of a delay integrator in Fig. 3. This circuit is controlled by the non-overlapping clocks P1, P1D, P2 and P2D[10].

The ideal gain of the integrator is $g = C_\mathrm{s}/C_\mathrm{i}$. Process mismatch and circuit non-ideality will cause gain variation. Process mismatch is less than 1%[11], so it can be ignored. The opamp can be modeled as a single pole system, and the transient response of the integrator[4, 12, 13] can be expressed as

$$V_\mathrm{o}(t) = (1+g)V_\mathrm{a}(t) + K_\mathrm{i}, \tag{10}$$

$$V_\mathrm{a}(t) = -a_2/a_1 \cdot (1 - e^{a_1 t}) + V_\mathrm{a}(0) \cdot \mathrm{e}^{a_1 t}, \tag{11}$$

$$a_1 = \frac{g_\mathrm{m}}{C_\mathrm{eq}}\left(1 + \frac{1+g}{\mathrm{An}}\right),\quad a_2 = \frac{g_\mathrm{m}}{C_\mathrm{eq}}\left(V_\mathrm{os} - \frac{K_\mathrm{i}}{\mathrm{An}}\right), \tag{12}$$

$$C_\mathrm{eq} = C_\mathrm{s} + C_\mathrm{ip} + C_\mathrm{op} + (C_\mathrm{s} + C_\mathrm{ip})C_\mathrm{op}/C_\mathrm{i}. \tag{13}$$

In Eqs. (10)–(13), $V_\mathrm{o}(t)$ is the integrator's practical output voltage, K_i is its ideal output. $V_\mathrm{a}(t)$ is the opamp's inverting node voltage, and $V_\mathrm{a}(0)$ is the original value of $V_\mathrm{a}(t)$. C_eq is the opamp's equivalent load. C_ip and C_op are the opmap's input and output parasitic capacitor.

With the transient model of Eqs. (10)–(13), effects caused by the opamp's finite DC gain and GBW can be studied, and the result is shown in Fig. 6. It can be seen that when DC gain is low, the modulator spectrum has a second order slope in the signal band, which means that E_1 leaks to the output. When the opamp's GBW is low, the modulator will generate inband harmonics, but the spectrum slope is still third order. This means that a finite GBW does not cause E_1 leakage, so it can be said that DC gain is the main reason for E_1 leakage.

The integrator's non-idealities caused by the opamp's finite DC gain can be described with its effective gain g_eff, and

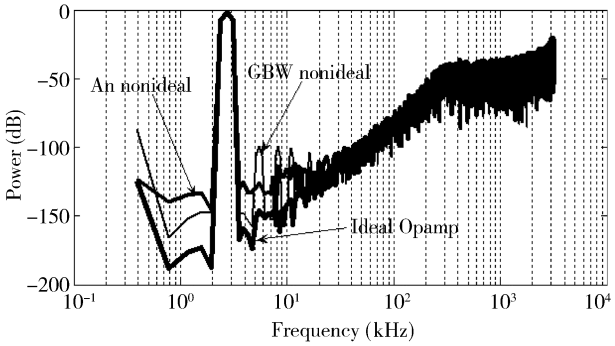

Fig. 6. MASH21 PSD with non-ideal OP.

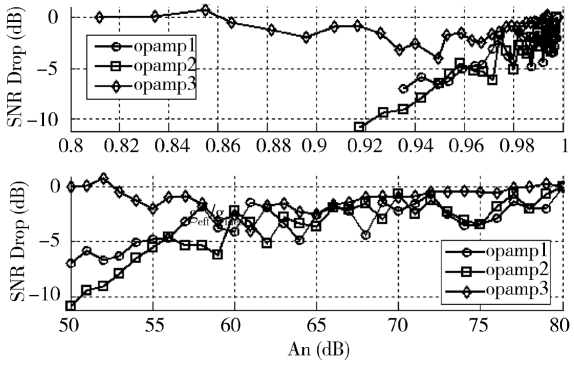

Fig. 7. Opamp finite An effect.

then the ideal integrator can be employed as in Section 2. The discrete time integrator can be expressed as

$$V_{\rm o}(n) = V_{\rm o}(n-1) + g_{\rm eff}V_{\rm in}(n-1). \tag{14}$$

With the transient response model of Eqs. (10)–(13), we can define $g_{\rm eff}$ as:

$$g_{\rm eff} = g + (1+g)V_{\rm a}(T_{\rm s}/2)/V_{\rm in}(n-1). \tag{15}$$

$g_{\rm eff}$ is not fixed when the modulator is working; its RMS value is employed here. The first integrator's $g_{\rm eff}$ determines the mismatch of a_1 and b_1; the second integrator's $g_{\rm eff}$ determines the mismatch of a_2 and b_2; the third integrator's $g_{\rm eff}$ determines the mismatch of a_3, a_4 and b_3.

Figure 7 shows the SNR drop caused by the opamp finite An. It can be seen that opamp3's finite DC gain causes nearly no SNR drop. This is because the third integrator's $g_{\rm eff}$ affects both a_3 and b_3, and their effects are cancelled by each other, as shown in Eq. (9). The first and second integrator's $g_{\rm eff}$ effects are in good agreement with Fig. 4.

4. Circuit design according to E_1 leakage

In this part, a MASH21 modulator is designed to verify the mismatch analysis. The modulator's bandwidth is 25 kHz, and the expected SNDR is 90 dB.

The MASH21 modulator is shown in Fig. 8[8]. Its sampling frequency is 6.4 MHz, and the reference voltage is ± 1.8 V. A single bit quantizer is used for the linearity consideration. The first stage sampling capacitance is 5 pF. The modulator's scaling parameters are $a_1 = 1/5, b_1 = 1/5, a_2 = 2/5, b_2 = 1/5, a_3 = 1/1, a_4 = 1/10, b_3 = 2/5$. It has an ideal SNR of 108 dB.

According to Fig. 7, the first and second opamp's An should be larger than 70 dB, when finite An causes leakage the SNR drop needs to be less than 5 dB. A two stage Miller opamp fits well into the system requirements[14–16]; this opamp is shown in Fig. 9.

Cascode PMOS is employed to enhance the opamp's DC gain. The common gate MOS close to the output node can use the smallest size to reduce the parasitic capacitance. The main specifications of the opamp are listed in Table 1.

Figure 10 shows a comparison between ideal modulator modeling, simulation and testing. The ideal modulator has 108 dB SNDR; the simulating SNDR is 100 dB, and the testing

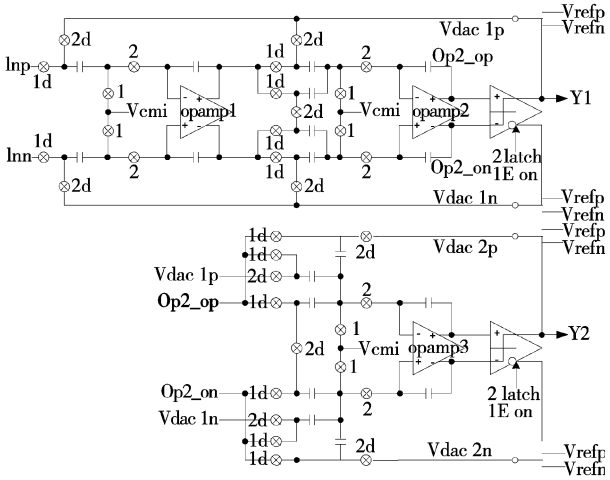

Fig. 8. Circuit implementation of the MASH21 modulator.

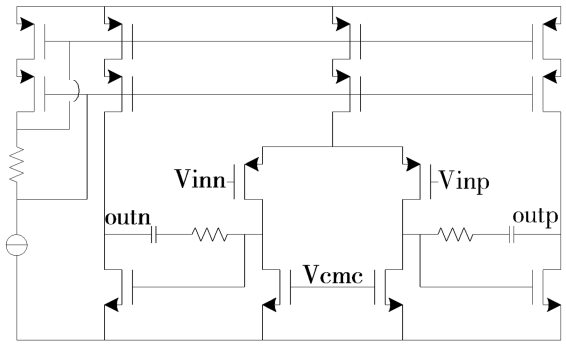

Fig. 9. Two stage Miller opamp.

Table 1. Opamp specifications.

Parameter	Opamp1	Opamp2/3
DC_gain (dB)	> 80	> 80
GBW (MHz)	35	30
$V_{\rm on}$ (mV)	< 100	< 100
SR (V/μs)	36	21/17
$C_{\rm eq}$ (pF)	7	3.5/4.5

SNDR is 91 dB. From Fig. 10 it can be seen that the simulation and test results have a good third order slope like the ideal modulator; this means that the opamp's specifications, and especially its DC gain, have reached the modulator's requirements

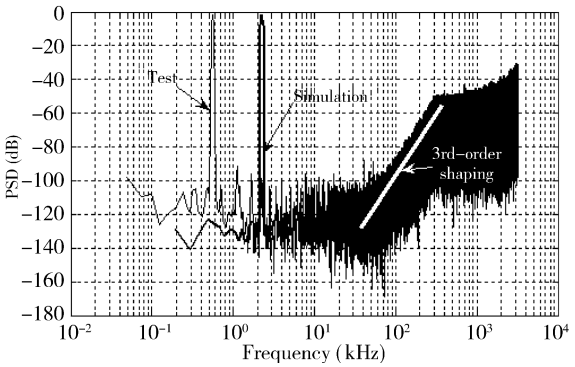

Fig. 10. Modulator output PSD.

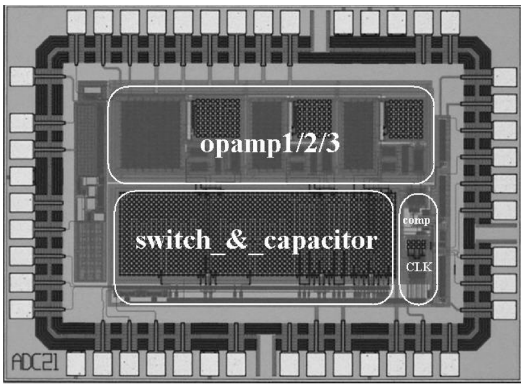

Fig. 11. Die photo of the audio MASH21 modulator.

and E_1 leakage has been eliminated very well.

The main specifications and a die photo of the modulator are shown in Table 1 and Fig. 11. The higher sampling frequency and small characteristic size make this work produce more harmonics, but the result is still very close to the design in Ref. [6].

5. Conclusions

In this paper, E_1 leakage in a MASH21 modulator is studied through system analysis and circuit modeling. A conclusion is reached that the finite DC gain of the opamp is the main reason for E_1 leakage. A digital audio MASH21 modulator is design to verify the design criteria; test results show that this modulator eliminates E_1 leakage very well, and the modulator achieves 91 dB SNDR.

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