Improved low-distortion sigma–delta ADC with DWA for WLAN standards*

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Abstract: An improved low distortion sigma–delta ADC (analog-to-digital converter) for wireless local area network standards is presented. A feed-forward MASH 2-2 multi-bit cascaded sigma–delta ADC is adopted; however, this work shows a much better performance than the ADCs which have been presented to date by adding a feedback factor in the second stage to improve the performance of the in-band SNDR (signal to noise and distortion ratio), using 4-bit ADCs in both stages to minimize the quantization noise. Data weighted averaging technology is therefore used to decrease the mismatch noise induced by the 4-bit DACs, which improves the SFDR (spurious free dynamic range) of the ADC. The modulator has been implemented by a 0.18 μm CMOS process and operates at a single 1.8 V supply voltage. Experimental results show that for a 1.25 MHz @ –6 dBFS input signal at 160 MHz sampling frequency, the improved ADC with all non-idealities considered achieves a peak SNDR of 80.9 dB and an SFDR of 87 dB, and the effective number of bits is 13.15 bits.

Key words: WLAN; low distortion; sigma–delta ADC; data weighted averaging
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1. Introduction

Wireless local area network (WLAN) technologies emerged in the 1980s as a high bandwidth, two-way data geographical area. By using radio as the transmission communication network operating over a limited medium, a wireless LAN serves as an extension to, or as an alternative for, a wired LAN. By using wireless LAN, users can access shared information without having to look for a place to plug in[1−3].

To achieve higher data rates in emerging wireless generations, the analog front-end must be able to handle wider bandwidths at lower noise and power levels. Generally, the minimum dynamic range of 60 to 80 dB for a 10 MHz bandwidth is required for these architectures. In order to achieve the necessary ADC performance, some modifications and optimization of conventional modulators have been made in this work. This paper also presents the architecture of the improved sigma–delta modulator and a comparison with the modulator presented before; the circuit design and the DWA mechanism; and experimental results and comparisons with conventional modulators.

2. Improved architecture

The modulator employs an improved MASH 2-2 multi-bit sigma–delta architecture which can achieve a low distortion performance and provide both greater SNDR and SFDR over a 10 MHz bandwidth. Multi-bit DACs which are able to reduce the quantization noise are used for both stages. The theoretical SNDR of a sigma–delta modulator is given by

$$\mathrm{SNDR} = \frac{3\pi}{2}\frac{2L+1}{\pi^{2L+1}}\left(2^B-1\right)^2\cdot \mathrm{OSR}^{2L+1}, \qquad (1)$$

where L is the order of the modulator, B is the number of bits of the quantizer, and OSR is the oversampling ratio. Obviously, the SNDR is determined by L, B and OSR and for a wide bandwidth application, such as the WLAN receiver, OSR and L cannot be made higher for the consideration of high sampling frequency, circuit complexity and power dissipation. In this design, an OSR of 8 and L of 4 have been chosen as a trade-off between the sampling frequency and the given signal bandwidth. Then, the quantizer resolution B determines the performance of the modulator since OSR and L have been determined. To reach the required SNDR specification of the receiver, 4-bit quantizers should be used for both stages. The whole architecture of the modulator is shown in Fig. 1. The first stage of the modulator is a second-order, 4-bit feed-forward architecture and the second stage has nearly the same structure in the absence of the added feedback factor. In order to decrease the mismatch noise of the 4-bit DAC, DWA technology should be used in the modulator, which will be described later. The transfer function of the first stage is given by

$$Y_1(z) = X(z) - \frac{(1-z^{-1})^2}{1+(a_1b_1-2)z^{-1}+(1-a_1b_1+a_1a_2b_2)z^{-2}}E_1(z), \qquad (2)$$

and the outputs of the integrators in the first stage are given respectively by

$$V = \frac{a_1z^{-1}(1-z^{-1})}{1+(a_1b_1-2)z^{-1}+(1-a_1b_1+a_1a_2b_2)z^{-2}}E_1(z), \qquad (3)$$

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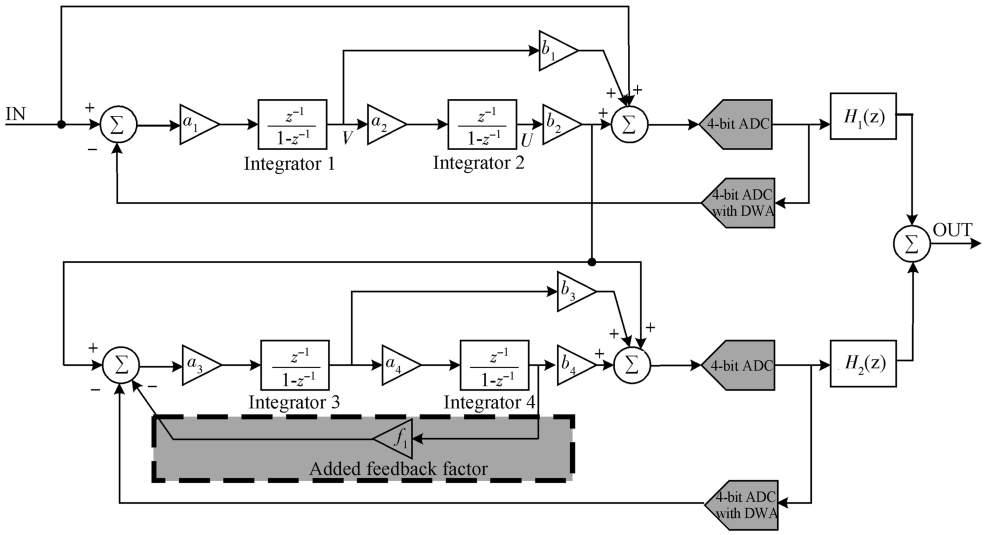

Fig. 1. Improved MASH 2-2 modulator architecture.

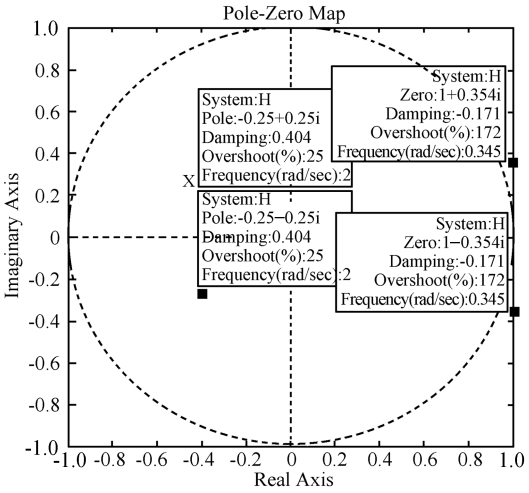

Fig. 2. Zeros and poles of NTF with feedback factor.

$$U = \frac{a_1 a_2 z^{-2}}{1 + (a_1 b_1 - 2)z^{-1} + (1 - a_1 b_1 + a_1 a_2 b_2)z^{-2}} E_1(z). \quad (4)$$

It is observed from Eqs. (3) and (4) that the integrators process only the quantization noise. As a result, the output swing of the integrators is reduced and the requirements of the operational amplifier are greatly relaxed. This is the advantage of the feedforward architecture[4].

The second stage adopts nearly the same structure as the first stage but adds a local resonator feedback factor f_1. In the conditional method, adding a small negative-feedback term around pairs of integrators in the loop filter, it is possible to move the open-loop pole, which becomes the noise transfer function (NTF) zero when the loop is closed, away from dc along the unit circle[5, 6]. However, this work has a large feedback factor and other factors such as b_3 and b_4 never have the original values which can be calculated from the conditional method.

The noise transfer function NTF of the second stage in this design is given by

$$\mathrm{NTF}(z) = \frac{1 - 2z^{-1} + (1 + f_1 a_3 a_4)z^{-2}}{1 + (a_3 b_3 - 2)z^{-1} + (1 + f_1 a_3 a_4 + a_3 a_4 b_4 - a_3 b_3)z^{-2}} \times E_2(z), \quad (5)$$

where $E_2(z)$ the quantization noise of the quantizer in the second stage. Then, the output of the second stage of the modulator can be given by

$$\begin{aligned} Y_2(z) &= b_2 U + \mathrm{NTF}(z) \\ &= \frac{a_1 a_2 b_2 z^{-2}}{1 + (a_1 b_1 - 2)z^{-1} + (1 - a_1 b_1 + a_1 a_2 b_2)z^{-2}} E_1(z) \\ &\quad - \frac{1 - 2z^{-1} + (1 + f_1 a_3 a_4)z^{-2}}{1 + (a_3 b_3 - 2)z^{-1} + (1 + f_1 a_3 a_4 + a_3 a_4 b_4 - a_3 b_3)z^{-2}} \\ &\quad \times E_2(z). \end{aligned} \quad (6)$$

Using Eqs. (2), (5), and (6), the final result after digital cancellation logic ($H_1(z)$, $H_2(z)$) can be obtained as

$$\begin{aligned} Y(z) &= H_1(z)Y_1(z) + H_2(z)Y_2(z) = z^{-2}X(z) - \frac{1}{a_1 a_2 b_2} \times \\ &\quad \frac{[1 - 2z^{-1} + (1 + f_1 a_3 a_4)z^{-2}](1 - z^{-1})^2}{1 + (a_3 b_3 - 2)z^{-1} + (1 + f_1 a_3 a_4 + a_3 a_4 b_4 - a_3 b_3)z^{-2}} \\ &\quad \times E_2(z), \end{aligned} \quad (7)$$

where $H_1(z) = z^{-2}, H_2(z) = (1 - z^{-1})^2/a_1 a_2 b_2$. The coefficients of the second stage should be scaled carefully since the transfer function is different from the first stage. From the discussion presented above and using MATLAB SDtoolbox, the proposed optimal coefficients of this work can be given by $a_1 = a_2 = a_3 = a_4 = f_1 = 0.5, b_1 = b_2 = 4, b_3 = 5, b_4 = 6$. Then, Equation (7) can be written as

$$Y(z) = z^{-2}X(z) - \frac{(1 - 2z^{-1} + 1.125z^{-2})(1 - z^{-1})^2}{0.125z^{-2} + 0.5z^{-1} + 1}. \quad (8)$$

The zeros and poles of NTF in Eq. (8) are shown in Fig. 2. The poles inside the unit circle ensure the stability of the modulator and the zeros, shifted away from dc but not along the unit circle, give a reduction of noise power at about 10 MHz.

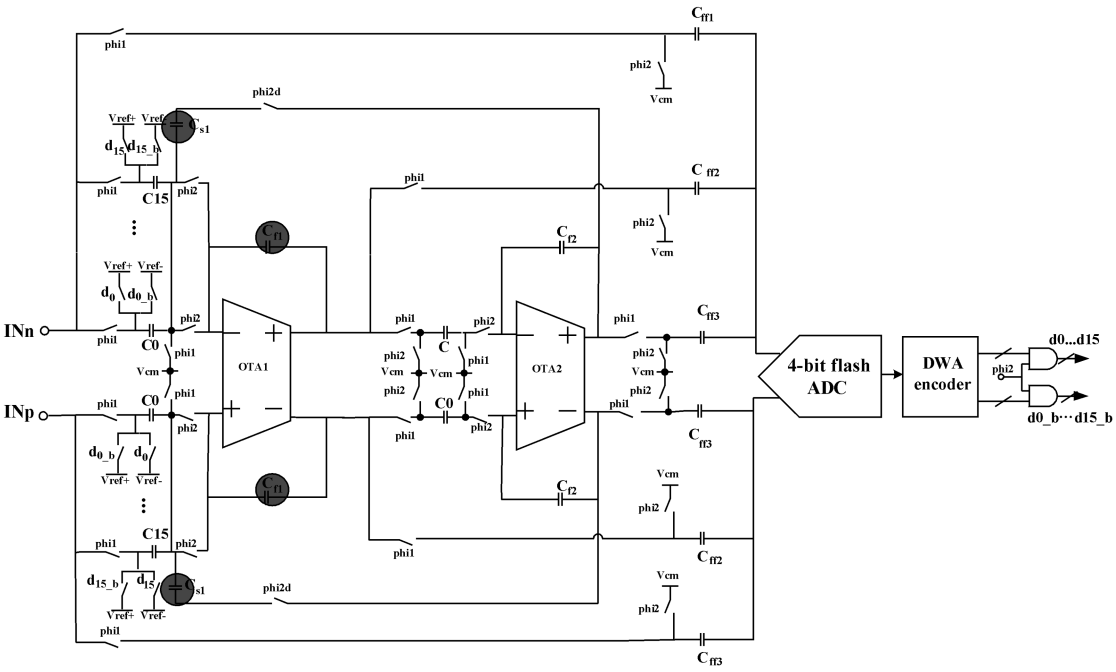

Fig. 3. Full differential SC CMOS implementation of the second stage.

3. Circuit design

The improved MASH2-2 multi-bit sigma–delta modulator is designed in TSMC 0.18 μm technology and operates at a 1.8 V supply voltage. Figure 3 shows the proposed full differential CMOS implementation of the improved second stage of the modulator. Switched-capacitor (SC) networks are used to implement the feedback and feed-forward paths. When clock phi1 is on, the output of OTA2 charges capacitor C_{s1}, and when clock phi2d is on, the charges on C_{s1} transfer to C_{fl} since the input of OTA1 is virtual ground. Therefore, C_{s1}/C_{fl} can realize the added feedback factor f_1. Clock phi1d and phi2d, the delayed versions of phi1 and phi2, are used to minimize the noise from switches. Bottom-plate sampling technology is also employed to minimize signal-dependent charge-injection and clock feed-through. The sizes of the sampling and integrating capacitors were governed by the noise requirements and matching requirements and there is a trade-off between mismatch consideration, KT/C noise and the layout area[7−12]. The sampling capacitors of the first order are combined with sixteen small unit capacitances to realize the 4-bit DAC and the DWA (data weighted averaging) technique is used to minimize the distortion introduced by the multi-bit DAC.

3.1. Integrator amplifier

The operational transconductance amplifier (OTA) in this design employs a full differential. The need for fast settling and an appropriate open-loop gain to suppress harmonic distortion encouraged the use of the folded cascade operational amplifier as shown in Fig. 4. Implemented by the switched-capacitor circuit, the common-mode feedback of the amplifier is also shown in Fig. 4. Since the performance of the modulator is relatively insensitive to non-linearity of the OTAs in the second stage, the requirements of OTA3 and OTA4 can be greatly relaxed and, therefore, the power of the modulator can be scaled down.

Table 1. Specifications of OTAs.

OTA specification	OTA1, 2	OTA3	OTA4
Finite DC gain (dB)	70	61	54
GBW (C_{load} = 5 pF) (MHz)	340	100	70
SR (C_{load} = 5 pF) (V/μs)	160	122	100
Phase margin (degree)	68	65	65
I_{diss} (mA)	3	2	1.3
P_{diss} (mW)	5.4	3.6	2.34

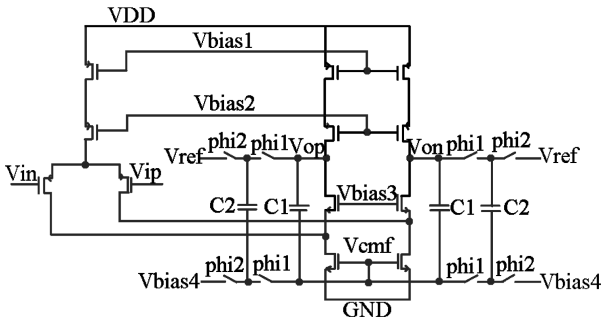

Fig. 4. Full differential folded cascade OTA with SC feedback circuit.

Table 1 gives the specifications of the OTAs used in the modulator, and Figure 5 shows the simulation results of OTA1 and OTA2.

3.2. 4-bit flash ADC and DWA of DACs

Figure 6 shows the architecture of the 4-bit flash ADC and the comparator used in the flash ADC. The distribution of the resistors employs a folded mode which could minimize the common-mode errors introduced by the resistors and comparators. Fast and power efficient regenerative comparators without pre-amplification are used in the 4-bit flash ADCs of both stages. The modulator performance is also very tolerant of the

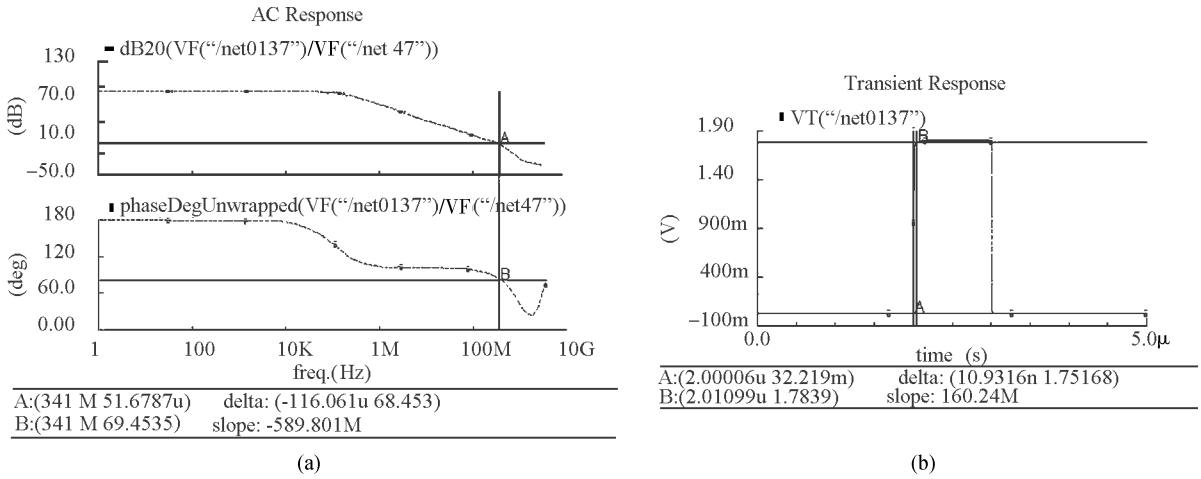

Fig. 5. Simulation results of OTA1,2. (a) Open-loop gain and phase margin. (b) Slew rate.

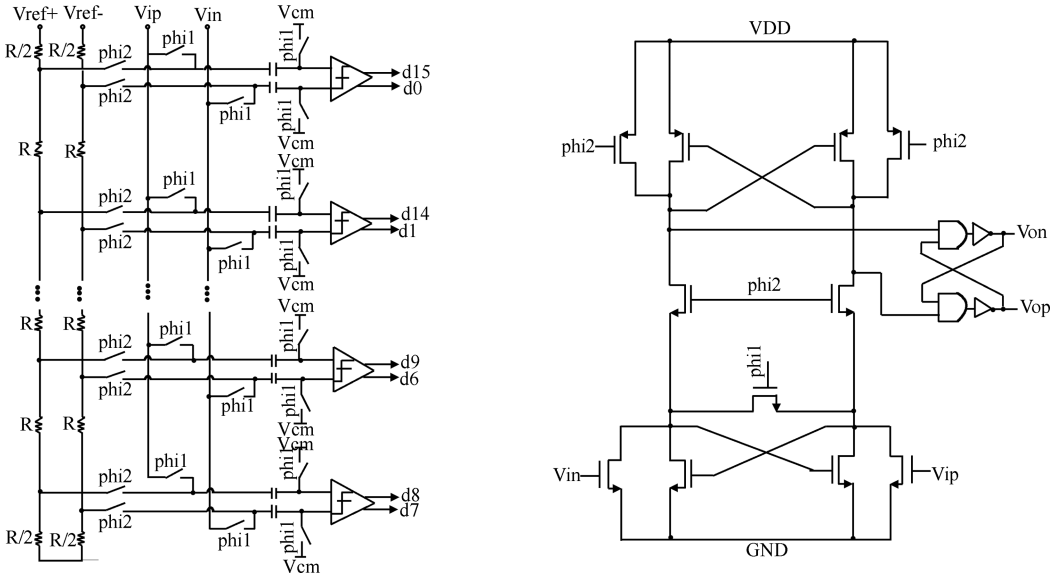

Fig. 6. 4-bit flash ADC and the comparator circuit.

input	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
4																*p*
5												*p*				
9							*p*									
3														*p*		
12											*p*					

Fig. 7. Mechanism of DWA.

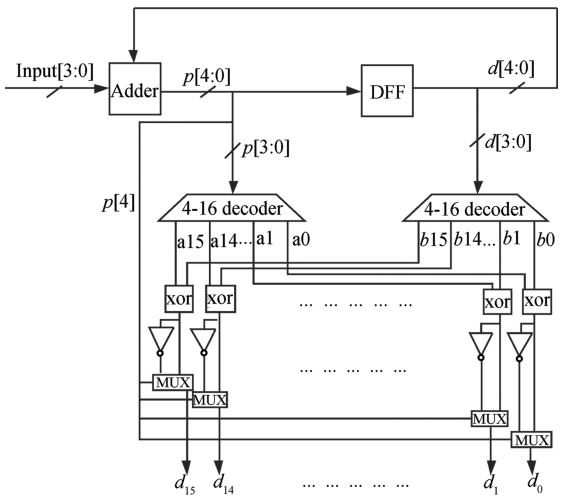

Fig. 8. IMD measurement setup.

non-linearity of the comparators, especially the ones used in the second stage, because their effects are attenuated in the base-band by noise shaping[12, 13]. However, in the layout design, attention should also be paid to factors such as matching the input transistors and distributing the capacitors reasonably[14]. The 4-bit DACs used in the modulator have a capacitor mismatch noise which limits the linearity of the overall converter. This non-linearity induces harmonic distortion in the output spectrum and therefore decreases the SFDR and the accuracy of the converter. There are several main DEM methods to realize this linearity enhancement, such as individual level aver-

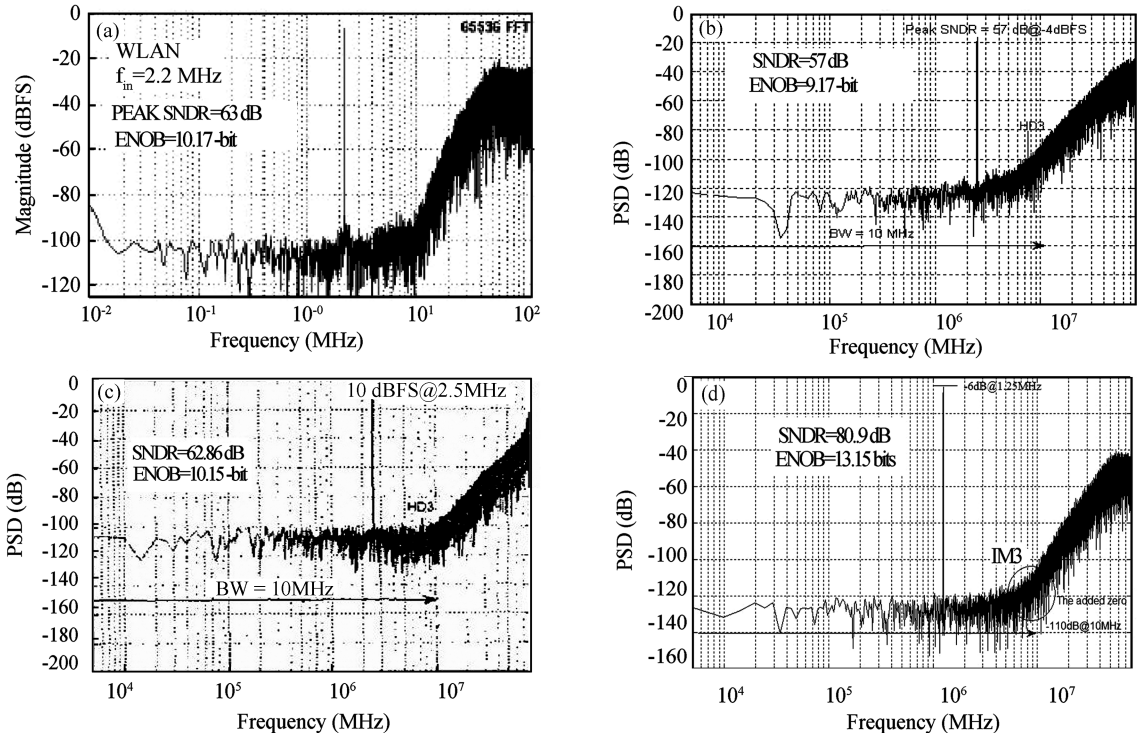

Fig. 9. Output power spectral density of (a) Ref. [6], (b) Ref. [7], (c) Ref. [8], and (d) this work.

aging (ILA), clock averaging (CLA), randomization, and data weighted averaging (DWA)[15–18]. In these algorithms, however, the DWA algorithm, using elements at the maximum possible rate to ensure that the DAC errors are minimized over the signal band and that the distortion is moved to high frequencies, is the simplest and is also adequate for multi-bit DAC linearization in sigma–delta ADCs.

Figure 7 shows an example of the DWA mechanism used in this paper. There are 16 capacitors in the 4-bit DAC, and the algorithm selects these capacitor elements clockwise in the digital-to-analog conversion. The symbol p stands for the starting point and $p \in [0, 16]$. For example, when the input code is 4 for the first D/A conversion period, four capacitors C_0,C_1,C_2,C_3 are chosen and the pointer p is set to point to C_4. Then, five capacitors C_4–C_8 are chosen in the next conversion period when the input code is 5 and p is set to point to C_9; attention should be paid that, when the input code is 9, nine capacitors C_9–C_{15} and C_0, C_1 are chosen to meet the selection clockwise mechanism of the DWA. Mathematically, the original analog signal is interpreted correctly and maintained in the output of the DAC; however, the mismatch noise of the capacitors is first-order shaped over a sufficiently long period as[19]

$$E(z) = \sum_{i=0}^{p(z)-1} \frac{\Delta C_i}{E(C_i)} - z^{-1} \sum_{i=0}^{p(z)-1} \frac{\Delta C_i}{E(C_i)}$$

$$= (1 - z^{-1}) \sum_{i=0}^{p(z)-1} \frac{\Delta C_i}{E(C_i)}, \tag{9}$$

where ΔC_i is the difference between C_i and $E(C_i)$—the mean value of the capacitors chosen in the corresponding period, and term $\sum_{i=0}^{p(z)-1} \frac{\Delta C_i}{E(C_i)}$ is called the integral mismatch. Figure 8 shows the control logic implementation of the DWA algorithm.

4. Experimental results

The improved MASH2-2 cascaded sigma–delta modulator has been fabricated by TSMC 0.18 μm technology and operates at a single 1.8 V voltage. In practice, the main non-idealities include switched-capacitor KT/C noise, input sampling clock jitter, amplifier thermal noise, amplifier slew-rate, amplifier finite bandwidth, amplifier dc gain, integrator gain capacitor mismatch, integrator output saturation, and 4-bit DAC non-linearity. In these non-idealities, some influence the SNDR of the modulator and the others influence not only the SNDR but also the SFDR and the total harmonic distortion (THD). However, these non-idealities have been considered in the systematic design; therefore, as long as the devices in the circuits operate in the determined frame, the requirements of the ADC will be met[20, 21]. The experimental result of the modulator in this work is shown in Fig. 9(d). The SNDR of this work is slightly higher than 80 dB @ –6 dBFS in a bandwidth of 10 MHz, which is 17 dB higher than that of Ref. [6] (Fig. 9(a)), 23 dB than that of Ref. [7] (Fig. 9(b)), and 18 dB than that of Ref. [8] (Fig. 9(c)). The corresponding effective number of bits (ENOB) is 13.15 bits, which is 3 bits higher than Refs. [6, 8] and 4 bit higher than Ref. [7]. Since a 4-bit ADC and the DWA for a 4-bit DAC are used in the improved version, this work has a much better performance than Ref. [6] which employs 1.5-bit ADCs (Fig. 9(a)). The added zero presented in Fig. 9(d) makes the noise floor nearly –115 dB at 10 MHz, while it is –100 dB at 10 MHz in Refs. [7, 8]. Figure 10 shows the SNDR versus the input amplitude. There are

Table 2. Performance comparison between Refs. [6–8] and the improved version.

Modulator architecture	MASH($2_{1.5b}$-$2_{1.5b}$) in Ref. [6]	MASH (2_{1b}-2_{4b}) in Ref. [7]	MASH (2_{4b}-2_{4b}) in Ref. [8]	Proposed improved MASH (2_{4b}-2_{4b}) with DWA
Signal bandwidth (MHz)	10	10	10	10
Sampling frequency (MHz)	240	160	160	160
Peak SNDR (dB)	63 @ –6 dBFS	57 @ –4 dBFS	62.86 @ –6 dBFS	80.9 @ –6 dBFS
ENOB (bit)	10.17	9.17	10.15	13.15
Peak SFDR (dB)	77 @ –6 dBFS	66 @ –6 dBFS	82.2 @ –6 dBFS	87 @ –6 dBFS
IMD_3 (dB)	–85	–65	–77.5	–93
Process technology	1.2 V 0.13 μm CMOS	1.8 V 0.18 μm CMOS	1.8 V 0.18 μm CMOS	1.8 V 0.18 μm CMOS
Power dissipation (mW)	20.5	42	42	39

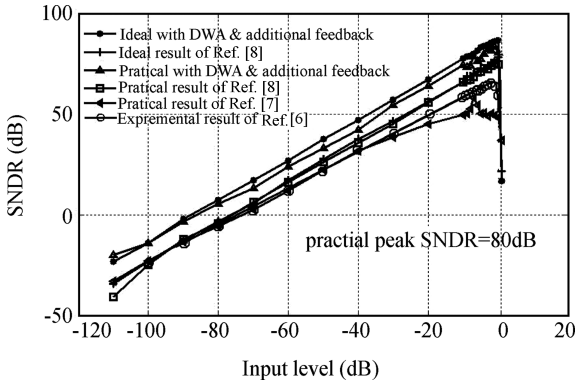

Fig. 10. SNDR versus the input amplitude.

six curves which represent the performance of Refs. [6–8] and the improved version. With DWA enabled and the additional feedback factor, the practical peak SNDR of this work is 80.9 dB, which can be observed by the two curves in the upper side of Fig. 10. Table 2 shows a performance comparison between Refs. [6–8] and this design.

5. Conclusions

An improved highly linear sigma–delta ADC is designed for WLAN applications. Experimental results show that this modulator achieves an SNDR of 80.9 dB over a 10 MHz bandwidth, an SFDR of 87 dB @ –6 dBFS and a HD3 (third harmonic distortion) of –93 dB. By adding a feedback factor in the second stage, employing two 4-bit ADCs and DWA technology for the multi-bit DACs, the SNDR increases by nearly 23 dB dynamic range compared to Ref. [7] and 17 dB compared to Refs. [6, 8]. The proposed modulator has been designed in TSMC 0.18 μm CMOS technology and operates at a 1.8 V supply voltage. The dissipation of the whole modulator is 39 mW and the die area is 0.64 mm^2.

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