High linearity 5.2-GHz power amplifier MMIC using CPW structure technology with a linearizer circuit

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Abstract: A built-in linearizer was applied to improve the linearity in a 5.2-GHz power amplifier microwave monolithic integrated circuit (MMIC), which was undertaken with 0.15-μm AlGaAs/InGaAs D-mode PHEMT technology. The power amplifier (PA) was studied taking into account the linearizer circuit and the coplanar waveguide (CPW) structures. Based on these technologies, the power amplifier, which has a chip size of 1.44 × 1.10 mm^2, obtained an output power of 13.3 dBm and a power gain of 14 dB in the saturation region. An input third-order intercept point (IIP_3) of –3 dBm, an output third-order intercept point (OIP_3) of 21.1 dBm and a power added efficiency (PAE) of 22% were attained, respectively. Finally, the overall power characterization exhibited high gain and high linearity, which illustrates that the power amplifier has a compact circuit size and exhibits favorable RF characteristics. This power circuit demonstrated high RF characterization and could be used for microwave power circuit applications at 5.2 GHz.

Key words: power amplifier; linearizer; MMIC; CPW
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1. Introduction

In communication applications, ISM (industrial, scientific and medical) band communication systems have been widely investigated in recent years. Coplanar waveguide MMIC power amplifiers are usually adopted in the transmitter communication system[1−3]. Several researchers (Muraguchi *et al*. in 1984, Liu *et al*. in 2006) have reported that microwave monolithic integrated circuits with CPW were adopted in the transmitter communication system. Broadly speaking, many advantages have been obtained in this CPW schematic layout, such as unnecessary back-side fabrication, good electronic isolation property and compact drawing in the circuit layout[3, 4]. In other words, the CPW MMIC can not only reduce the chip size by eliminating discrete components, but also degrade the parasitic effect of the wire-bonding issue.

Generally speaking, an amplifier circuit consists of an active FET device and matching circuit in the MMIC, which exhibits favorable RF characteristics. The function factors of RF, such as low insertion loss, high efficiency, high power and high linearity, are critically important characteristics in power amplifier MMICs. The linearity performance of RF characterization was likely limited by passive devices, e.g., matching inductors, MIM capacitors and resistors. Indeed, the linearity and efficiency of characterization is a trade-off issue in the power amplifier. Some literature is available on power amplifiers; however, information on the linearity effect in power amplifiers is limited[5]. Clearly, the linearity effect of power amplifiers is a topic that should be considered. Consequently, the purpose of this paper is to investigate a power amplifier MMIC associated with CPW structure by using a built-in linearizer circuit configuration, which improves the linearity effect of the power amplifier.

For the objective to be achieved, the circuit was designed as follows. First, the power amplifier used a cascade architecture, which consisted of a driver-stage and power-stage in a two-stage circuit. The work was designed to simulate the S-parameters of the power amplifier by the advanced design system (ADS) operating at a frequency of 5.2 GHz, which is the one most frequently used in current commercial wireless communication systems[6, 7]. The amplifier was designed to fully match the input and output impedance of 50 Ω without any external circuit. The power amplifier was then fabricated and the S-parameters were measured by a vector network analyzer. Finally, the results obtained from the measured S-parameters demonstrated the fabrication of the power amplifier at 5.2 GHz, which is appropriate for microwave power integrated circuits.

2. Operation principle of the built-in linearizer

It is fairly obvious that PA characterization usually exhibits gain compression at high power levels, which leads to signal distortion. Figure 1 shows that the linearizer has a gain expansion characteristic to compensate for the gain compression and to extend the linear output power region of the amplifier[8].

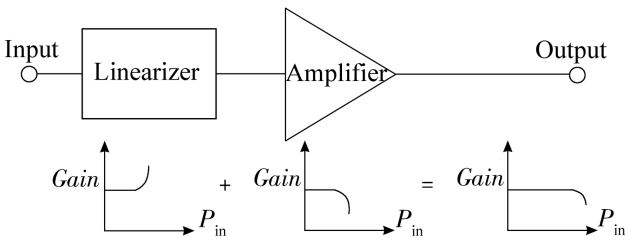

Fig. 1. Operation principle of linearization.

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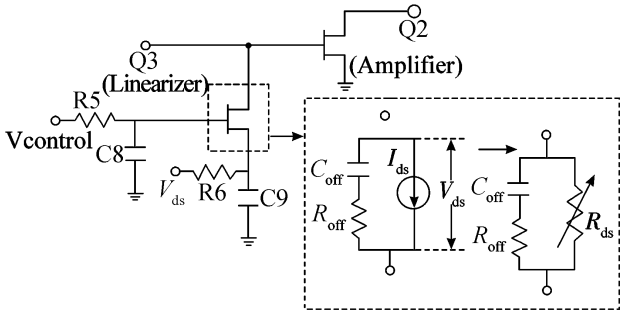

Fig. 2. Equivalent circuit model of the built-in linearizer with amplification.

A schematic and a simplified equivalent circuit model of this built-in linearizer are shown in Fig. 2. The core part of the linearizer circuit consisted of a PHEMT (Q3) linearizer, two bias-feed resistors (R5, R6), and two bypass capacitors (C8, C9). The Q2 PHEMT was the amplification stage transistor. The Q3 PHEMT for linearizer applications was expressed as the parallel combination of a capacitor series with a small resistor and a current source[9]. In FET operation, the Q3 PHEMT linearizer could be applied in the resistive region, which was biased near a zero drain–source voltage (V_{ds}) and gate–source voltage control ($V_{control}$). The slope of the DC I_{ds}–V_{ds} curve was fixed in the linear region, in which the linearizer acted as a resistor with a constant value. When the input power was increased, the swing area of the dynamic load line approached the nonlinear region, which resulted in an increased drain–source resistor (R_{ds}). In other words, the Q3 PHEMT should have a positive gain-expansion characteristic at large-signal operation, which compensates for the compression of the amplifier. Moreover, for different input power levels, the drain–source resistor (R_{ds}) variation was significantly larger than the variations of C_{off} and R_{off}[9]. Therefore, C_{off} and R_{off} for the Q3 PHEMT linearizer were assumed to be constants in this linearizer. Therefore, the drain–source resistor (R_{ds}) was the critical parameter of the linearizer, which generates the gain-expansion characteristic. This gain-expansion characteristic could be used to compensate for the gain compression of the power amplifier in the nonlinear region. Consequently, it was necessary that the variable resistor (R_{ds}) component with the equivalent circuit model of the built-in linearizer was closely related to the RF input power, and was increased along with the RF input power. Thus, the built-in linearizer could have contributed to the attainment of a gain-expansion characteristic for high linearity power amplifier applications.

3. Design and simulation of the CPW with linearizer PA MMIC

The power amplifier was achieved by a cascade architecture, which consisted of a driver-stage of class A and a power-stage of class AB, as shown in Fig. 3. Furthermore, the schematic of the PA was carried out with matching networks associated with the linearizer circuit. To be more accurate, Figure 3 also indicates that the matching circuit networks were performed with three-stage matching circuits, which contain the input port, inter-stage and output port. Considering the matching impedance, the PA was applied the two-stage single-ended amplifier in order to fully match the impedance of 50 Ω.

To begin with, the output matching network was designed for the maximum output power and power associated high efficiency in the 50 Ω impedance system. The output matching network was designed according to the power contour to achieve the maximum RF output power. Meanwhile, the HEMT device was operated at AB class in the output matching network, which was biased by $V_{ds} = 4$ V and $V_{gs} = -0.8$ V. Then, the linearizer circuit was presented in the inter-stage, which enhanced the linearity effect of the power amplifier. After this, the inter-stage network was optimized to reduce the mis-matching loss in the PA circuit. This stage matched the output of the driver stage into the input of the output-power stage. During the input network matching, the HEMT device was operated at A class, which was biased by $V_{ds} = 4$ V and $V_{gs} = -0.5$ V. Finally, we designed the input network matching to achieve a maximum small-signal gain and to improve the impedance matching for the proper input return loss; the input matching network was simply conjugate matched for maximum gain. Moreover, the PA circuit was executed to ensure enough power to drive the output-power stage and to allow fabrication variation. The PA circuit was designed with a conservative device-drive ratio, namely, 1 : 4. To put it clearly, the gate width of the PHEMT device configuration was designed in the input and output networks with the 0.15 μm AlGaAs/InGaAs depletion mode, which used 75 μm × 2 fingers and 150 μm × 4 fingers, respectively. In addition, the linearizer circuit used 75 μm × 4 fingers.

Furthermore, stability was an important consideration in the amplifier design. However, the instability issue resulted from micro-strip discontinuities and the electromagnetic (EM) effect in the power circuit. It was also likely caused by the coupling of various components at high frequency, at which all passive components were evaluated by an EM field simulator[5]. Therefore, circuit stability analysis was carried out for each stage in order to ensure a sufficient margin at 5.2 GHz. This PA circuit also adjusted the gate resistors of each stage to improve the circuit stability in the CPW power amplifier[6]. In addition, the CPW gap was designed with a narrow size, which could reduce the excitation wave of parallel-plate modes[7] and eliminate the discontinuous micro-strip effect. The capacitors and resistive loading were used to prevent oscillations at low frequency. Eventually, the stability factor of the amplifier was achieved to fulfill unconditional stability at 5.2 GHz. Consequently, circuit parameter optimization and EM simulation based on these essential matching networks were performed, so as to achieve the required circuit performance.

To achieve a favorable characterization, the S-parameters and power gain of the PA circuit were simulated by the advanced design system (ADS). Figures 4(a) and 4(b) illustrate an input return loss (S_{11}) of 12.8 dB and an output return loss (S_{22}) of 20.8 dB at 5.2 GHz with a signal gain (S_{21}) of 26.4 dB, respectively. Figure 5 indicates the simulated output power, gain and power added efficiency (PAE) at $V_{ds} = 4$ V and 5.2 GHz. It also shows that the 1 dB compression power points (P_{1dB}) at the input and output were −4 dBm and 20.4 dBm, respectively. The power of this amplifier reached about 23.5 dBm in the saturation region, with a maximum PAE of 30.6%, as also depicted in Fig. 5.

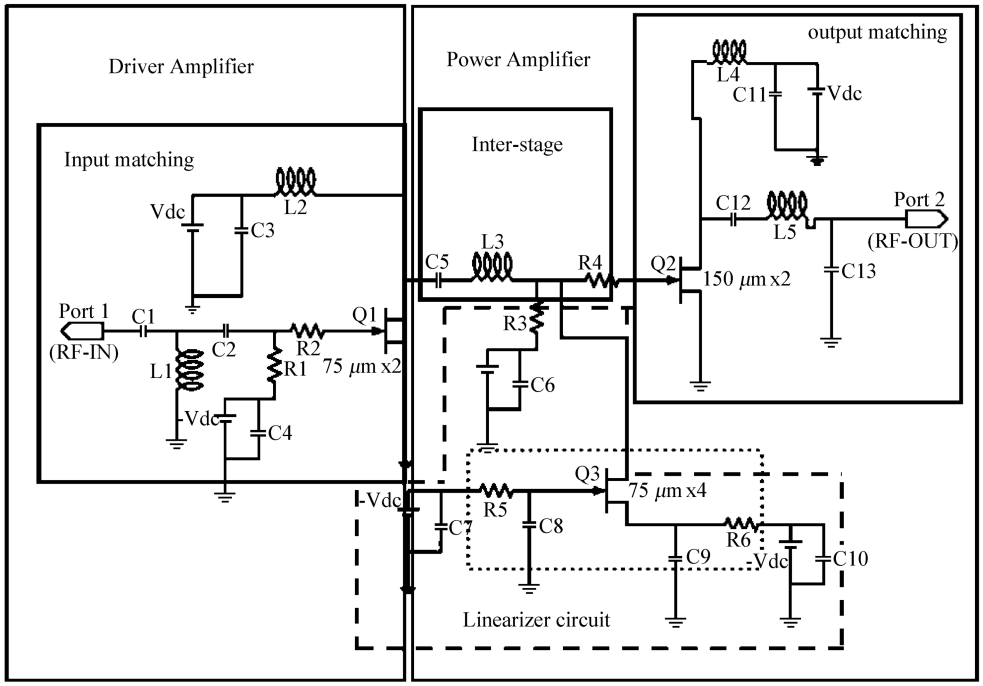

Fig. 3. Schematic of the PA-contained matching networks associated with the linearizer circuit.

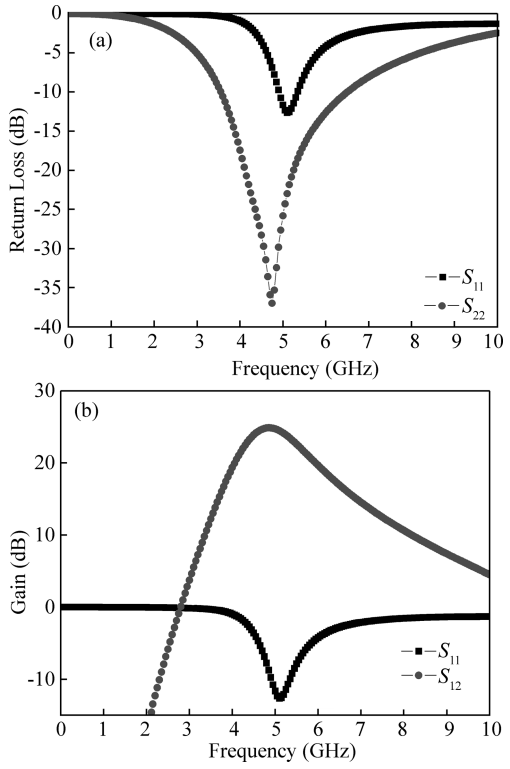

Fig. 4. Simulated S-parameters of the power amplifier at 5.2 GHz. (a) Input return loss S_{11} and output return loss S_{22} (b) Signal gain S_{21}.

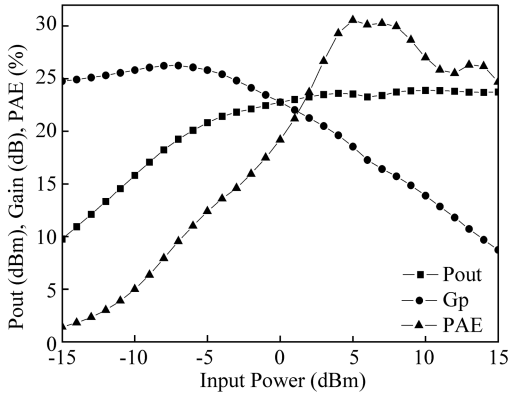

Fig. 5. Simulated output power, gain and power added efficiency of the power amplifier at 5.2 GHz.

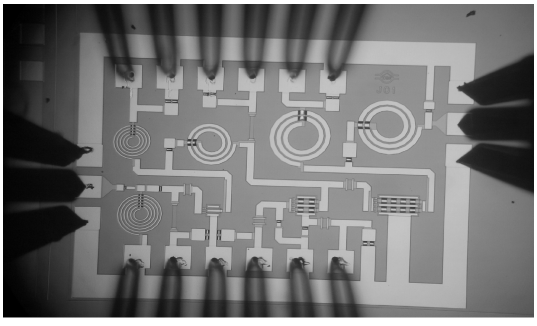

Fig. 6. Microphotograph of the power amplifier with a chip size of 1.44×1.10 mm^2.

4. Power measured results and discussion of CPW linearizer PA MMIC

The two-stage power amplifier MMIC was realized with 0.15 μm AlGaAs/InGaAs depletion mode technology. A microphotograph of the two-stage built-in linearizer CPW PA MMIC with a chip area of 1.44×1.10 mm^2 is depicted in Fig. 6.

The measurement of the S-parameters was performed by an Agilent 8510C vector network analyzer. Figure 7 illustrates

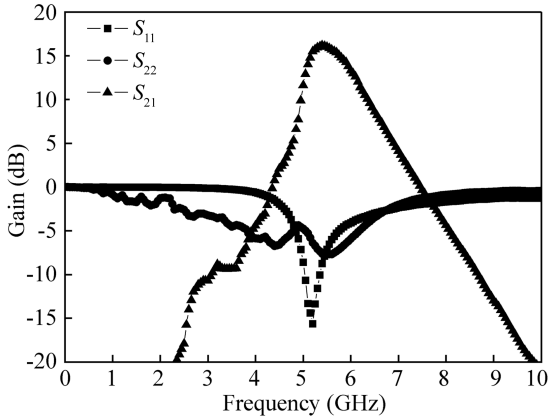

Fig. 7. Measured S-parameters of the power amplifier at 5.2 GHz.

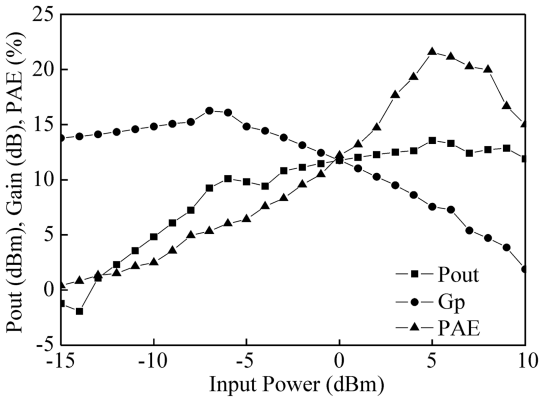

Fig. 8. Measured output power, gain and power added efficiency of the power amplifier at 5.2 GHz.

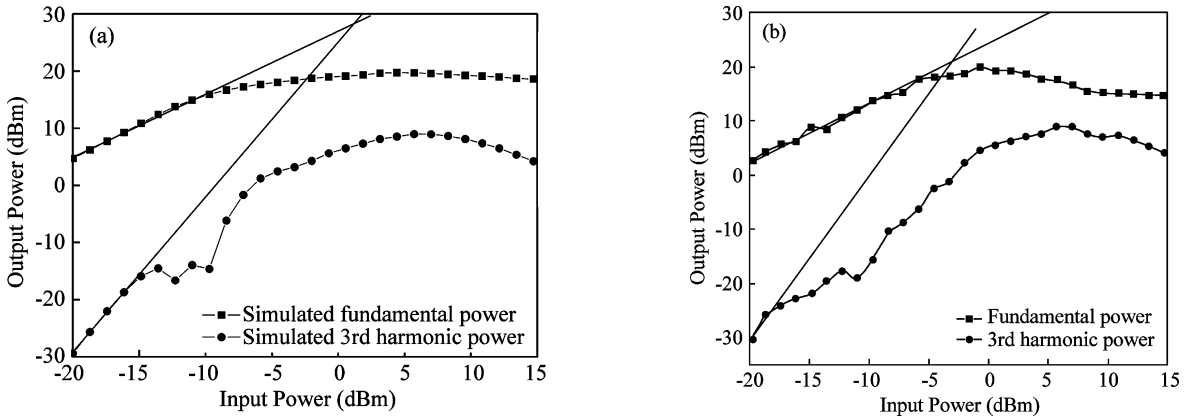

Fig. 9. Simulated and measured IP_3 of the power amplifier at 5.2 GHz. (a) The simulated third-order intercept point. (b) The measured third-order intercept point.

Table 1. RF characterization comparisons of the simulation and the measurement.

5.2 GHz CPW with linearizer power amplifier	Simulated	Measured
I/P return loss S_{11}(dB)	−12.8	−15.6
O/P return loss S_{22}(dB)	−20.8	−6.36
Insertion gain S_{21}(dB)	26.4	15.5
O/P power gain (dB)	26	14
O/P P_{1dB}(dBm)	20.4	10.2
O/P power @ saturation region (dBm)	23.5	13.3
OIP_3 (dBm)	27.5	21.1
IIP_3 (dBm)	1.5	−3.0
PAE (%)	30.6	22

the signal gain (S_{21}) of 15 dB, the input return loss (S_{11}) of 15 dB and the output return loss (S_{22}) of 6 dB at 5.2 GHz, respectively. In the power measurement, Figure 8 depicts the on-wafer measured output power, gain and PAE at V_{ds} = 4 V and 5.2 GHz. P_{1dB} was attained with about 10.2 dBm, the saturation output power was achieved with 13.3 dBm, and the maximum PAE of 21.1% was obtained at P_{in} = 5 dBm, respectively.

Furthermore, it is interesting to note the third intercept inter-modulation (IP_3), which could describe the specificity index of the circuit's dynamic range. In other words, the input signal was fed to two tones in the amplifier, and it would produce fundamental power and high order harmonic power inter-modulation products. Hence, two-tone evaluation was performed at frequencies of 5.2 GHz and 5.201 GHz, which were mixed to produce inter-modulation products in the power amplifier. Figure 9 illustrates the comparison of the simulated and measured IP_3. Figure 9(a) shows the simulated input third-order intercept point (IIP_3) of 1.5 dBm and the output third-order intercept point (OIP_3) of 27.5 dBm, respectively. The IIP_3 of −3 dBm and the OIP_3 of 21.1 dBm were also measured, as depicted in Fig. 9(b).

Table 1 illustrates the RF characterization comparisons of the simulation and measurement. Those power characterizations revealed a small inconsistency between the simulated and measured performance, which might be caused by fabrication variation and parasitic resistance. These issues are explained as follows. One explanation is that this fabrication variation results from the elimination of thinning-polish and via-hole of

backside processing, which could give rise to weak power consumption in the chip. The other is the matching circuit with additional parasitic effects in RF GSG probe pads generated from the parasitic resistances and capacitances, which could induce thermal noise. In addition, the linearizer circuit associated with the resistors might cause mis-matching in the output circuit, which could likely result in the gain compression characterization at high power levels. Regarding the poor gain issue, the authors suggest that addition of an extra buffer stage amplifier might be designed to compensate for gain compression in the output stage, as the buffer amplifier could enhance the gain characteristic. Even so, the linearity power performances were poorer than expected in the simulation.

Additionally, output return loss S_{22} was better than S_{11} in the simulation. However, S_{22} was worse than S_{11} in the measurement. The S_{22} characterization was poor and likely limited. More specifically, the polishing procedure and the formation of via holes were eliminated during backside fabrication processing, worsening the power consumption of the chip. The output matching circuit suffered from additional parasitic effects during the measurement, caused by parasitic resistances and capacitances in the RF GSG probe pads, generating thermal noise. The poor power consumption and parasitic effects substantially degraded the output return loss, which was directly related to the S_{22} characteristic in the power amplifier. Hence, output return loss S_{22} performed worse than S_{11} in the measurement. On the basis of the overall power characterization, this CPW with a linearizer PA MMIC still exhibited favorable RF characteristics at 5.2 GHz.

5. Conclusion

This article is devoted to a two-stage MMIC power amplifier using built-in linearizer and CPW topologies, consisting of a driver-stage with class A and power-stage with class AB. The power amplifier was realized with 0.15-μm AlGaAs/InGaAs D-mode PHEMT technology, and exhibited an appropriate RF performance at 5.2 GHz. The results of the simulation were obtained by an ADS simulator, which found a power gain of 26 dB associated with an output power of 23.5 dBm, and a maximum PAE of 30.6%, respectively. Finally, the characterization of the MMIC power amplifier revealed an output power of 13.3 dBm, a linear power gain of about 14 dB and an OIP_3 of 21.1 dBm. In summary, the overall power characterization exhibits high gain and linearity, with favorable RF characteristics and is very suitable for 5.2 GHz microwave integrated circuit power transmission applications.

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