Improvements to the extraction of an AlGaN/GaN HEMT small-signal model*

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Abstract: The accurate extraction of AlGaN/GaN HEMT small-signal models, which is an important step in large-signal modeling, can exactly reflect the microwave performance of the physical structure of the device. A new method of extracting the parasitic elements is presented, and an open dummy structure is introduced to obtain the parasitic capacitances. With a Schottky resistor in the gate, a new method is developed to extract R_g. In order to characterize the changes of the depletion region under various drain voltages, the drain delay factor is involved in the output conductance of the device. Compared to the traditional method, the fitting of S_{11} and S_{22} is improved, and f_T and f_{max} can be better predicted. The validity of the proposed method is verified with excellent correlation between the measured and simulated S-parameters in the range of 0.1 to 26.1 GHz.

Key words: AlGaN/GaN HEMT; small-signal model; Schottky resistor; drain delay
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1. Introduction

Developments in wireless communications have drastically increased the need for high-power, high efficiency, linear, low-cost, monolithic solid-state amplifiers in the 1–100 GHz frequency range[1−3]. The design of power amplifiers for communication systems based on AlGaN/GaN HEMT requires an accurate large-signal model. In bottom-up modeling techniques, an accurate evaluation of the equivalent small-signal model is the foundation of the large-signal model, and then an efficient method is required to extract the parasitic elements of the device for the small-signal model, which also supports the basic parameters for the noise model.

Approaches to small-signal modeling have been presented in many papers; the first detailed small-signal model extraction procedure of FETs was proposed by Dambrine *et al.*[4], and subsequent researchers developed the method according to particular materials, different device structures and more fields of application[5−8]. The difficulty lies in obtaining physically meaningful parameters and suppressing negative values according to the structure of the device. An improved method is presented in this paper: we discuss the extraction of parasitic capacitance with the open dummy method, a new method to extract R_g and the effects of the drain delay factor, which are meaningful for small-signal models of GaN HEMTs.

2. Device structure and fabrication

The layer structure of the device used in the study was grown on a semi-insulating 4H-SiC substrate. The epitaxial layer consists of a 3 μm unintentionally doped GaN buffer layer, a 1 nm AlN spacer layer, a 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and 3 nm GaN on top. The device has a 0.25 μm gate length and 140 μm (35 × 4) gate width T-shaped AlGaN/GaN HEMT. An average electron mobility of 1250 $cm^2/(V{\cdot}s)$ and a sheet carrier density of 1.4×10^{13} cm^{-2} were obtained by room-temperature Hall measurement. The AlGaN/GaN HEMT fabrication commenced with metallizing by high-vacuum evaporation in drain and source; ohmic contacts were formed by depositing the metals Ti/Al/Ti/Au followed by rapid thermal annealing (RTA) at 870 °C for 50 s in N_2 ambient. All of these steps above resulted in a low ohmic contact resistivity of $l0^{-6}\,\Omega{\cdot}cm^2$. After ion implantation, SiN film used for passivation was grown by PECVD, and a gate recess was etched using a fluorine-based and subsequent chlorine-based ICP process. Then, a T-Schottky gate was formed by Ni/Au evaporation and the subsequent lift-off process. Finally, Au air bridges were deposited by electroplating in order to connect all the source areas.

3. Extraction procedure

Based on the AlGaN/GaN HEMT device structure, an improved method is proposed to extract small-signal model parameters. Since this method is a direct extraction and not an optimization, we can obtain original values of the equivalent circuit elements which reflect the real physical meanings of the device characteristics. The complete equivalent topology is given below in Fig. 1. R_g, R_d and R_s are access resistors including ohmic contact, L_g, L_d and L_s are parasitic inductors in series with the resistors, C_{pgd}, C_{pg} and C_{pd} are parasitic pad capacitances, C_{gs}, C_{gd} are capacitances modeling the changes in the depletion region with variation of the bias voltage, while

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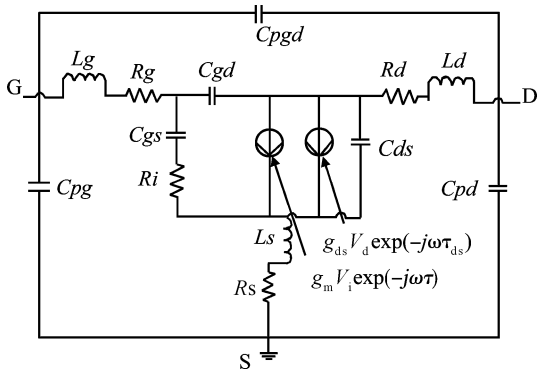

Fig. 1. Equivalent topology of AlGaN/GaN HEMTs.

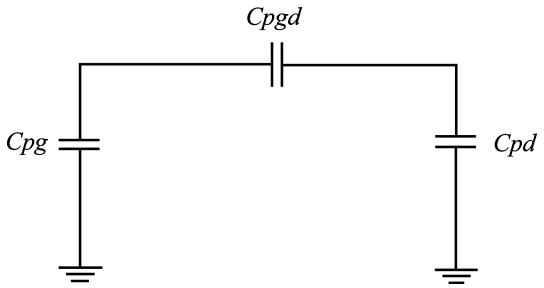

Fig. 2. Equivalent circuit of the open dummy structure.

C_{ds} is the drain source capacitance modeling the geometric capacitance effects between the drain and source electrodes, R_i is the intrinsic resistance under the gate between the channel and source, g_m is the transconductance with the delay factor τ, and g_{ds} is the output conductance with the drain delay factor τ_{ds}.

3.1. Parasitic capacitance extraction

An open dummy structure is introduced to extract the parasitic capacitances. The dummy device was fabricated on the same wafer and had the same layout structure without an active region. Figure 2 shows the equivalent circuit of the passive device; the values of the three capacitances can be solved by Eqs. (1)–(3) from the imaginary part of the Y parameters.

$$\mathrm{Im}(Y_{11}) = \omega(C_{pg} + C_{pgd}), \tag{1}$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{12}) = -\omega C_{pgd}, \tag{2}$$

$$\mathrm{Im}(Y_{22}) = \omega(C_{pd} + C_{pgd}). \tag{3}$$

3.2. Parasitic resistor and inductance extraction

The parasitic capacitances were first evaluated and de-embedded, and the next step was to extract the resistors and inductances in series. When $V_{ds} = 0$ V, $V_{gs} > V_{th}$, the channel can be equivalent to a distributed RC network and the equivalent circuit can be simplified as shown in Fig. 3. The R_{dy} and C_g are the Schottky resistor and capacitance which characterize the Schottky effects at the gate, while R_{ch} and C_{ds} account for the channel resistor and drain source capacitance. The transmission line method is used to model the region under the gate[9], and the Schottky capacitance and drain–source capacitance can be neglected in high frequency conditions, so

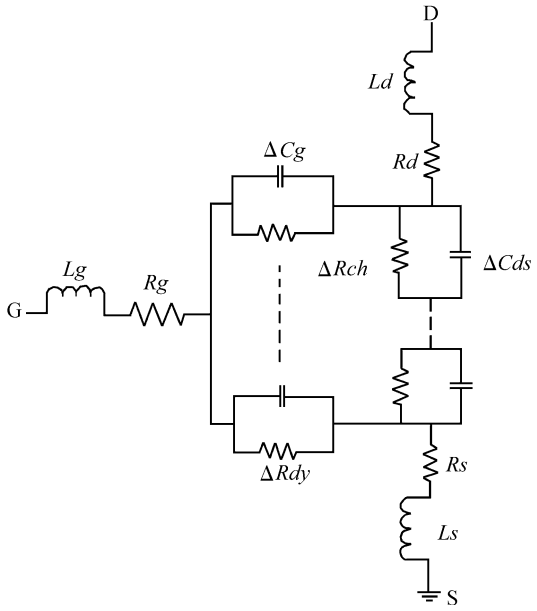

Fig. 3. Equivalent circuit with $V_{ds} = 0$ V, $V_{gs} > V_{th}$.

the simplified Z parameters of Fig. 3 are expressed as follows:

$$Z_{11} = R_s + R_g + R_{dy} + \alpha_g R_{ch} + \mathrm{j}\omega(L_s + L_g), \tag{4}$$

$$Z_{12} = Z_{21} = R_s + \alpha R_{ch} + \mathrm{j}\omega L_s, \tag{5}$$

$$Z_{22} = R_s + R_d + 2\alpha R_{ch} + \mathrm{j}\omega(L_s + L_d). \tag{6}$$

α_g and α represent the fraction of gate current flowing through the channel. For a symmetric device they always can be set to 1/3 and 1/2. A method is adopted to calculate the Schottky resistor R_{dy}. Two S parameters at $V_{ds} = 0$, $V_{gs} > 0$ are needed, and two very close V_{gs1} and V_{gs2} are chosen to make the I_{gs} smaller than 10 mA, which assures that the ideality factor is in the range of allowable error; the ideality factor can be calculated from Eq. (7). R_{dy} is then found from Eq. (8), and all the resistors and inductors can be obtained from the real and imaginary parts of the Z parameters.

$$n = \frac{\mathrm{Re}(Z_{11}^1) - \mathrm{Re}(Z_{11}^2)}{kT/(qI_g^1 - qI_g^2)}, \tag{7}$$

$$R_{dy} = \frac{nkT}{qI_g}, \tag{8}$$

where n is the ideality factor, k is the Boltzmann constant, and T is the temperature.

3.3. Intrinsic element extraction

Intrinsic element values can be determined from the measured intrinsic Y parameters of the device after de-embedding the external parasitic parameters[10]. Compared to the traditional intrinsic Y parameters, the drain delay factor τ_{ds} is introduced to characterize the time delay of g_{ds} as shown in Eq. (9). The delay of g_m is the transit time that the electrons drift the efficient length of channel. τ_{ds} is a function of drain voltage and frequency conditions, which is the time required for electrons to traverse the depletion region between the gate and drain.

Table 1. Extracted capacitances with open dummy structure.

Parameter	Value
C_{pg}	9.96 fF
C_{pd}	13.04 fF
C_{pgd}	2.34 fF

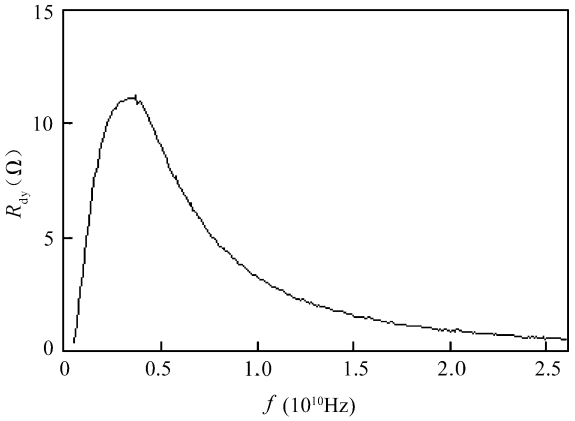

Fig. 4. Relationship between R_{dy} and frequency.

$$\begin{aligned} Y_{22} &= g_{ds}e^{-j\omega\tau_{ds}} + j\omega(C_{gd} + C_{ds}) \\ &= g_{ds}\cos\omega\tau_{ds} + j(\omega C_{gd} + \omega C_{ds} - g_{ds}\sin\omega\tau_{ds}) \\ &= g_{ds}\left[1 - \frac{(\omega\tau_{ds})^2}{2}\right] + j\omega(C_{gd} + C_{ds} - g_{ds}\tau_{ds}) \\ &\approx g_{ds} + j\omega(C_{gd} + C_{ds} - g_{ds}\tau_{ds}). \end{aligned} \tag{9}$$

τ_{ds} cannot be obtained directly, but we can get g_{ds} and τ_{ds} from the real part and imaginary part of Y_{22} with Euler's formula and limit approximation as $\omega\tau_{ds} \ll 1$.

4. Analysis and results

The traditional extraction of parasitic capacitance is based on the "cold FET" method[4, 7], but sometimes there exist negative values of C_{pg} or C_{pd}, because the equivalent capacitances in the depletion have not reach an agreement, and assumption of the gate capacitances under zero drain bias and pinch-off gate voltage may be not enough. The sequence of the extraction is another problem, and the probe in contact with the pad creates a small inductance, so L_g and L_d are de-embedded first[4] which is difficult to realize according to the measurement limit and calculation. In this paper, C_{pg} and C_{pd} are de-embedded first, and the negative capacitance reflects inductance, so the change may be the issue. The measurement uncertainty can also cause negative values. The open dummy method is a simple and efficient way to obtain the parasitic elements, which also gets rid of the negative values of capacitance to ensure extracted values with definite physical meaning. The parameter values by this method are shown in Table 1.

Accurate values of the parasitic resistors and inductors are very important, as some of them have a great effect on the results. The gate resistor R_g results from the metallization resistance of the gate Schottky contact, and the author found that accurate extraction of R_{dy} has great effects on R_g, which

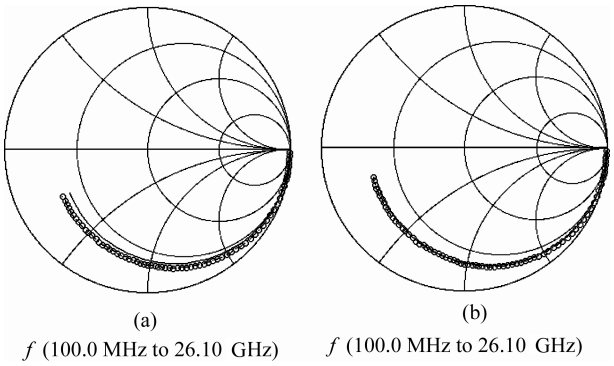

Fig. 5. Comparison fitting of S_{11} with (a) the traditional and (b) improved methods. The solid line is the simulated curve, and the circles are the measured curve.

Table 2. Extracted resistors and inductors of 4×35 μm GaN HEMT.

Parameter	Value
R_g	4.08 Ω
R_d	0.5 Ω
R_s	4.0 Ω
R_{dy}	4.5 Ω
L_g	0.02 pH
L_d	0.04 pH
L_s	0.001 pH

makes a big difference in the fitting of S_{11} as shown in Fig. 5. Due to the gate being biased at different voltages, R_{dy} shows a slight variation with different I_{gs}. R_{dy} also changes greatly with increasing frequency; it must be extracted more reasonably at the condition the transistor is working on. As displayed in Fig. 4, R_{dy} is calculated under the bias condition V_{gs} = 1.5 V, V_{ds} = 0 V, and the frequency is in the range of 0.1 to 26.1 GHz. The values of these parameters are shown in Table 2.

To increase the breakdown voltage of the device, the gate-to-drain spacing has to be increased. With increasing drain voltage, the depletion region encroaches into the gate–drain region more than confined under the physical dimensions of the gate, which reduces the gate drain capacitance but increases the transit time by adding drain delay. When the device is biased at a high drain voltage to maximize the power output, it creates a drain depletion region that is on the order of the gate length of the device, so drain delay is an important parameter for microwave power HEMTs. The drain delay represents a delay of the drain current response to the drain voltage arising from delays associated with the partially depleted high-field region, and it improves the dependence of the signal in the drain on frequency and bias voltage.

In Fig. 6, compared to the measured S_{22}, there is a phase separation in the model without τ_{ds}; sometimes this phase difference may lead to negative C_{ds}. With the phase delay of g_{ds}, it can compensate for the phase separation at high frequencies due to the depletion region extension changes. Both the delays of g_{ds} and g_m increase significantly when the drain bias is high, in the saturation region as a condition in the paper, and the drain delay τ_{ds} exceeds τ.

Table 3. Extracted intrinsic parameters of 4×35 μm GaN HEMT.

Parameter	Value
C_{gs}	0.197 pF
C_{gd}	0.074 pF
C_{ds}	0.025 pF
g_m	65.06 mS
τ	1.3 ps
R_i	1.5 Ω
g_{ds}	3.08 mS
τ_{ds}	5.62 ps

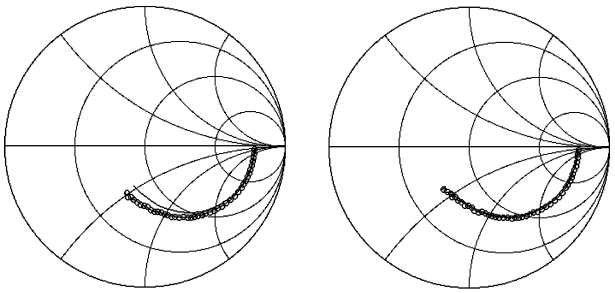

Fig. 6. Comparison fitting of S_{22} for models (a) without τ_{ds} and (b) with τ_{ds}. The solid line is the simulated curve, and the circles are the measured curve.

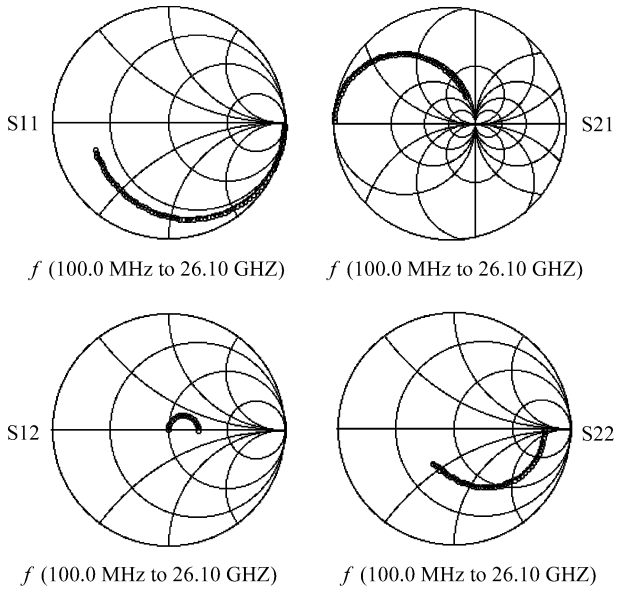

Fig. 7. Comparison between measured and simulated S parameters. The solid line is the simulated curve, and the circles are the measured curve.

With the extracted parameters shown in Table 3, the error which uses the concept introduced in Ref. [8] is 3.4%; as shown in Fig. 7, it shows a good match with the measurement. Figure 8 gives the high frequency performance of a device with 36 GHz of f_T and 58 GHz of f_{max}. Sometimes it also shows a good match with the fitting of the S parameters using the traditional method, but there is a big discrepancy in the predictions of f_T and f_{max}. Here, we can predict that f_T and f_{max} are 34.9 GHz and 56.4 GHz by Eqs. (10) and (11)[11] with the

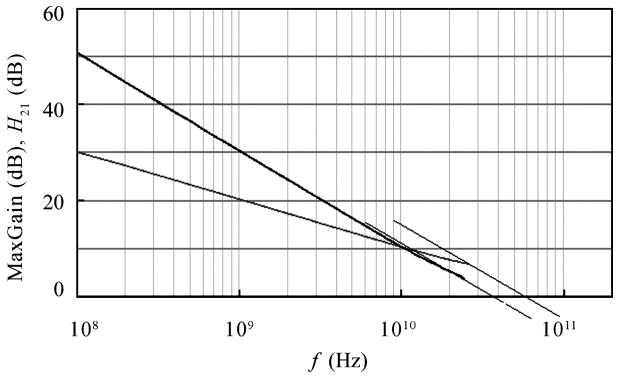

Fig. 8. High frequency performance with V_{ds} = 10 V and V_{gs} = −1.5 V.

small-signal parameters based on the improved method; this also gives good evidence for the whole extraction method.

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\left[1+\left(R_s+R_d\right)g_{ds}\right]+C_{gd}g_m\left(R_s+R_d\right)}, \tag{11}$$

$$f_{max} = \frac{f_T}{2\sqrt{\left(\left(R_g+R_i+R_s\right)g_{ds}+2\pi f_T C_{gd}R_g\right)}}. \tag{12}$$

5. Conclusion

An improved and direct small-signal parameter extraction procedure has been presented for a GaN HEMT device. The parasitic pad capacitances are extracted with the open dummy structure. The parasitic resistors and inductors are extracted under gate forward bias and zero drain voltage conditions, the accuracy of R_g which influences the value of R_i shows an important relationship with the fitting of S_{11}. In order to improve the fitting of S_{22}, the drain delay factor, which reflects a time delay at the output and a phase delay at high frequency, is introduced to model the changes of depletion with different drain voltages. The validity of this method is verified by comparing the measured and simulated S parameters, and the predictions of f_T and f_{max} with the extracted elements show a good match with the measured ones.

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