A 12-bit 40 MS/s pipelined ADC with over 80 dB SFDR

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Abstract: This paper describes a 12-bit 40 MS/s calibration-free pipelined analog-to-digital converter (ADC), which is optimized for high spurious free dynamic range (SFDR) performance and low power dissipation. With a 4.9 MHz sine wave input, the prototype ADC implemented in a 0.18-μm 1P6M CMOS process shows measured differential nonlinearity and integral nonlinearity within 0.78 and 1.32 least significant bits at the 12-bit level without any trimming or calibration. The ADC, with a total die area of 3.1 $\times$ 2.1 mm^2, demonstrates a maximum signal-to-noise distortion ratio (SNDR) and SFDR of 66.32 and 83.38 dB, respectively, at a 4.9 MHz analog input and a power consumption of 102 mW from a 1.8 V supply.

Key words: analog-to-digital converter; pipeline; spurious free dynamic range
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1. Introduction

High performance analog-to-digital converters (ADCs) are widely used in wireless communication systems, radar and digital video broadcasting. Many applications such as portable wireless communication systems always require a resolution of at least 10-bit and tens of megahertz sampling rates with low power and high spurious free dynamic range (SFDR). Up to now, the available precision of pipelined ADCs has always suffered from process mismatch. Therefore, to obtain a higher SFDR and finer resolution, a variety of analog and digital calibration techniques have been widely used in pipelined ADCs[1−6]. Unfortunately, even very novel and effective calibration techniques, which always use elaborate calibration algorithms and complicated circuit implementations, inevitably increase the power dissipation or slow down the operation speed. Indeed, high matching accuracy can be simply implemented by careful layout technique[7].

In this paper, a 1.8 V 12-bit 40 MS/s calibration-free pipelined ADC with high SFDR and low power dissipation is demonstrated. By employing common-centroid symmetric capacitor techniques in a multiplying DAC (MDAC), deep N-well substrate isolation and careful layout design, the proposed ADC achieves a high SFDR without any trimming or calibration techniques. Low power consumption is achieved by using SHA-less architecture, and optimizing the sampling capacitance size and operation transconductance amplifier (OTA) bias current.

2. ADC architecture

2.1. SHA-less front end

Traditional pipelined ADCs all consist of a sample and hold amplifier (SHA). Unfortunately, an SHA consumes a lot of energy and further introduces distortion and noise into the whole converter. In this design, we employ SHA-less architecture[8] to overcome the drawback. In the SHA-less architecture, the sample and hold circuit is integrated in the first MDAC, instead of a dedicated SHA at the front end.

The disadvantages of the SHA-less architecture have been profoundly analyzed in Refs. [8, 9]. To overcome the drawbacks, the RC parameter in the sampling networks of the sub-ADC and the MDAC of the first stage must be kept the same. Since the MDAC and the flash in the first stage of the SHA-less architecture both see the high speed analog input signal, instead of a signal held by the SHA in traditional pipelined ADCs, any mismatch between bandwidths of these two input sampling networks will result in a difference between the sampled values. In our design, the sampling switches and sampling capacitors used in the sub-ADC and the MDAC of the first stage are of the same size. Furthermore, the layout of the switches and capacitors also maintains complete symmetry. So the RC parameter in the sampling networks of the sub-ADC and the MDAC of the first stage is the same. This evidently eliminates sampling error in the two sampling networks.

Fortunately, the widely known digital error correction can rectify the error caused by bandwidth mismatch, provided that the difference does not overstep the redundancy correction range of the first pipeline stage. To achieve the maximum redundancy correction range, we adopt the well known 1.5-bit pipeline stage architecture, which can provide 200 mV redundancy correction range in our design. The measured results in

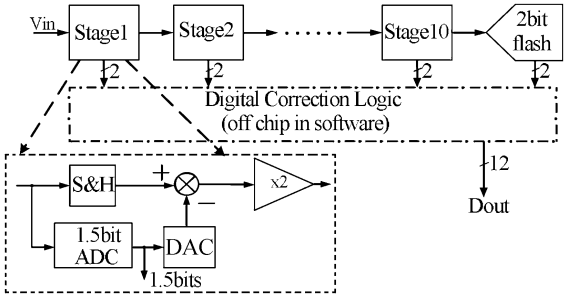

Fig. 1. Block diagram of the pipelined ADC.

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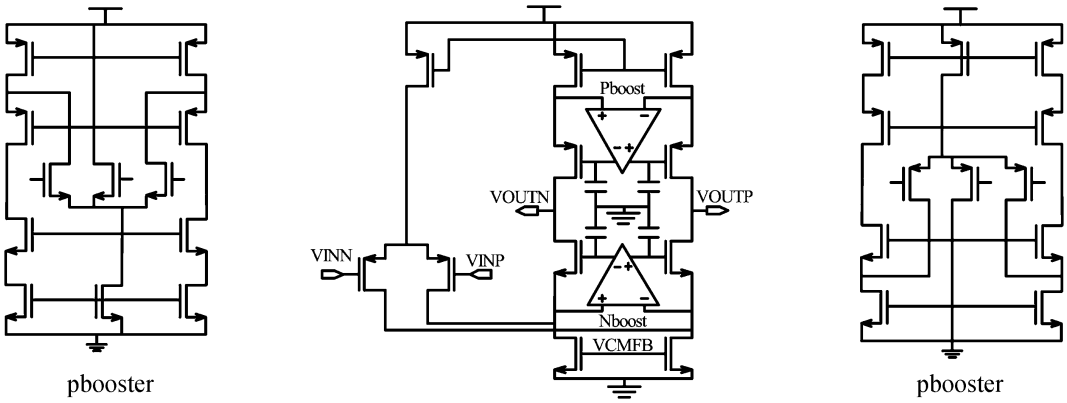

Fig. 2. Folded-cascode gain boost OTA.

Refs. [1, 8] achieve over 100 dB SFDR, which demonstrates the feasibility of the SHA-less architecture for high sampling rate ADCs.

Considering the above reasons, we propose a 12-bit 40 MS/s CMOS pipelined ADC that consists of ten 1.5-bit stages and a 2-bit flash ADC as illustrated in Fig. 1. The 1.5-bit pipeline stage architecture is well known; it is composed of a flash 1.5-bit sub-ADC with two comparators and an MDAC that generates the analog residue signal for the following stages.

2.2. Stage scaling

Most of the power in a pipelined ADC is consumed by the OTA, which is used in the MDAC to generate the analog residue signal for the following stages. So the stage scaling methodology[1] is used in this design to decrease power consumption by optimizing the size of the sampling capacitance and current of the OTA. To achieve 12-bit precision in the pipelined ADC, the size of every stage sampling capacitance is limited by process mismatch and noise. As pointed out in Fig. 1, along the analog residue signal flow through stage 1 to stage 10, signal accuracy and capacitance match demand decrease. So we can design the OTA by the capacitance load and setting precision to decrease the power. The sample and hold capacitance of the first stage should keep at least 12-bit precision; the latter stage can be relaxed by 1-bit. We can decide the size of the capacitance according to the process manual and the KT/C noise. In this design, the input sampling capacitance is 2.5 pF in the first stage considering 12-bit precision level thermal noise and process mismatch. According to Ref. [1], we should design separate OTAs for every stage to cut down the power consumption budget. However, this increases the layout work load, so in this design three different OTAs are used. The power dissipation can be further reduced by adopting more scaled OTAs.

3. Circuit implementation

3.1. Amplifier for the MDAC

The OTA, which is one of the most important components in a pipelined ADC, consumes most of the power and has an important impact on the analog residue signal precision. The most critical OTA is the one that is used in the first stage of the pipeline because it has to settle within at least 12-bit accuracy in less than half a clock cycle. Since the size of capacitance decreases along the stages, the load of the OTA also decreases. So we can design the OTAs according to the capacitance load and settling precision requirement to decrease the power. To reduce the layout work, this design employs three different OTAs. We can further decrease power dissipation by designing more scaled OTAs. The structure of the OTA is a folded cascode gain-boost, which provides high gain, fast settling time and low power at a low supply voltage, as shown in Fig. 2. The simulation result shows an output 1.6 Vp-p swing and a 90 dB gain with 600 MHz gain-bandwidth (GBW) for the OTA at 1.8 V power supply under suitable load.

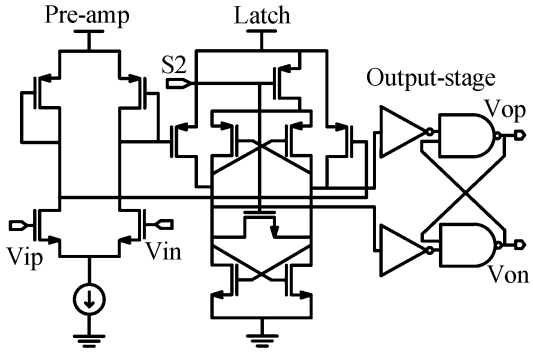

Fig. 3. Structure of the comparator.

3.2. The comparator design

The 1.5-bit sub-ADC used in every pipeline stage consists of two fully differential comparators. The comparator, as shown in Fig. 3, has three stages: pre-amplifier, latch and output stage. To prevent kick-back noise, we employ the pre-amplifier architecture. The pre-amplifier does not need very high gain to decrease the kick-back noise, so the bias current of the pre-amplifier is only 50 μA to decrease the static power. The latch stage gives comparison results on the falling edge of decision clock S2. The output stage employs RS flip-flop architecture. The threshold voltages of the two comparators in the 1.5-bit sub-ADC are set to be $-V_{\rm ref}/4$ and $+V_{\rm ref}/4$ respectively. The digital error correction logic at the output of the pipeline stages can correct comparator errors up to $V_{\rm ref}/4$ in the 1.5-bit

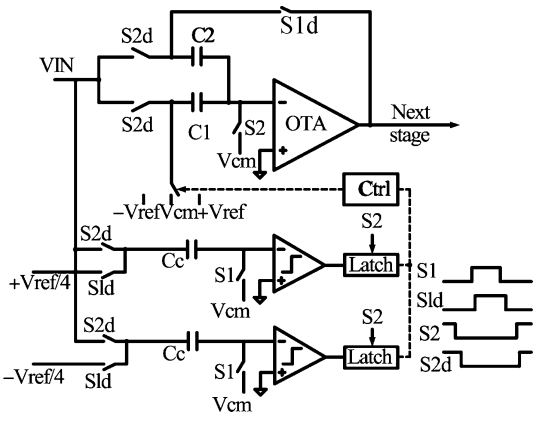

Fig. 4. The first stage of the ADC.

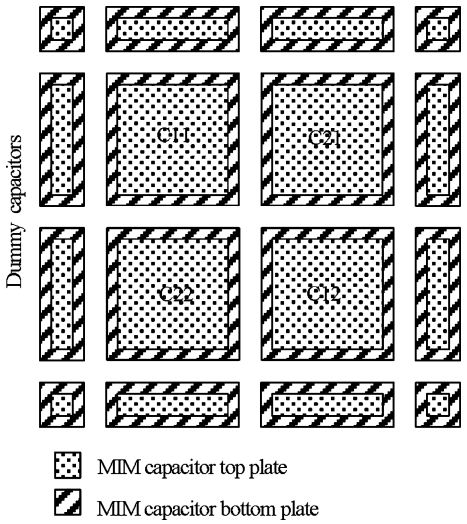

Fig. 5. Proposed fully symmetric MDAC capacitors.

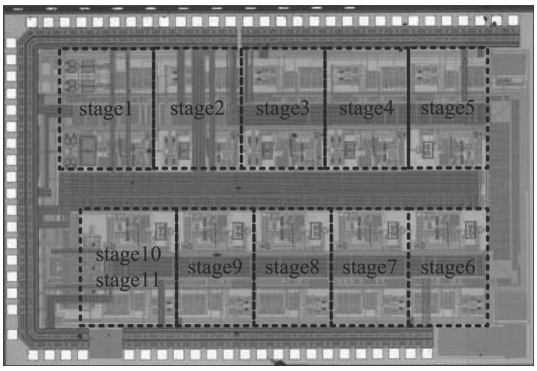

Fig. 6. Die photograph of the prototype ADC.

pipeline stage, so the comparators do not need to be of very high accuracy.

3.3. The first stage architecture

The detailed architecture of the first stage is shown in Fig. 4. A conventional bootstrap switch[10] is employed to linearize the sampling switch and to minimize the nonlinear distortion of sampled inputs due to switch on resistance variations at low power-supply voltage. A single ended version is shown in Fig. 4 for simplicity and the circuit is fully differential in reality. When the S1d controlled switches are turned off and the S2d controlled ones are turned on, the first stage is in sample phase and the second one in amplification phase. At the same time, the input analog signal is sampled by the C1, C2 and Cc. When the S1d controlled switches are turned on and the S2d controlled ones are turned off, the first stage is in amplification phase and the second stage is in sample phase. Meanwhile, the comparator compares VIN with reference voltages $+V_{\rm ref}/4$ and $-V_{\rm ref}/4$. In this clock phase, C2 is crossed over the OTA to realize the amplification of the VIN 2 times and its combining with the reference voltage add or reduction functions. The analog output signal is sampled by the second stage at the falling edge of S1. As a result of the SHA-less technique, we need to keep their RC time constant values the same and maintain the layout symmetry, to reduce the sampling path mismatch between the operational amplifier and the comparator.

3.4. Symmetric capacitor layout of the MDAC

The capacitor mismatch of the MDAC is critical to the pipelined ADC static and dynamic performances and is caused primarily by process variations. Various calibration techniques have been invented to overcome the capacitor mismatch of high resolution pipelined ADCs. However, every calibration technique consumes more power or slows down the ADC sampling rate, since they inevitably have to add extra circuits or timing cycles to the converter. Actually, the high capacitor matching accuracy can be achieved simply by appropriate layout techniques[7].

To achieve satisfactory SFDR performance, the capacitor C1 and C2 in Fig. 4 must be highly matched, so we adopt common-centroid symmetric capacitor layout techniques in our design. The proposed common-centroid symmetric capacitor layout techniques are illustrated in Fig. 5 and the capacitance used in this chip is a metal–insulator–metal (MIM) structure capacitor provided by the foundry. For realizing common-centroid placement, the capacitor C1 in Fig. 4 is divided into two parts, C11 and C12. Similarly, the capacitor C2 is also composed of C21 and C22. To minimize the capacitor mismatch, every unit capacitor is enclosed by another capacitor, dummy and metal, so each capacitor has an identical environment and parasitic capacitance.

3.5. Layout consideration

It is well known that layout is very important in mixed signal systems and the layout details determine the overall ADC converter performance. So several careful layout techniques are used through the design to guarantee high dynamic performance, including substrate isolation, noise shielding, power decoupling and so on.

The prototype ADC is fabricated in a 0.18-μm single-poly six-metal CMOS process with a MIM capacitor and deep N-well as shown in Fig. 6. In Fig. 6, the first stage can be seen at the front of the chip. The latter stage is placed next to the other to minimize the parasitic capacitance of the critical node. Stage 6 is turned around and is placed at the bottom of the chip. So the lengths of reference lines and power lines are just half and IR drops in power lines and ground lines are minimized.

Analog circuits in mixed signal circuits have always suf-

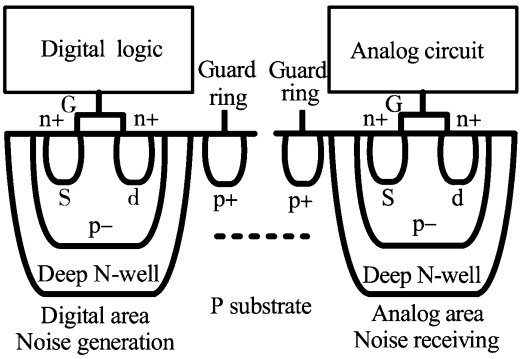

Fig. 7. Cross section of the proposed ADC with deep N-well and p^+ guard ring.

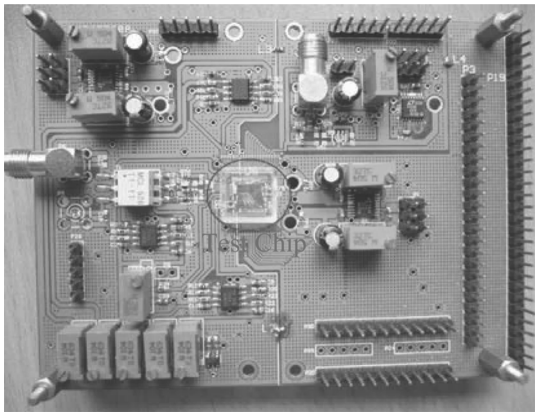

Fig. 8. The experimental PCB.

fered from digital circuit noise. In this design, we use a separate deep N-well provided by the foundry to isolate the analog circuit and the digital part, as shown in Fig. 7. All of the NMOS, both analog and digital, are implemented in the separate deep N-well, so the analog ground and the digital ground are physically completely isolated and there is no current flowing through the substrate. The noise coupled by the substrate from the digital part, which is very harmful to the analog circuit in a traditional chip, is eliminated. Although the analog ground and digital ground are physically isolated by the separate deep N-well, the analog circuit is also surrounded by several ground guard rings which are directly connected to one of the analog ground PADs for further isolation.

IR drops in power lines and ground lines in the chip are crucial to the performance of the whole ADC converter, so the digital and analog blocks use several separate power lines and ground lines to suppress digital noise. Furthermore, dummy ground is placed around every sensitive signal to providing shielding from noise. To reduce the resistance of the analog power lines, the lines are stacked from metal 2 to metal 6, with the width of 240 μm in parallel. The analog ground lines surround the analog part and are also stacked with several metal layers of hundreds of microns in parallel. In order to minimize power supply bounce and deliver more stable power lines, 2.5 nF and 1.3 nF decouple capacitors are added to the analog and digital supplies on the chip respectively. The decouple capacitors implemented by separate deep N-well NMOS devices

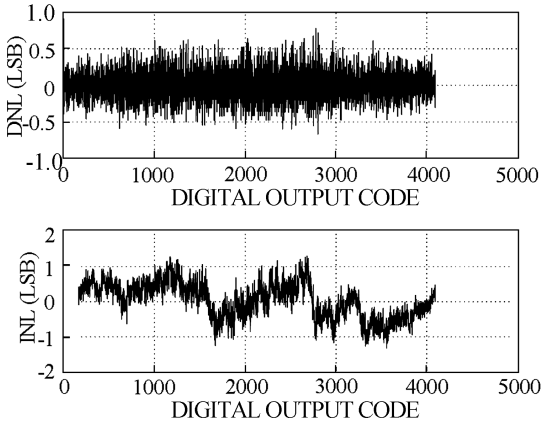

Fig. 9. Measured DNL and INL.

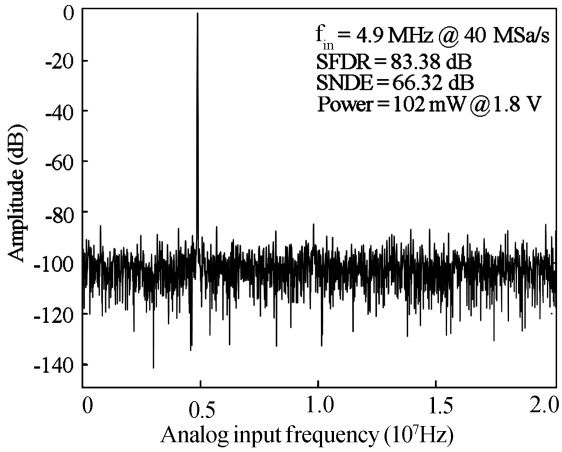

Fig. 10. Measured FFT spectrum.

Table 1. Summary of experimental results.

Parameter	Value
Resolution	12-bit
Conversion rate	40 MHz
Technology	0.18 μm CMOS with MIM capacitor
Supply voltage	1.8 V
Area (including PAD)	3.1×2.1 mm^2
Core circuit power	102 mW
DNL ($f_{in} = 4.9$ MHz)	-0.67 to $+0.78$ LSB
INL ($f_{in} = 4.9$ MHz)	-1.32 to $+1.3$ LSB
SFDR ($f_{in} = 4.9$ MHz)	83.38 dB
SNDR ($f_{in} = 4.9$ MHz)	66.32 dB

are placed in the blank areas and underneath the analog power lines and digital ground lines.

4. Measured results

The experimental printed circuit board (PCB) is show in Fig. 8. Figure 9 is the differential and integral nonlinearities (DNL and INL), which are measured with a 4.9 MHz full-scale sinusoidal wave input. As illustrated in Fig. 9, the DNL is within 0.78 LSB, and the INL is within 1.32 LSB at 40 MS/s. With a 4.9 MHz sinusoidal wave input, the output fast Fourier transform (FFT) spectrum is plotted in Fig. 10 at 1.8 V power supply and 40 MS/s. The measured signal-to-noise-and-

Table 2. Performance comparison with similar ADCs.

Reference	Bit	MS/s	Power (mW)	VDD (V)	DNL/INL	SFDR (dB)	SNDR (dB)	VIN (MHz)	Calibration	Technology	FOM* (pJ/step)
This work	12	40	102	1.8	0.78/1.32	83.38	66.32	4.9	N	0.18μm	1.5
Ref. [1]	13	16	78	1.3	0.5/2	62.5	59.2	8.75	N	0.25μm	6.5
Ref. [3]	14	30	350	3	0.5/1	84	64	1	Y	0.18μm	9
Ref. [12]	12	110	97	1.8	1.2/1.5	69.4	64.2	10	N	0.18μm	0.67
Ref. [13]	13	40	268	1.8	0.4/0.8	80	67	1	Y	0.18μm	3.6
Ref. [14]	12	75	273	3	0.64/0.95	75.8	65.6	1	Y	0.35μm	2.3

*FOM $= \frac{\text{Power}}{2^{\text{ENOB}} \times f_s}$.

distortion ratio (SNDR) is 66.32 dB, and the spurious free dynamic range (SFDR) is 83.38 dB. The ADC occupies a die area of 3.1 × 2.1 mm^2 and dissipates 102 mW at 40 MS/s.

The measured performances of the prototype ADC are summarized in Table 1. Table 2 compares this work with ADCs of similar performance recently reported in IEEE Journal of Solid-State Circuits (JSSC). The table reveals that the SFDR of this work is the best among the ADCs with 12-bit resolution and is very close to the value of the 14-bit resolution ADC in Ref. [3]. The FOM (figure of merit) of this work is only higher than that of Ref. [12]. However, Reference [12] may suffer from missing code, since the differential nonlinearity (DNL) of this ADC is larger than 1. Furthermore, the SFDR of Ref. [12] does not meet the requirements for modern communication applications[15]. So the tradeoffs between SFDR, SNDR and power are well balanced in our work, resulting in a high efficiency ADC.

5. Conclusion

This design proposes a 1.8 V 12-bit 40 MS/s calibration-free CMOS pipelined ADC, which can provide high dynamic performance with low power dissipation. A high SFDR is guaranteed by common-centroid symmetric capacitor techniques, deep N-well substrate isolation and careful layout design. Low power consumption is realized by using SHA-less architecture and by optimizing the sampling capacitance size and OTA bias current. The measurement results show 66.32 dB SNDR and 83.38 dB SFDR for 4.9 MHz input at 40 MSa/s. The prototype ADC presents a power consumption of 102 mW and occupies a total die area of 3.1 × 2.1 mm^2.

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