A low-jitter RF PLL frequency synthesizer with high-speed mixed-signal down-scaling circuits*

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Abstract: A low-jitter RF phase locked loop (PLL) frequency synthesizer with high-speed mixed-signal down-scaling circuits is proposed. Several techniques are proposed to reduce the design complexity and improve the performance of the mixed-signal down-scaling circuit in the PLL. An improved D-latch is proposed to increase the speed and the driving capability of the DMP in the down-scaling circuit. Through integrating the D-latch with 'OR' logic for dual-modulus operation, the delays associated with both the 'OR' and D-flip-flop (DFF) operations are reduced, and the complexity of the circuit is also decreased. The programmable frequency divider of the down-scaling circuit is realized in a new method based on deep submicron CMOS technology standard cells and a more accurate wire-load model. The charge pump in the PLL is also realized with a novel architecture to improve the current matching characteristic so as to reduce the jitter of the system. The proposed RF PLL frequency synthesizer is realized with a TSMC 0.18-μm CMOS process. The measured phase noise of the PLL frequency synthesizer output at 100 kHz offset from the center frequency is only –101.52 dBc/Hz. The circuit exhibits a low RMS jitter of 3.3 ps. The power consumption of the PLL frequency synthesizer is also as low as 36 mW at a 1.8 V power supply.

Key words: PLL; down-scaling circuits; prescalers; charge pump; jitter
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1. Introduction

The RF phase locked loop (PLL) frequency synthesizer is one of the most important parts of the DVB-T tuner, which is being widely researched due to the growing population of portable digital video broadcasting devices. As the RF PLL frequency synthesizer is also a mixed-signal system containing analogue and digital components, the design and realization of a low-jitter PLL-type frequency synthesizer is one of the challenging tasks of DVB-T tuner design[1], especially when it should be realized in deep submicron CMOS technology[2].

The down-scaling circuit is one of the most complicated components in the PLL frequency synthesizer. In order to realize the large division rate and frequency-hopping, the down-scaling circuit is always a programmable and mixed-signal component[3]. There are hundreds, even thousands of transistors in the down-scaling circuit of the RF PLL frequency synthesizer. Reducing the difficulty of designing the down-scaling circuit to improve the performance of the circuit is important in the realization of the PLL frequency synthesizer[4].

This paper presents the design of a low-jitter RF PLL frequency synthesizer with high-speed mixed-signal down-scaling circuits. At first, the structure of the PLL frequency synthesizer is introduced. Subsequently, the circuit techniques of high-speed mixed-signal down-scaling circuits such as an improved D-latch utilized in the DMP and a new method realizing the programmable frequency divider are discussed. Furthermore, the improved circuit topology making the current well matched for a charge pump in the proposed frequency synthesizer design is introduced. Then, the realization, and measurement of the RF PLL frequency synthesizer are discussed. Finally, some conclusions are presented.

2. PLL architecture

In the proposed DVB-T tuner, the filtered RF signal from the LNA (low noise amplifier) is at first mixed with the first local oscillator signal (LO1). Then, the signal is filtered by a poly-phase filter and mixed with the second local oscillator sig-

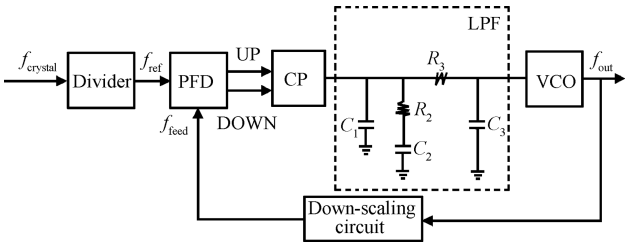

Fig. 1. Simplified architecture of the proposed PLL-type frequency synthesizer.

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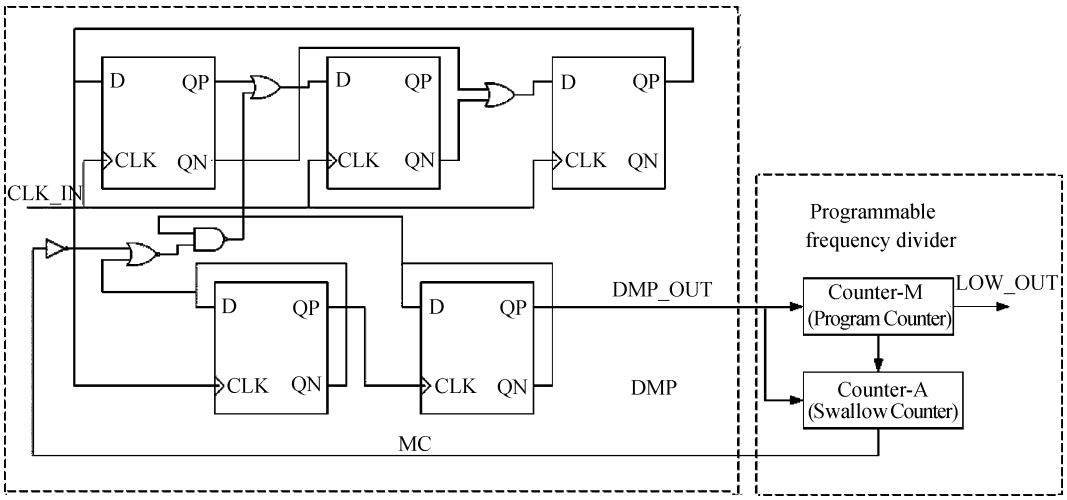

Fig. 2. Architecture of the down-scaling circuit.

nal (LO2). In the next step, the converted signal filtered by the other poly-phase filter is sent to a channel selecting filter to get the final signal needed by the system.

The PLL-type frequency synthesizer producing the second local oscillator signal (LO2) is proposed in this paper. As shown in Fig. 1, it is made up of a divider, a phase frequency detector (PFD), a charge pump (CP), a voltage-controlled oscillator (VCO), a down-scaling circuit, and a low pass filter (LPF) off the chip[5]. There is a divider with dividing-by-8 function to convert the signal of the off-chip crystal oscillator at a frequency of 16.38 MHz into the reference signal for the PFD. In order to reduce the chip area, the LPF of the frequency synthesizer is realized by off-chip components. An LO2 signal which covers the frequency band from 1170 to 1180 MHz is produced by the VCO and sent to the mixer. The output signal of the VCO is divided by the down-scaling circuit to obtain the feeding back signal of the loop for the PFD.

3. Key technology description

In the jitter of the RF PLL frequency synthesizer, the proportion of the jitter caused by the down-scaling circuit and the charge pump is sometimes even more than that caused by the VCO[6]. A high-speed mixed-signal down-scaling with high performance and a charge pump with current well-matched are proposed to reduce the jitter of the frequency synthesizer.

3.1. Down-scaling circuits

The block diagram of the down-scaling circuit in the proposed PLL-type frequency synthesizer is shown in Fig. 2. As shown in the figure, the down-scaling circuit consists of two parts: a DMP and a programmable frequency divider made up of a counter-M and a counter-A[7]. The values of A and M are initialized to counter-A and counter-M, and both counters begin to count up. The DMP divides the output by $P + 1$ until counter-A counts up to A. At this point it switches over and divides by P until counter-M counts up to M. Then, two counters are reset and DMP switches back to divide-by-$(P + 1)$ at the same time. The total division ratio of the down-scaling circuit N is equal to $PM + A$.

In the proposed frequency synthesizer, the lowest division ratio of the frequency synthesizer is 573 when $A = 13$ and $M = 35$, and the largest division ratio is 575 when $A = 15$ and $M = 35$. As shown in Fig. 2, the DMP is made up of a synchronous divided-by-4/5 circuit, two asynchronous divided-by-2 circuits made up of several master/slave D-flip-flops (DFFs), and some control logic gates. The signal MC is used to select the dual modulus division ratio. When the control signal MC is at logic high ($MC = 1$), the division ratio of the synchronous divided-by-4/5 circuit is equal to 5 and the total division ratio of the DMP is 17. Otherwise, the division ratio of the synchronous divided-by-4/5 is equal to 4, and the total division ratio of the DMP is equal to 16.

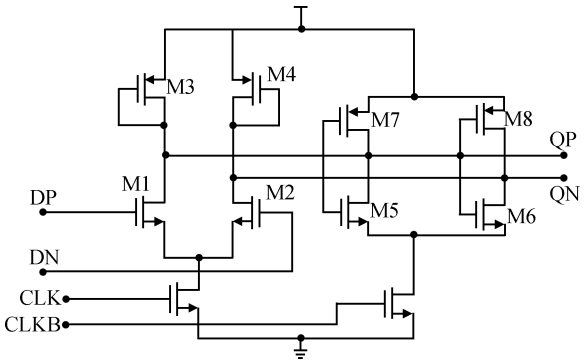

Fig. 3. Architecture of the improved D-latch.

3.1.1. DMP

The proposed DMP circuit is made up of some master/slave DFF and some control logic gates. The improved D-latch as shown in Fig. 3 is utilized to realize the master/slave DFFs in the DMP[8]. Compared with the conventional D-latch, the tail current resource is canceled. M1 and M2 form the input current switch pair. Complementary cross-coupled pairs M7 and M8 are used in the output part of the latch. The load of the output part is lightened, so the speed could be increased. M5 (M6) is used to turn off the discharge path when QP (QN) changes from logic 0 to logic 1. Although the output logic 1 decreases from VDD, and a static current path exists if the input data changes in the evaluation phase (CLK = logic '1'), the proper logic

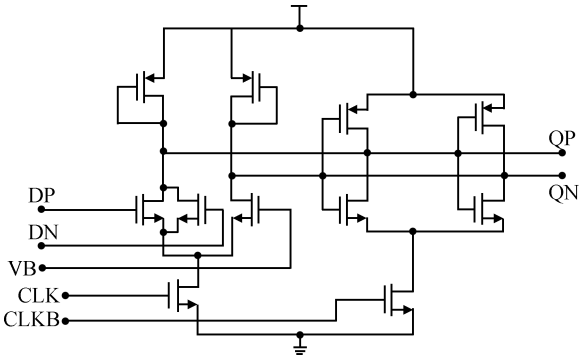

Fig. 4. Architecture of the improved D-latch integrated with 'OR' logic.

operation could be ensured by carefully selecting the sizes of the transistors. Moreover, in high-speed applications, due to the continuous switching at high frequencies, the dynamic power dissipation dominates and the added static power dissipation is not significant. So the improved high-speed DFF is favorable for RF applications and the output voltage can directly drive the following block without any post amplifier.

As shown in Fig. 2, the proposed DMP is made up of several source-coupled logic (SCL) DFFs and several 'OR' gates[9]. As an SCL DFF is made up of two latches with same structure, one works as the master-latch, the other one works as the slave-latch. Based on the D-latch shown in Fig. 3, the 'OR' gate is integrated with the master-latch of the DFF. The architecture of the latch integrated with 'OR' logic is shown in Fig. 4. It can be seen that DP and DN become two input ports of the 'OR' gate. VB is a reference bias voltage of 1 V. Through merging the 'OR' logic for dual-modulus operation into DFF, the delays associated with both the 'OR' and DFF operations are reduced, which increases the maximum operating frequency and decreases the complexity of the circuit.

3.1.2. Programmable frequency divider

The block diagram of the proposed programmable divider is shown in Fig. 2. It consists of two counters. One is the program counter, and the other is the swallow counter, where the program counter is modulus M while the swallow counter is modulus A ($M > A$). The control parameters M and A can be configured according to practical applications. Both of the counters count up until the values are equal to M and A separately. A period of LOW_OUT is completed when the program counter counts up to M. At the same time, the counters of the programmable frequency divider are cleared when the program counter counts up to M[10]. The most important output of the programmable frequency divider is MC, which is used to control the proposed DMP divided-by-16/17. If MC is high, the DMP is divided-by-17; otherwise, it is divided-by-16. The total division ratio N of the down-scaling circuit in the DVB-T receiver can be realized based on the following formula: $N = A \times 17 + (M - A) \times 16 = M \times 16 + A$.

The proposed programmable frequency divider is designed in a new method based on Artisan's 0.18-μm CMOS standard cell library. Unlike the full custom design, the standard cell based design mainly depends on EDA tools and the standard cell library[11].

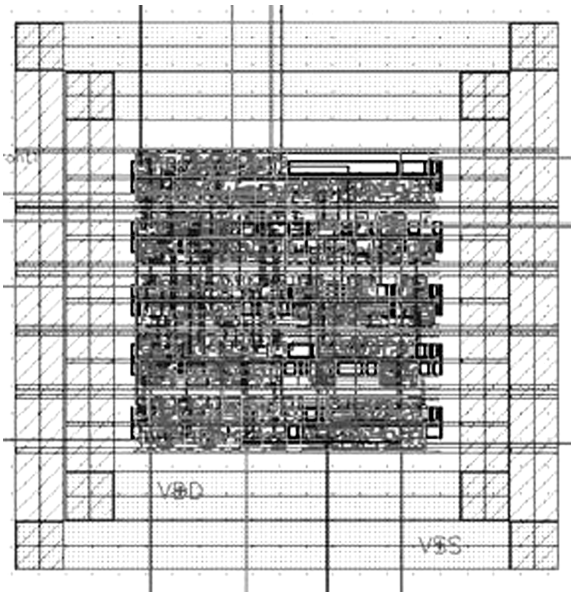

Fig. 5. Layout of the programmable frequency divider.

In the first step, the function is realized in Verilog-HDL. Then a synthesis tool of a design compiler is used to synthesize the design in the first step. In submicron technology, especially in deep submicron CMOS technology, the more accurate the wire-load model is, the more optimal the design is. In most cases, the default wire-load models provided by synthesis tools are linear with respect to the fan-outs of the circuit, in which the path delay, wire-load and wire length have linear relationships with the fan-outs of the circuits. That is to say, the default relationships between the path delay, wire-load and wire length with the fan-outs are linear. However, that is not practical. So it is necessary to generate a more accurate wire-load model to improve the synthesis results for a specific design. In order to create a custom wire-load model before detailed synthesis, initial synthesis and initial placement and route are added to this step when compared with the traditional design flow. The "initial" means that there is no need to pay much attention to timing because initial synthesis and initial placement and route are just for creating a practical wire-load model. After finishing initial placement and route, RC parameters and wire-load delay are obtained and then back-annotated to synthesis tools to generate the final custom wire-load models. In the obtained custom wire-load models, wire-length, and so on do not vary linearly with the fan-outs. Compared with the default linear wire-load models, the custom wire-load models are more accurate and practical.

The next steps are placement and route, which are back-end designs and can be completed in Apollo, Synopsys' VLSI implementation program. The last step of the design flow is the verification. In this step, the layout information is imported from Apollo into Cadence Virtuoso, and some processes such as design rule check (DRC) and layout versus schematic (LVS) can be done to verify the correction of the design. It was finally realized in a 0.18 μm mixed-signal CMOS process. The final layout of the programmable frequency divider is shown in Fig. 5.

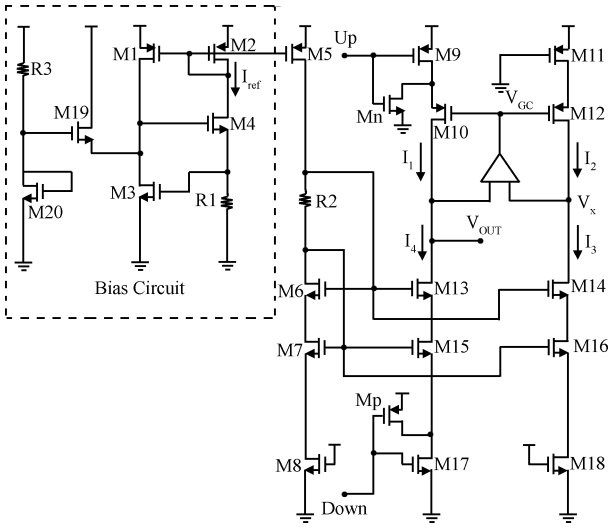

Fig. 6. Architecture of the charge pump.

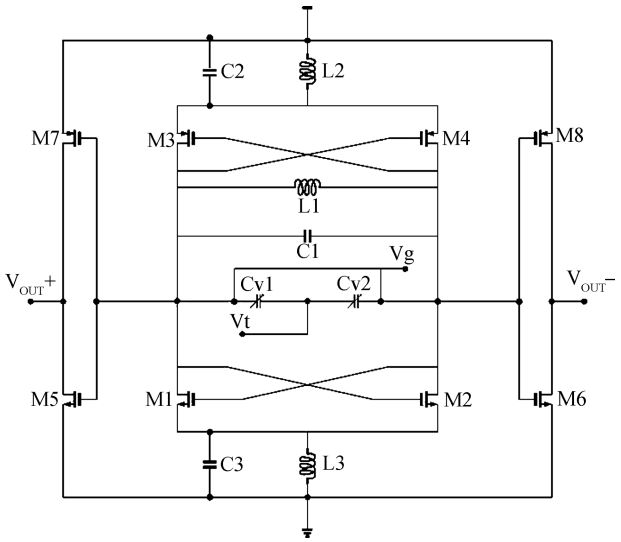

Fig. 7. Schematic diagram of the VCO.

3.2. Charge pump

The current mismatch of the charge pump in the PLLs generates a phase offset which increases the jitters of the PLL output signals. Also, the phase offset reduces the locking range of the PLL. Conventional CMOS charge pump circuits have some current mismatch due to the difference between the drain–source voltage of the PMOS and NMOS transistors. The current mismatch of the charge pump in the PLLs generates a phase offset which increases spurs in the PLL output signals. Also, the phase offset reduces the locking range in the wide range PLL with a dual loop scheme frequency locking loop and phase locking loop, especially[12]. Therefore, a new charge pump with better current matching characteristics is proposed. Its schematic is shown in Fig. 6.

As shown in Fig. 6, transistors M17 and M9 are used as switches. Mp and Mn are connected to them respectively to reduce power/ground bounce due to the on/off action of the switches[13]. By using an error amplifier, the voltage $V_{\rm X}$ at the reference node of the current mirror (M11, M12, M14, M16, M18) follows the voltage $V_{\rm OUT}$ at the output node of the charge pump (M9, M10, M13, M15, M17). As a result, voltage $V_{\rm X}$ is equal to the voltage $V_{\rm OUT}$ as long as the amplifier maintains a high enough gain. For M9 = M11, M10 = M12, M6 = M13 = M14, M7 = M15 = M16, M8 = M17 = M18, there is $I_1 = I_2 = I_3$ if the DOWN and the UP signal are high, and there is $I_3 = I_2 = I_4$ if the DOWN and the UP signal are low. So $I_1 = I_4$ is maintained well. In order to increase the pull-in range of the current matching, a self-biasing cascade current mirror, which is made up of R2, M6, M7, M13, M15, M9 and M17, is included in the charge pump to reduce the charge sharing. The bias circuit of the charge pump is shown in Fig. 6. The output current of the proposed bias circuit is $I = V_{\rm th}/R_1 + 1/R_{12}k + (2R_1kV_{\rm th} + 1)^{1/2}/R_1^2k$, where $k = \mu_{\rm n}c_{\rm OX}$. So the output current of the bias circuit is independent of the power supply. Because M10, M12 and the error amplifier form a closed loop, the parameters of the transistors in the loop are well calculated to ensure the stability of the loop. With all the techniques above, the current matching characteristics are much improved.

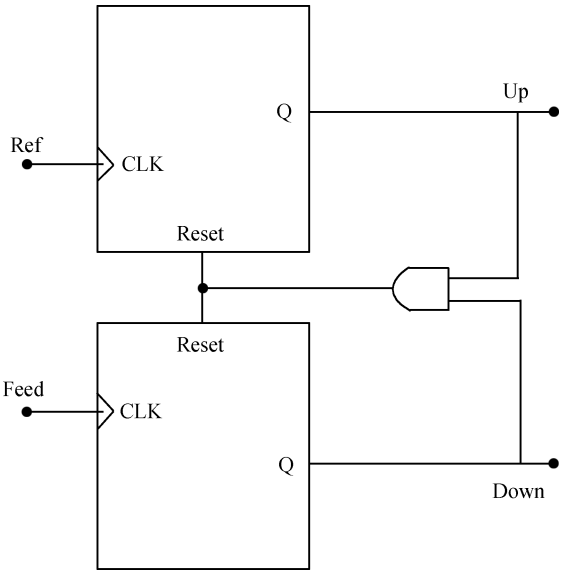

Fig. 8. Block diagram of the PFD.

4. Other building blocks

The schematic of the VCO in the PLL is shown in Fig. 7. In the PLL, only this circuit was realized in a 0.18-μm RF CMOS process and the other components were realized in a 0.18-μm mixed-signal CMOS process. The oscillator core includes both PMOS and NMOS cross-coupled amplifiers. The advantage of the topology is current reuse, which means the same current can provide more negative resistance. The offset voltage $V_{\rm g}$ is set to 0.8 V. The output buffers are realized with invertors. Two resonant circuits, with resonant frequency of $2\omega_0$, consist of L_2, C_2 and L_3, C_3. They can depress the deterioration of the quality factor of the tank circuit, which is caused by the cross-coupled amplifiers. This is called the noise filtering technique[14].

A block diagram of the PFD and the charge pump is shown in Fig. 8. The tri-state PFD was made up of two resettable DFF and an 'and' gate[15]. The DFF was realized with the true sin-

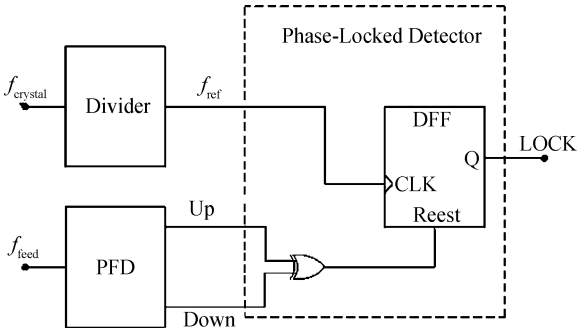

Fig. 9. Block diagram of the phase-locked detector.

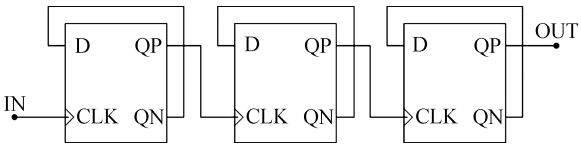

Fig. 10. Block diagram of the frequency divider.

gle phase clock (TSPC) structure. To eliminate dead-zone, a delay element was added to the reset path. The proposed PFD has the advantages of a pre-charged PFD. It has lower power consumption and a higher precision than the latch-based PFD because the dynamic logic circuit has lower propagation delay and better matching. The phase noise contribution of the PFD can be relieved.

A diagram of the phase-locked detector is shown in Fig. 9. When PLL is locked, up and down pulses are narrower than the delay time value. The phase-locked detector circuit detects these narrow pulses and counts for some update (reference) periods, and then produces a high voltage signal.

In the proposed PLL, the output signal of the crystal oscillator should be divided by 8 to get the reference signal for the PFD. The diagram of the frequency divider is shown in Fig. 10. It is realized with three TSPC DFFs.

5. System design strategy

A mixed MATLAB and C-language platform is utilized in the behavior simulation of the PLL frequency synthesizer. In order to approximate the dynamic behavior model of the PLL frequency synthesizers, a dynamic behavior model based on the bilinear z-transform is programmed in the C-language to realize the fast behavior simulation of the PLL frequency synthesizer[16]. The results of the behavior simulation program are executed with MATLAB. This combination results in a high degree of versatility in a simulation environment. Compared with a conventional simulation method, it has higher efficiency and definition.

The 3-order loop filter is somewhat more complicated. The impedance of the loop filter is given by

$$Z_{\rm lpf3}(s) = (1+s\tau_2)\{s[s^2C_1\tau_2\tau_3 + s(C_1\tau_2 + C_1\tau_3 + C_3\tau_2 + C_2\tau_3) + C_1 + C_2 + C_3]\}^{-1}, \quad (1)$$

where $\tau_2 = R_2C_2$, $\tau_3 = R_3C_3$. The frequency dominant function can be transferred into the time dominant function of

Table 1. Summary of the loop parameters.

Parameter	Value	Parameter	Value
Reference clock	2.0475 MHz	C_1	1.5 nF
Loop bandwidth	13 kHz	C_2	11.1 nF
Phase margin	45°	C_3	20 pF
$I_{\rm CP}$	0.5 mA	R_2	1.6 kΩ
$K_{\rm VCO}$	51 MHz/V	R_3	4.5 kΩ

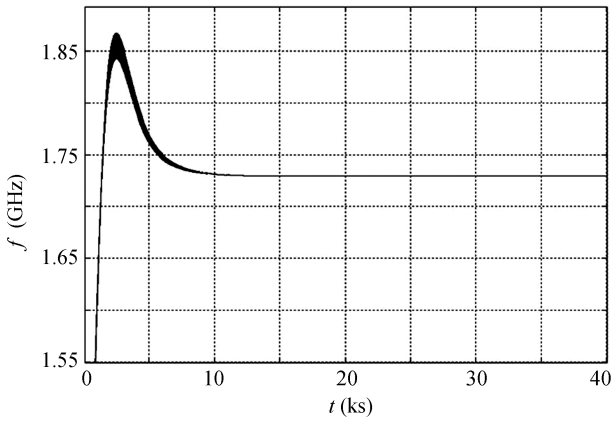

Fig. 11. Simulation of the PLL frequency synthesizer.

the sampling time $T_{\rm step}$ by replacing each occurrence of s by $2(1-z^{-1})/T_{\rm step}(1+z^{-1})$ as follows:

$$f(z) = \frac{2}{T_{\rm step}}\frac{1}{1-z^{-1}}F\left(\frac{2(1-z^{-1})}{T_{\rm step}(1+z^{-1})}\right). \quad (2)$$

Equation (1) can be rearranged as

$$Z_{\rm lpf3}(z) = \frac{a_3z^{-3}+a_2z^{-2}+a_1z^{-1}+a_0}{b_4z^{-4}+b_3z^{-3}+b_2z^{-2}+b_1z^{-1}+b_0}, \quad (3)$$

where

$$\begin{aligned}
b_4 &= 8C_1R_2C_2R_3C_3 - 4(C_1R_2C_2 + C_1R_3C_3 + C_3R_2C_2 \\
&\quad + C_2R_3C_3)T_{\rm step} - (-2C_3 - 2C_1 - 2C_2)T_{\rm step}^2, \\
b_3 &= -32C_1R_2C_2R_3C_3 + 8(C_1R_2C_2 + C_1R_3C_3 \\
&\quad + C_3R_2C_2 + C_2R_3C_3)T_{\rm step}, \\
b_2 &= 48C_1R_2C_2R_3C_3 - (4C_3 + 4C_1 + 4C_2)T_{\rm step}^2, \\
b_1 &= -32C_1R_2C_2R_3C_3 - 8(C_1R_2C_2 + C_1R_3C_3 \\
&\quad + C_3R_2C_2 + C_2R_3C_3)T_{\rm step}, \\
b_0 &= 8C_1R_2C_2R_3C_3 + 4(C_1R_2C_2 + C_1R_3C_3 + C_3R_2C_2 \\
&\quad + C_2R_3C_3)T_{\rm step} + (2C_3 + 2C_1 + 2C_2)T_{\rm step}^2, \\
a_3 &= T_{\rm step}^3 - 2R_2C_2T_{\rm step}^2, \\
a_2 &= 3T_{\rm step}^3 - 2R_2C_2T_{\rm step}^2, \\
a_1 &= 3T_{\rm step}^3 + 2R_2C_2T_{\rm step}^2, \\
a_0 &= T_{\rm step}^3 + 2R_2C_2T_{\rm step}^2.
\end{aligned}$$

In order to keep the stability of the loop, the phase margin of the proposed PLL is set to 45°. The loop bandwidth of the

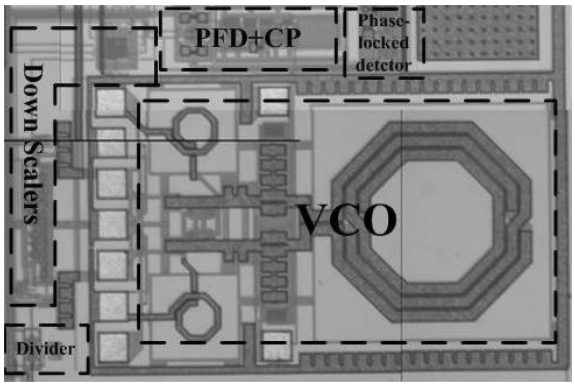

Fig. 12. Chip microphotograph of the PLL frequency synthesizer.

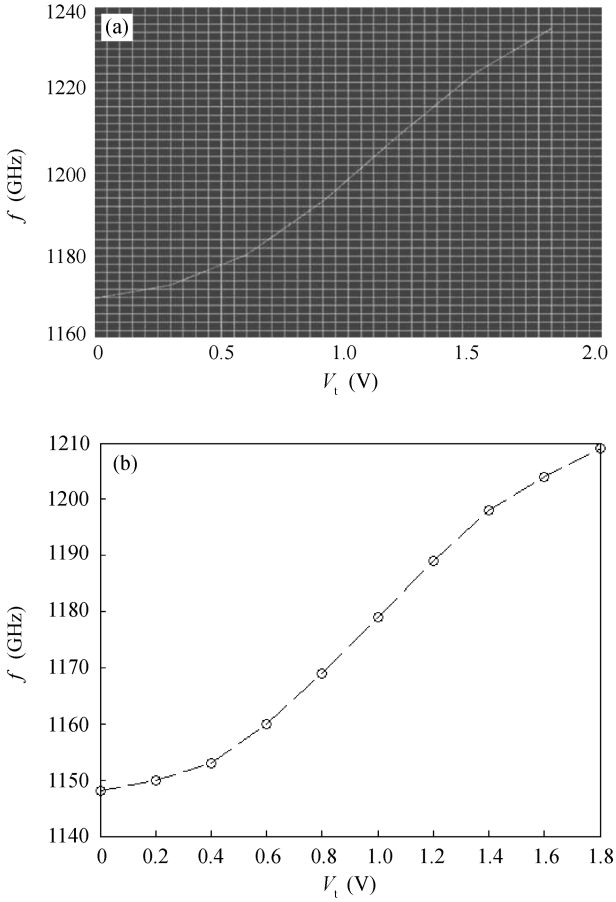

Fig. 13. (a) Post simulation results of the VCO's tuning characteristic. (b) Measured tuning characteristic of the VCO.

PLL can be increased to constrain the phase noise. However, the stability of the loop will decrease if the bandwidth is too large. A compromise should be made when the parameters of the components in the LPF and the other important parameters in the loop are considered. Some important loop parameters of the proposed PLL are listed in Table 1.

Figure 11 shows the transient response of the VCO output frequency in the closed loop state. It can be seen that the stability time of the PLL is about 27.3 μs. This result approaches the simulation result of the transistor-level simulation.

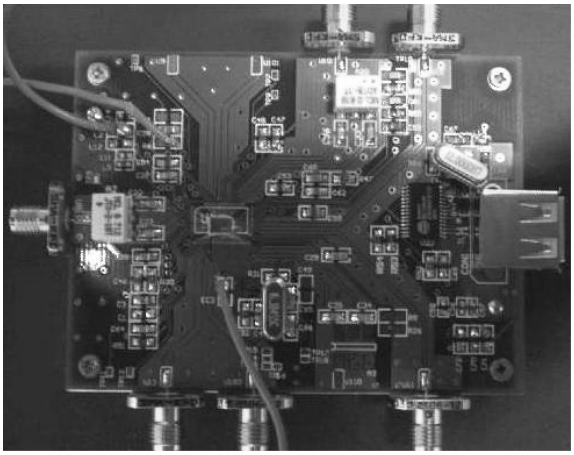

Fig. 14. Photograph of the test PCB.

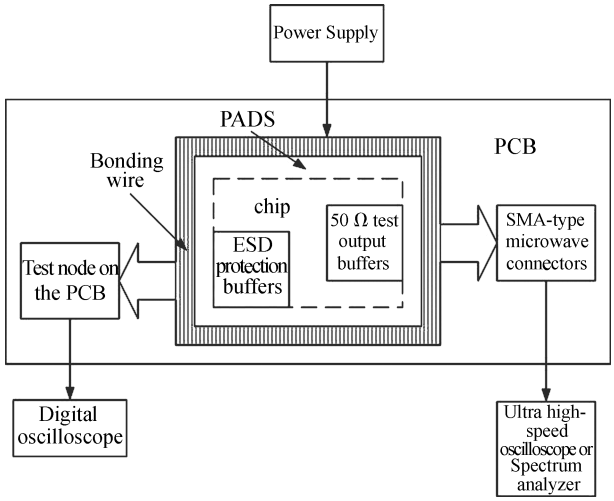

Fig. 15. Measurement system architecture.

6. Experimental results

The proposed frequency synthesizer was implemented in TSMC's 0.18-μm CMOS process with 1.8 V power supply and was integrated into the DVB-T tuner chip. The total area of the tuner chip is about 2.0 $\times$ 2.0 mm^2, including the area of the proposed frequency synthesizer, about 140 $\times$ 110 μm^2. Figure 12 shows a microphotograph of the frequency synthesizer.

The measurement of the chip includes two parts. In the first part, the VCO part was tested alone on-wafer. The post simulation result of the VCO tuning characteristic is shown in Fig. 13(a). The experimental result of the VCO tuning characteristic is obtained through on-wafer measurement as shown in Fig. 13(b). Notice that frequency band 1.17–1.18 GHz is in the linear region of the curve and the slope of the linear region is not too large, which shows that the output frequency band of VCO includes the second local oscillator signal of the DVB-T tuner.

In the second part of the measurement, the proposed frequency synthesizer is tested as a part of the tuner chip. The test PCB bonded with the DVB-T tuner chip is shown in Fig. 14. The off-chip components such as the crystal oscillators, LPF, balun and so on are welded onto the PCB. The architecture of

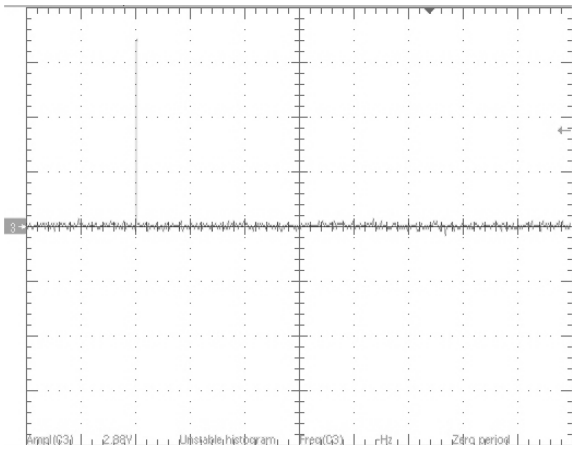

Fig. 16. Measured output signal of the phase-locked detector.

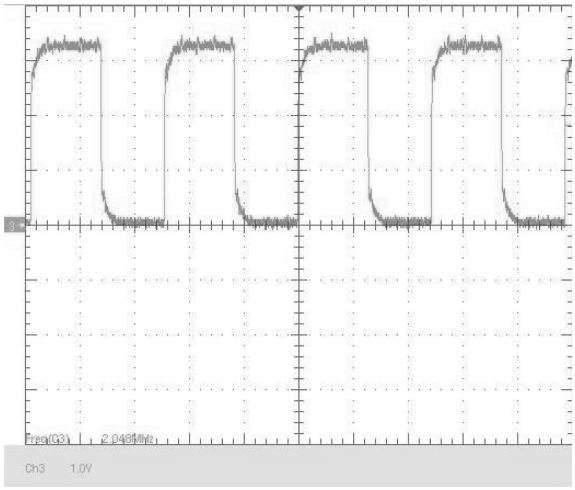

Fig. 17. Measured output signal of the down-scaling circuit (y axis, 1 V/div).

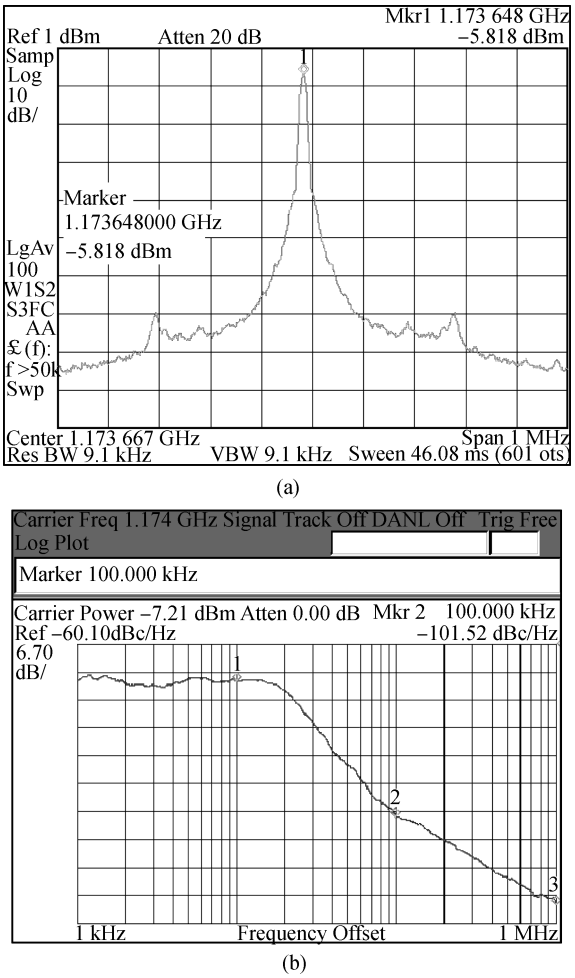

Fig. 18. (a) Measured spectrum of the frequency synthesizer's output signal. (b) Measured phase noise of the frequency synthesizer's output signal.

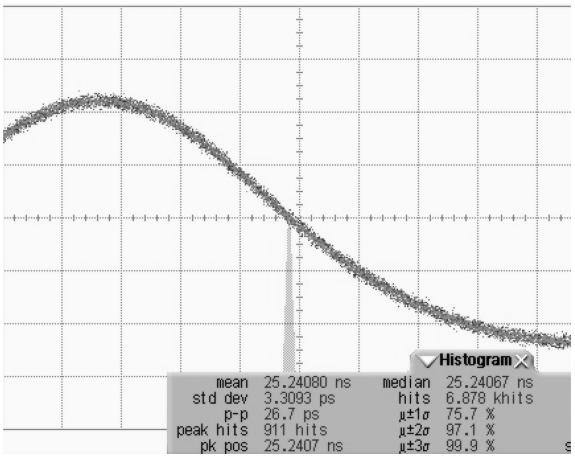

Fig. 19. Measured jitter of the output signal.

the measurement is shown in Fig. 15.

Some signals at high frequency which need to be tested are connected to SMA-type microwave connectors at the edge of the PCB. These signals are sent to the ultra high-speed oscilloscope or spectrum analyzer. The input resistance of the measurement instruments above is 50 Ω. Some 50 Ω test output buffers are designed at the output nodes before they are connected to the pads in the chip. On the other hand, some test nodes for signals at low frequency which need to be tested are designed on the PCB. In order to prevent electronic discharge (ESD), ESD protection buffers are added between the output nodes of these low frequency signals with the pads in the chip. These ESD protection buffers have an independent power supply. The testing detectors connected to the measurement instruments such as the digital oscilloscope are touched on these nodes to get the desired signals.

The measurement results show that the proposed PLL frequency synthesizer can work well with the other parts of the tuner. The PLL frequency synthesizer only consumes 30 mW from 1.8 V power supply.

The measured output signal of the phase-locked detector is shown in Fig. 16. The measured output voltage is kept at a high value of 2.9 V, as the power supply voltage of the ESD protection buffers is 3.3 V. The output signal of the down-scaling circuit is shown in Fig. 17. The measured output frequency is 2.048 MHz, which keeps the reference signal of the PFD the same. It can be seen from all the above that the PLL is well locked. All these measurement results show that the proposed

circuit is a good choice for integrating into the DVB-T tuner.

Figure 18(a) shows the measured spectrum of the proposed frequency synthesizer's output signal in a locked state at 1.173 GHz with a reference signal of 2.048 MHz. From the figure it can be seen that the center frequency is 1.173 GHz and the output power is −5.8 dBm. It can be seen from Fig. 18(b) that the phase noise is only −101.52 dBc/Hz at 100 kHz off the center frequency.

The measured jitter of the output signal is shown in Fig. 19 at a frequency of 1.173 GHz in the PLL frequency synthesizer when the loop is locked. It can be seen in the figure that RMS jitter is only 3.3 ps.

All these measurement results show that the proposed circuit is a good choice for integrating into the DVB-T tuner.

7. Conclusions

A low-jitter RF PLL frequency synthesizer with high-speed mixed-signal down-scaling circuits is proposed in this work. Some new circuit techniques are adopted to improve the performance of the proposed PLL frequency synthesizer. The DMP is realized with improved D-latch architecture and the novel D-latch architecture is integrated with 'OR' logic. The programmable frequency divider designed with the new method is based on standard cells and a more accurate wire-load model. It can be seen that the complexity of the down-scaling circuit is reduced and the performance of the circuit is improved with the circuit techniques above. Furthermore, the charge pump is realized with a novel architecture to realize a perfect current matching characteristic in order to reduce the jitter of the system. The proposed frequency synthesizer was implemented in TSMC's 0.18-μm CMOS process with 1.8 V power supply and was integrated into the DVB-T tuner chip. The measurement results show that the proposed PLL frequency synthesizer has a low jitter of only 3.3 ps when it is locked. Its consumption is as low as 36 mW.

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