Numerical study of the sub-threshold slope in T-CNFETs*

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Abstract: The most attractive merit of tunneling carbon nanotube field effect transistors (T-CNFETs) is the ultra-small inverse sub-threshold slope. In order to obtain as small an average sub-threshold slope as possible, several effective approaches have been proposed based on a numerical insight into the working mechanism of T-CNFETs: tuning the doping level of source/drain leads, minimizing the quantum capacitance value via tuning the bias condition or increasing the insulator capacitance, and adopting a staircase doping strategy in the drain lead. Non-equilibrium Green's function based simulation results show that all these approaches can contribute to a smaller average inverse sub-threshold slope, which is quite desirable in high-frequency or low-power applications.

Key words: sub-threshold slope; T-CNFETs; quantum capacitance; BTBT; NEGF
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1. Introduction

Due to the thermally broadened Fermi distribution of carriers, the minimal inverse sub-threshold slope of conventional FETs is limited to 60 mV/dec at room temperature, which is a major obstacle to further reducing the supply voltage and switching delay. Recently, band-to-band tunneling (BTBT) has been proposed as an effective means to obtain sub-threshold slope (SS) below this limitation. For T-CNFETs[1], due to the superior gate control and the one-dimensional current transport in CNFETs, the BTBT barrier is transparent enough to be easily tunneled through. SS much smaller than 60 mV/dec can be obtained[1, 2].

On one hand, unfortunately, the quantum capacitance (QC), which is unlikely to be neglected in scaled CNFETs[2, 3], has a negative impact on the device performance. For example, the impact of QC on saturation source-drain current $I_{\rm d}$ in CNFETs was observed in Ref. [4] using both density functional theory and NEGF formalism. Due to the substantial impacts of QC in the device design, much research work has been done on both theoretical simulation[3, 5] and experimental measurement[6−8] of the QC value.

On the other hand, T-CNFETs suffer from an ambipolar transport characteristic owing to the fact that either electrons or holes can BTBT through CNT-source/drain contacts[9]. Such ambipolar conductance would impact the sub-threshold performance in application.

In this paper, based on an insight into the analysis expression of inverse sub-threshold slope in T-CNFETs, causes that result in the increase of SS have been studied and some corresponding measures are presented to decrease SS as soon as possible.

2. Modeling

Due to wave-particle dualism, charges in CNFETs are governed by both the Schrödinger and Poisson equations. In the nano region in particular, quantum phenomena play an important role in device performance and can no longer be ignored. In this paper the NEGF method is used to develop the CNFET model in order to take quantum phenomena such as electron tunneling and quantum capacitance into account. The NEGF formalism, which solves the Schrödinger equation and Poisson equation iteratively, describe the carrier transport in CNFETs exactly[10−11] and provides a sound basis for quantum device simulation. In this approach, the device is described by a Hamiltonian $H_{\rm C}$ using a simple π-orbital nearest neighbor tight-binding model without consideration of the exchange-correlation effect. For the convenience of calculation, self-energy matrices $\sum_{\rm S}$ and $\sum_{\rm D}$, which provide the appropriate quantum boundary conditions, are introduced to describe the effect of source/drain leads.

In order to relieve the computational burden, mode space is doped in this paper and it is valid when the potential variation around the tube is much smaller than the spacing between the sub-bands. Due to quantum confinement along the tube circumference, the wave functions of carriers are bound around the CNT and can only propagate along the tube axis. Therefore the potential profile does not vary around the circumference of the CNT and sub-bands can be decoupled[12]. According to both theoretical analysis and experimental results, it is valid for mode space to consider the lowest two sub-bands as for CNFETs with a $(13, 0)$ carbon nanotube channel[9, 13−14] under the assumed bias condition in this paper.

It should be pointed out that the flat band voltage is assumed to be 0 V and carbon nanotube chirality is $(13, 0)$ unless stated otherwise. A detailed description on the modeling of CNFETs based on the NEGF method can be found in Ref. [12, 15].

3. Impacts of source/drain doping level

According to Ref. [6], the inverse sub-threshold slope in T-CNFETs can be expressed as

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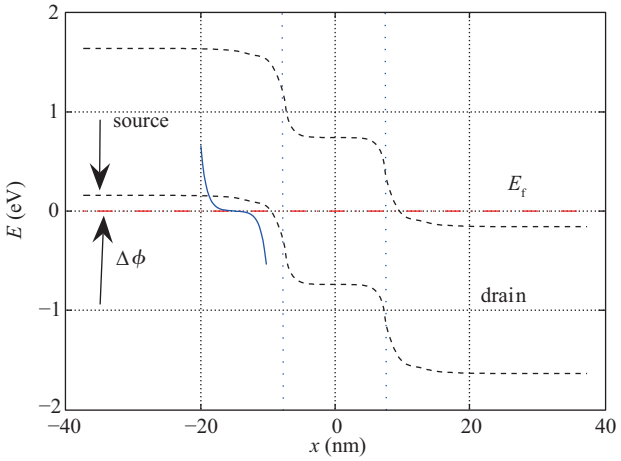

Fig. 1. T-CNFET band diagram, where gate voltage $V_g = 0$ V, drain-source bias voltage $V_{DS} = 0$ V, source/drain doping level $\rho = 8\times10^8$ cm^{-1}, tight-binding parameter $\phi_{pp} = -3$ eV, insulator thickness t = 2 nm, insulator dielectric constant $\varepsilon = 16$.

$$S = \ln(10) I_d \left\{ \frac{2q^2}{h} \left[\frac{\partial T}{\partial E_C^{ch}} F(E) + T \frac{\partial F(E)}{\partial E_C^{ch}} \right] \right\}^{-1}, \quad (1)$$

where T denotes the band-to-band transmission probability and $F(E) = \int_{E_V^S}^{E_C^{ch}} (f_s(E) - f_d(E))\,dE$ denotes the electron distribution functions, where E_C^{ch} represents the conductance top in the channel and E_V^S the valence bottom in the source lead.

The right side of Eq. (1) is composed of two parts, representing two different mechanisms for realizing a steep SS respectively. The former part dominates when T is small and increases rapidly with variation of V_g, while the latter part becomes dominant if T is close to unity and changes only slightly with the variation of V_g. However, it is important to note that a small SS with a certain gate voltage is not sufficient: an average small S_{ave} over a much larger gate voltage range is more desirable. Therefore, it is desirable to make $T(E)$ as close to unity as possible since this allows for higher switching speed in practice.

As shown in Fig. 1, the electron distribution in CNFETs is governed by the Fermi–Dirac function. In order to achieve a minimal S_{ave}, the source/drain doping level, denoted by ρ, and the CNT diameter d must satisfy

$$f(\rho) = E_g/2 + \Delta\phi \approx 0.4/d + \Delta\phi, \quad (2)$$

where $f(\rho)$ denotes the band variance due to acceptor / dispenser iron doping in source/drain leads. The corresponding energy band is shown in Fig. 1. A gap of $\Delta\phi$ exists between the valence (conductance) band in the source (drain) lead and the conductance (valence) band in the channel.

The $\Delta\phi$ value cannot be too large in order to achieve an ideal S_{ave}. Figure 2 shows transfer characteristics of T-CNFETs with three different source/drain doping levels. When different source/drain doping levels are doped, the source Fermi energies vary from 0.11 eV to 0.54 eV as Fig. 2(a) shows, and the corresponding S_{ave} increases from 23.6 up to 48.3 mV/dec.

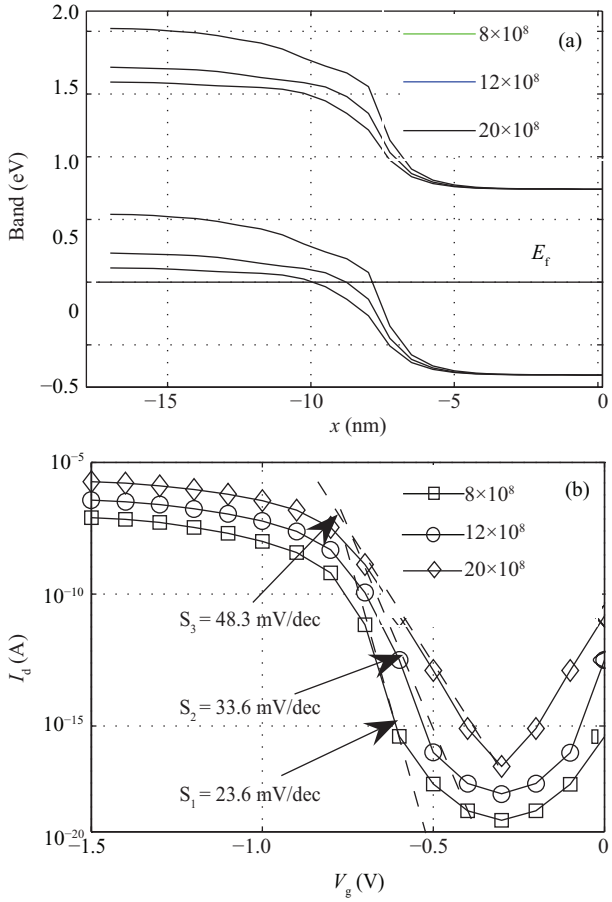

Fig. 2. (a) Impact of doping level on band structure in T-CNFETs, and (b) the corresponding transfer characteristics with $V_{DS} = -0.6$ V.

Note that what Fig. 1 models is the PIN structure. The NIP structure can of course also be used to get T-CNFETs.

4. Impacts of quantum capacitance

In low-dimension systems, the available electron states are numbered. The electric charges are regulated by the limited density of states (DOS) as well as the electrostatic force. Therefore, the QC arising from a finite DOS is unlikely to be neglected in the quantum regime. The QC effect contributes to the total capacitance by adding an additional quantum capacitance C_q to the insulator capacitance C_{ox} in series $C_{tot} = (\frac{1}{C_q} + \frac{1}{C_{in}})^{-1}$. Due to the series connection of C_q to C_{ox}, the control ability of gate voltage on channel conductance is negatively impacted. For example, the dependence of ΔE_C on V_g is modeled as shown in Fig. 3, where ΔE_C denotes the surface potential variation with V_g increasing by 1 V. The circle-marked line represents the situation with $V_{DS} = -0.3$ V, while the diamond-marked line represents that with -0.6 V. It is obvious that ΔE_C is always smaller than the varying step of V_g, which would have a negative effect on the sub-threshold performance just as Fig. 4 shows, where the average sub-threshold slope over the whole sub-threshold region is increased from 52.8 mV/dec to 65.3 mV/dec.

In order to improve the sub-threshold performance of T-CNFETs, much effort should be made to decrease the value of QC in the device design.

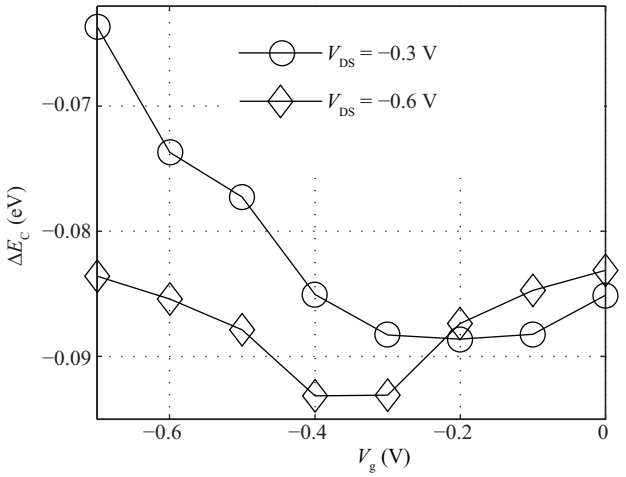

Fig. 3. Impact of quantum capacitance on the CNT surface potential in T-CNFETs with V_{DS} of −0.3 V (circle-marked line) and −0.6 V (diamond-marked line).

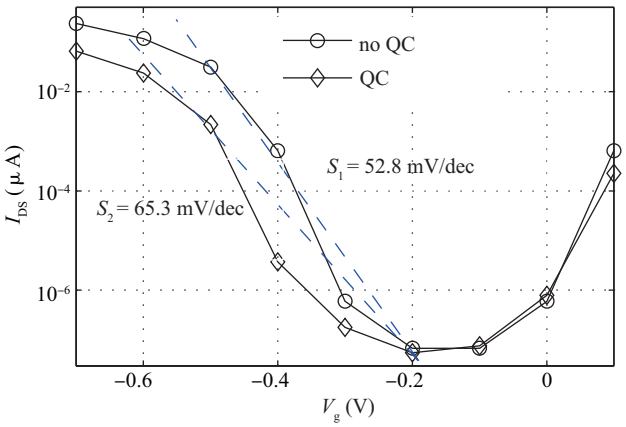

Fig. 4. Impact of quantum capacitance on the transfer characteristic of T-CNFETs with $V_{DS} = -0.6$ V.

As Ref. [14] introduced, the value of QC can be expressed as:

$$C_Q = \frac{q^2}{4k_B T_K h}\sqrt{\frac{m_{eff}}{2}}\int_0^\infty \frac{M(E)}{\sqrt{E}}T^* \times\left[\sec h^2\left(\frac{E+E_g/2-qV_{CS}}{2k_B T_K}\right)\left(\frac{2}{T_D}-1\right) + \sec h^2\left(\frac{E+E_g/2+q(V_{DS}-V_{CS})}{2k_B T_K}\right) \times\left(\frac{2}{T_S}-1\right)\right]dE, \quad (3)$$

where m_{eff} denotes the electron effective mass in CNT and is set to $0.06m_0$ in this paper, T_S, T_D are the transmission probabilities over source-channel and channel-drain contacts respectively, $T^* = T_S T_D/(T_S + T_D - T_S T_D)$ is the composite transmission probability for the entire system, k_B is Planck's constant, T_K is the lattice temperature and V_{CS} denotes the surface potential of the channel.

The right side of Eq.(3) consists of two parts. The former

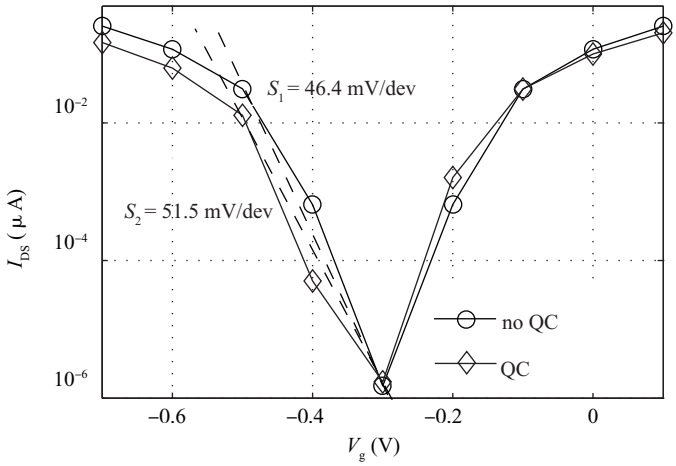

Fig. 5. Impact of quantum capacitance on the transfer characteristic of T-CNFETs with $V_{DS} = -0.3$ V.

reaches the minimum when $V_{CS} = 0$ V and increases quasi-quantitively with the increase or decrease of V_g. The latter part resembles the former with the exception that V_{CS} is replaced with $V_{CS} - V_{DS}$, such that its dependence on E is shifted by a value of V_{DS}.

When a symmetrical doping strategy is adopted, Equation (3) gives:

$$V_g^{min} = F^{-1}(V_{DS}/2), \quad (4)$$

where V_g^{min} denotes the gate voltage that corresponds to the minimal QC value, while F is the function between V_{CS} and V_g.

As Eq. (4) shows, V_g^{min} depends strongly on the drain-source bias voltage V_{DS}, which is consistent with the simulation result as Fig. 3 shows, where the absolute value of ΔE_C corresponding to $V_{DS} = 0.6$ is basically smaller than that corresponding to $V_{DS} = 0.3$. The transfer characteristics of T-CNFETs with $V_{DS} = 0.3$ are modeled in Fig. 5, where the S_{ave} over the whole sub-threshold region increases from 46.4 up to 51.5 mV/dev due to the QC effect. It is obvious, by comparing Fig. 5 to Fig. 3, that the impact of QC on SS is decreased from 23.4% down to 10.9% with V_{DS} changing from −0.6 V to −0.3 V. So, the first possible measure is to tune the bias condition of the device. But much attention should be paid to the choice of the bias condition in the device design owing to the fact that many other figures of merit, the ON–OFF current ratio for instance, depend strongly on the supply voltage value.

Another obvious measure is to increase the insulator capacitance by decreasing the insulator thickness or increasing the insulator dielectric constant. For example, a slight increase in the absolute value of ΔE_C is obtained when the insulator thickness is decreased from 6 nm to 3 nm, just as Figure 6 shows. This would contribute to a better sub-threshold performance as noted above.

5. Staircase doping strategy

The most attractive advantage of T-CNFETs is its super-high switching speed. However, due to the fact that either holes

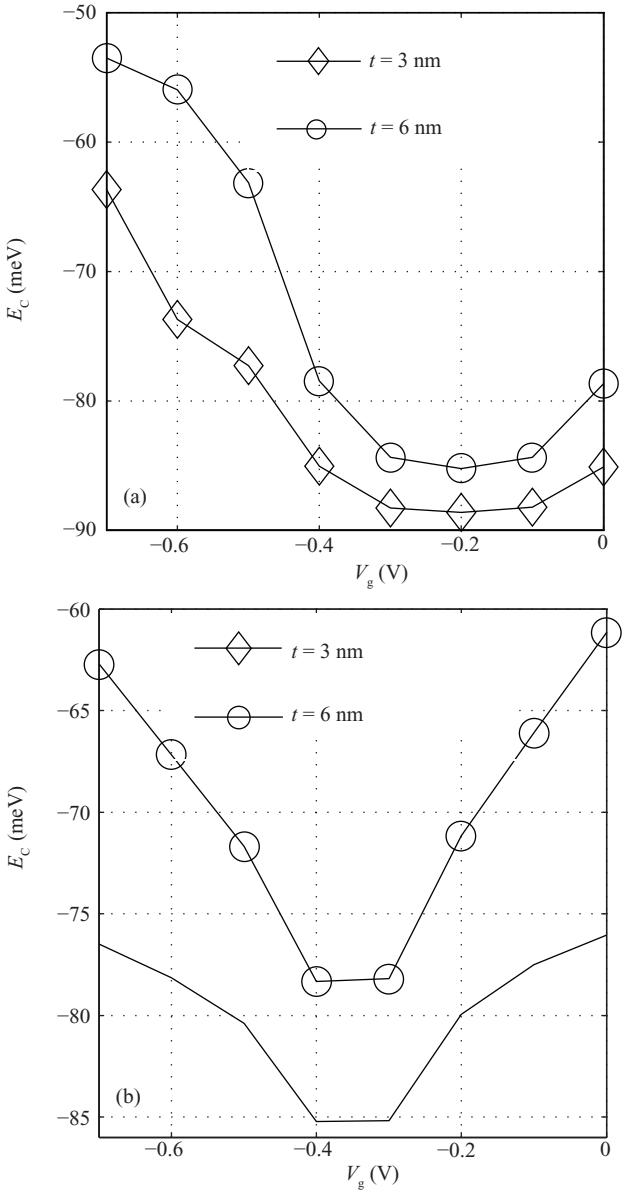

Fig. 6. Impact of insulator thickness on the CNT surface potential in T-CNFETs with V_{DS} of −0.3 V (circle-marked line) and −0.6 V (diamond-marked line).

or electrons can band-to-band tunnel into a channel with different gate bias conditions, T-CNFETs suffer from serious ambipolar conductance. The resulting limited I_{ON}/I_{OFF} ratio, an important figure of merit of FETs, will have a great impact on device performance. In order to reduce such ambipolar conductance in T-CNFETs, a staircase doping strategy is proposed in this paper. A two-dimension schematic view of the proposed device structure is shown in Fig. 7. Coaxial geometry, realizable in realistic application[16], is adopted for simplicity. By controlling the electrostatics of the nanotube environment by molecules[17] or metal ions[18], the left part of the CNT, serving as the source region, is heavily doped with a doping level of ρ_1, as the left "N" labeled rectangle shows. The middle part of the CNT is left intrinsic and serves as the conducting channel, as the "i" labeled rectangle shows. The drain region is composed of two parts, the one near the channel is lightly doped while

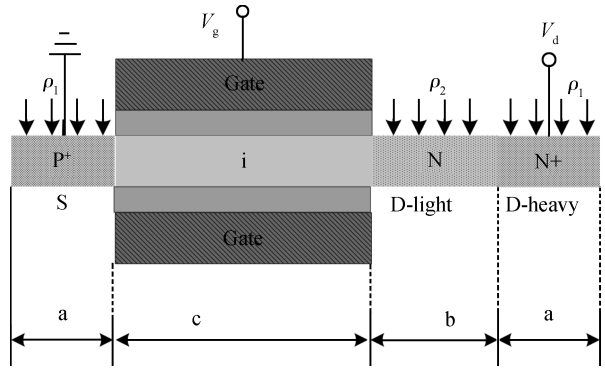

Fig. 7. Two-dimension sketch of the SDT-CNFET device structure.

the one far away from the channel is heavily doped with the same doping level as that in the source region. A coaxial gate is placed around the intrinsic part of the nanotube and separated by an oxide with a thickness of 2 nm. Such a staircase doping profile can be achieved via a multi-doping technique such as multiple steps of modulated chemical doping with appropriate exposed area in the lithography process for each step[19]. Another technique of non-uniform doping has been reported by Afzali-Ardakani *et al.*[20].

For convenience of introduction, the proposed device and conventional T-CNFETs are denoted as "SDT-CNFETs" and "UDT-CNFETs" respectively.

With the parameters as listed in the caption of Fig. 8, the transfer characteristics of both UDT-CNFETs and SDT-CNFETs are simulated as the black and gray lines in the main panel of Fig. 8 respectively. It is clear that not only is there a sharp increase of I_{ON}/I_{OFF} (from 1.6×10^5 to about 1.4×10^{10}) and a distinct reduction of ambipolar conductance, but a slight decrease of sub-threshold slope can also be achieved with our proposed staircase drain doping strategy. With the initiative gate voltage V_0 set to 0.3 V, the average sub-threshold slope of SDT-CNFETs is just 23.3 mV/dec regarding the fact that the threshold voltage is about 0.4 V here, about 39% smaller than that of UDT-CNFETs.

It should be noted that what Fig. 7 and Fig. 8 model is the N-type device. Ideal P-type T-CNFETs can also be obtained with such a staircase doping strategy adopted in the source lead.

6. Conclusion

One of the most attractive merits of T-CNFETs is the ultra-small sub-threshold slope, which is necessary to improve the system frequency and minimize the power consumption in the process of scaling. Several effective approaches have been proposed to improve the sub-threshold performance of T-CNFETs to make them as ideal as possible: tuning the doping level of source/drain leads, minimizing the quantum capacitance value by tuning the bias condition or increasing the insulator capacitance, and adopting a staircase doping strategy in the drain lead. NEGF based simulation results shows that all these measures could contribute to a steeper inverse sub-threshold slope, which is quite desirable in T-CNFET design. Meanwhile, we must note the fact that only quantum capacitance resulting from limited DOS is considered in this paper. In practice, electron interactions play an important role in low-dimensional devices too.

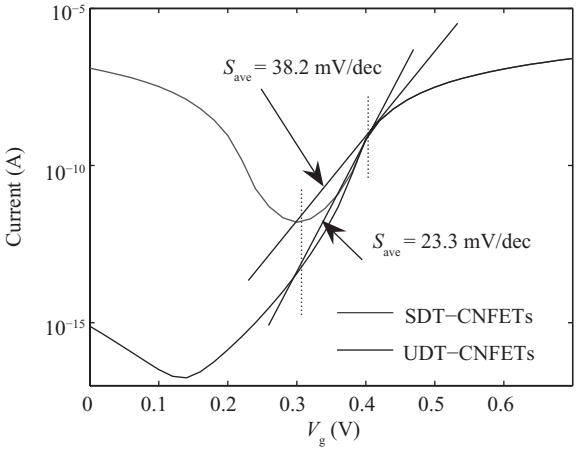

Fig. 8. The transfer characteristics of UDT-CNFETs (gray line) and SDT-CNFETs (black line) with $V_{DS} = 0.6$ V, $a = c = 15$ nm, $b = 30$ nm, $\rho_1 = 4 \times 10^8$ m^{-1}, $\rho_2 = 4 \times 10^6$ m^{-1}.

The existence of a negative capacitance resulting from electron interactions has not only been predicted to exist in theory but also observed in experimental measurements[21−23], and it will be taken into account in our next research work.

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