Simulation for signal charge transfer of charge coupled devices

Wang Zujun(王祖军)^{1,2,†}, Liu Yinong(刘以农)¹, Chen Wei(陈伟)², Tang Benqi(唐本奇)², Xiao Zhigang(肖志刚)², Huang Shaoyan(黄绍艳)², Liu Minbo(刘敏波)², and Zhang Yong(张勇)²

(1 Department of Engineering Physics, Key Laboratory of Particle & Radiation Imaging of Ministry of Education, Tsinghua University, Beijing 100084, China)

(2 Northwest Institute of Nuclear Technology, Xi'an 710024, China)

Abstract: Physical device models and numerical processing methods are presented to simulate a linear buried channel charge coupled devices (CCDs). The dynamic transfer process of CCD is carried out by a three-phase clock pulse driver. By using the semiconductor device simulation software MEDICI, dynamic transfer pictures of signal charges cells, electron concentration and electrostatic potential are presented. The key parameters of CCD such as charge transfer efficiency (CTE) and dark electrons are numerically simulated. The simulation results agree with the theoretic and experimental results.

Key words: CCD; CTE; dark signal; numerical simulation; MEDICI DOI: 10.1088/1674-4926/30/12/124007 EEACC: 2570

1. Introduction

Charge coupled devices (CCD) were first introduced by Boyle and Smith^[1] in 1970. They have a number of advantages, such as low cost, low power consumption, high bit density, and high sensitivity. Their applications include spaceborne astronomy, earth observation, surveillance, laser communications, and star trackers, etc.

In order to study the fundamental physical mechanisms and improve CCD design, CCD simulation was rapidly developed. A simulation system was developed to automatically analyze the basic electric characteristics of CCD image sensors. Using this simulation system, a CCD cell was realized with a high CCD saturation charge quantity of 1.8 times in comparison with conventional, effective transfer efficiency of over 99% and no image lag for driving read-out pulse voltage^[2]. A device simulator, SPECTRA, and an optics simulator, TOC-CATA, were developed for three-dimensional optical and electrical analysis of CCD. This combination enabled the total design of CCD cell structures on and in a silicon substrate^[3]. A complete optoelectronic simulation of a CCD cell structure was presented by means of the finite-difference time domain method^[4]. Some papers introduced fundamental physical mechanisms^[5-7]. However, the dynamic transfer process of CCD by the time-phase clock pulse driver has not been reported.

In this article, dynamic transfer pictures of signal charges cells, electron concentration and electrostatic potential are realized to show the transfer process of CCD operation by numerical simulation. Physical device models and numerical processing methods of a buried channel CCD are presented, which are used to simulate the dynamic transfer process of CCD with a three-phase clock pulse driver. By using the semiconductor device simulation software MEDICI, CTE and dark electrons of CCD are numerically simulated. The device structures are created by use of the mesh of MEDICI. The impurity profiles are created analytically from a Gaussian function. The mobility models and the recombination models of the carriers are chosen from MEDICI for the simulation.

2. Models and methods

2.1. Device structure and simulation models

Typical CCD structures include input structures, charge transfer structures, and output structures. Input structures which include an input dioxide (ID) and an input gate (IG) are used to generate signal charges. Signal charges can also be generated by the photo-electric effect. Charge transfer structures which include a series of MOS capacitances named transfer gates (G1, G2, G3) are used to transfer signal charges by the three-phase clock pulse driver. Output structures, including an output dioxide (OD) and an output gate (OG), are used to output signal charges^[8]. Figure 1 shows the dynamic transfer process of signal charges from electric injection, collection and storage to final output.

The simple CCD model used in the actual simulation is presented in Fig. 2. Figure 3 shows a schematic cross section of CCD. The transfer gates use three separate levels of polysilicon to form a three-phase overlapping semitransparent electrode structure. Signal charges are transferred in an N-buried channel in order to improve $CTE^{[9-11]}$.

The width of CCD for simulation is 26.8 μ m, and the length is 10.0 μ m. The gate dielectric thickness is 0.16 μ m, which includes Si₃N₄ and SiO₂. The thickness of Si₃N₄ is 0.07 μ m, and the thickness of SiO₂ is 0.09 μ m. The input and output gate lengths are both 4 μ m, the transfer gate and left gap lengths are both 4.1 μ m, the input and output dioxide lengths

[†] Corresponding author. Email: wzj029@qq.com

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 $\int_{-\infty}^{\infty} Ground$ Fig. 2. Schematic device structure for CCD transfer. polysilicon 3 polysilicon 1 polysilicon 2 polysilicon 3 polysilicon 1 Gate dielectric Si₃N₄ 0.07 µm SiO₂ 0.09 µm N-buried channel 0.5 µm Doping N_D = 2.6×10¹⁶ cm⁻³ Epitaxial silicon 10 µm Doping N_A = 5.0×10¹⁴ cm⁻³ P-type Si substrate Doping N_A = 5.0×10¹⁹ cm⁻³

P-type Si substrate

Fig. 3. Schematic cross section of the CCD.

are both 4 μ m, and the pixel size is $12 \times 12 \mu$ m². The P-Si substrate doping concentration is 5×10^{14} cm⁻³. The doping concentration of input and output dioxide is 1×10^{19} cm⁻³ with Gauss distribution, and the junction depth is 0.5μ m. The Nburied channel doping concentration is 2.6×10^{16} cm⁻³, and the depth is 0.5μ m. The minority carrier life is 100 ns, and the clock pulse driver frequency is 4 MHz. The back side of CCD is connected to ground.

For the simulation structures and parameters, the meshes of CCD which are shown in Fig. 4 are presented by using MEDICI. Figure 5 shows the 1-D impurity distribution along the vertical direction of CCD transfer gates.

2.2. Clock pulse driver circuit

During charge transfer, the operation voltages of the input and output dioxides are both from 12 to 0 V. The operation voltages of the input and output gates are both from -5 to



Fig. 4. Meshes of the CCD transfer structure.



Fig. 5. 1-D impurity distribution along the vertical direction.

5 V. The operation voltages of all the transfer gates are from -5 to 5 V. The back side of CCD connected to ground is 0 V.

Clock pulse driver circuits are designed to meet the following demands. When time *t* is 10 ns, I_G begins to jump from -5 to 5 V, and the jumping time is 10 ns. The input gate turns on accordingly. Transfer gate G1 begins to jump from -6 to 6 V, and the jumping time is 10 ns, too. A potential well which can store signal charges is formed below G1. When *t* is 20 ns, I_D jumps from 12 to 0 V, and signal charges are injected to the potential well below G1. When *t* is 80 ns, I_D jumps from 0 to 12 V, and signal charge injection is stopped. When *t* is 90 ns, I_G jumps from 5 to -5 V, and the input gate turns off. Now the signal charge cell is finally formed in the potential well below G1.

When t is 120 ns, transfer gate G2 jumps from -6 to 6 V, and then a potential well which can store signal charges is formed below G2. Accordingly, signal charges begin to transfer from the potential well below G1 to G2. When t is 130 ns, transfer gate G1 begins to jump from 6 to -6 V, and the potential well below G1 is gradually shoaled. When t is 150 ns, the potential well below G1 disappears and all the signal charges transfer to the potential well below G2. When t is 210 ns, transfer gate G3 begins to jump from -6 to 6 V, and then a potential well which can store signal charges is formed below G3. When t is 230 ns, transfer gate G2 begins to jump from 6 to -6 V, and then a potential well which can store signal charges is formed below G3. When t is 230 ns, transfer gate G2 begins to jump from 6 to -6 V, and the potential well below G2 is gradually shoaled. When t is 250 ns, the potential well below G2 disappears and all the signal charges transfer to the potential well below G2 disappears and all the signal charges transfer to the potential well below G3. When t is 250 ns, the potential well below G2 disappears and all the signal charges transfer to the potential well below G3. When t is 260 ns, a transfer period is finished, and the next



Fig. 6. Signal charge injection and three-phase clock pulse driver.

transfer period begins. Signal charges are transferred in turn until output.

In order to meet operation demands, the three-phase clock pulse drivers are designed. Figure 6 shows the signal charge injection and three-phase clock pulse driver. The clock pulse driver circuits are as follows:

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Start Circuit
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PCCD 1 = 1 2 = 2 3 = 3 4 = 4 5 = 5 6 = 6 7 =
7 0 = 8 FILE = CCD.MSH Width = 28.6
V1 1 0 PULSE 12 0 20n 10n 10n 40n 250n
V2 2 0 PULSE -5 5 10n 10n 10n 60n 250n
V3 3 0 PULSE -6 6 10n 10n 20n 110n 250n
V4 4 0 PULSE -6 6 110n 10n 20n 110n 250n
V5 5 0 PULSE -6 6 210n 10n 20n 110n 250n
V6 6 0 -5
V7 7 0 12
.NODESET V(0) = 0 V(1) = 12 V(2) = -5 V(3) = -6
V(4) = -6 V(5) = -6 V(6) = -5 V(7) = 12
Finish Circuit
```

2.3. Solution methods

When MEDICI is used for numeric simulation, various models are chosen. Considering the minority carrier life depends on the carrier concentration; the mobility models include concentration-dependent mobility (CONMOB), surface mobility (SRFMOB), and electric field dependent mobility (FLDMOB), etc. The recombination models of carriers include Shockley-Read-Hall recombination (SRH), Auger recombination (AUGER), and direct recombination (DIRECT), etc^[12].

Because an N-buried channel CCD is only necessary to solve Poisson's equation and the electron continuity equation, Newton's method is the most efficient solution technique^[12]. Most electronic CCD modeling is done with the drift-diffusion model, although the simplified hydrodynamic or energy balance models may also be used to account for carrier heating^[13]. The drift-diffusion model consists of Poisson's equation and continuity equations^[12, 14].

Poisson's equation is solved for the electrostatic potential.

Poisson's equation: $\varepsilon \nabla^2 \psi = -q(p - n + N_{\rm D}^+ - N_{\rm A}^-) - \rho_{\rm s}$, where ε is the permittivity, ψ is the electrostatic potential, q is the electron charge, n and p are the electron and hole densities, and $N_{\rm D}^+$ and $N_{\rm A}^+$ are the ionized donor and acceptor densities.

The hole and electron continuity equations are normally solved for the hole and electron concentrations.



Fig. 7. 2D potential contours for no signal charges.



Fig. 8. 2D potential contours for a signal charge cell.

Continuity equations:

$$\begin{aligned} \frac{\partial n}{\partial t} &= \frac{1}{q} \nabla \cdot \boldsymbol{J}_{\mathrm{n}} - (\boldsymbol{U}_{\mathrm{n}} - \boldsymbol{G}_{\mathrm{n}}) = \boldsymbol{F}_{\mathrm{n}}(\boldsymbol{\psi}, n, p),\\ \frac{\partial p}{\partial t} &= -\frac{1}{q} \nabla \cdot \boldsymbol{J}_{\mathrm{p}} - (\boldsymbol{U}_{\mathrm{p}} - \boldsymbol{G}_{\mathrm{p}}) = \boldsymbol{F}_{\mathrm{p}}(\boldsymbol{\psi}, n, p), \end{aligned}$$

where J_n and J_p are the electron and hole current densities, and U_n and U_p are the electron and hole recombination rates. G_n and G_p are the electron and hole generation rates.

Current density equations:

$$\boldsymbol{J}_{\mathrm{n}} = q\mu_{\mathrm{n}}\boldsymbol{n}\,\boldsymbol{E} + q\boldsymbol{D}_{\mathrm{n}}\,\nabla\,\boldsymbol{n},$$
$$\boldsymbol{J}_{\mathrm{p}} = q\mu_{\mathrm{p}}\boldsymbol{p}\,\boldsymbol{E} - q\boldsymbol{D}_{\mathrm{p}}\,\nabla\,\boldsymbol{p},$$

where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusion coefficients, and *E* is the electric field.

3. Simulation for signal charge transfer

3.1. 2D potential contours of signal charges formed and transferred

Before a signal charge cell is formed, the 2D potential contours show no signal charge cell in Fig. 7. After the signal charge cell is injected to the potential well below G1, the 2D potential contours show that a signal charge cell is formed in Fig. 8, which is a close potential contour. Figure 9 shows the 1D potential distribution before signal charge injection. The 1D potential distribution in Fig. 9 indicates that there is an empty potential well formed below G1, which can store the signal charges. After the signal charge cell is injected to the potential well below G1, the top of the 1D potential distribution is

4



Fig. 9. 1D potential distribution for no signal charges.



0.4

0.2

-0.2

-0.4

2

3

Distance (µm)

Potential (V)

Fig. 11. Signal charge cell is formed and transferred: (a) Signal charge cell is formed in G1 potential well; (b) Signal charge cell is transferring from G1 to G2; (c) Signal charge cell is transferred to G2; (d) Signal charge cell begins to transfer to G3; (e) Signal charge cell is transferring from G2 to G3; (f) Signal charge cell is transferred to G3.



Fig. 12. Electron concentration distribution of signal charge cell formation and transfer: (a) Electron concentration distribution for no signal charges; (b) Signal charges are formed in G1 potential well; (c) Signal charges are transferring from G1 to G2; (d) Signal charges are transferred to G2; (e) Signal charges are transferring from G2 to G3; (f) Signal charges are transferred to G3.

flat, because the signal charge cell is a close potential contour where the electrostatic potential is equal. The phenomena in Figs. 9 and 10 agree with the results of $Xiong^{[15]}$. In Figs. 7 to 10, visual signs of signal charge cell formation are displayed, and the location of the signal charge cell is clear in the N-buried channel. With the three-phase clock pulse driver, signal charges begin to transfer from the potential well below G1 to G3. Figure 11 shows that the signal charge cell is formed and transferred.

3.2. Electron concentration distribution of signal charges formed and transferred

Before the signal charge cell is formed, the electron concentration distribution in Fig. 12(a) shows that there is no signal charge cell below any of the transfer gates. After the signal charge cell is injected to the potential well below G1, the electron concentration distribution in Fig. 12(b) shows that a signal charge cell is formed. The electron concentration of the potential well below G1 is sharply increased. With the threephase clock pulse driver, signal charges began to transfer from the potential well below G1 to G2. The electron concentration distribution in Fig. 12(c) shows the transfer process of the signal charge cell. Figure 12(d) shows that signal charges have been completely transferred to the G2 potential well. From Fig. 12(d), it is clear that the electron concentration in the potential well below G2 is higher than G1 and G3. Figure 12(e) shows that signal charges are transferring from potential well G2 to G3. Figure 12(f) shows that signal charges have been completely transferred to G3 potential well. From Fig. 12, the dynamic transfer process of the signal charge cell is displayed by the change of electron concentration below all the transfer gates. The dynamic transfer process of Fig. 12 agrees with the results of Yu^[16]. The change of electron concentration below transfer gates confirms that the signal charge cell is certainly

transferred.

3.3. Electrostatic potential distribution of signal charges formed and transferred

The operation of CCD must firstly form the potential well below the transfer gates, and otherwise signal charges cannot be stored and transferred. Once the potential well below the transfer gates is formed, the electron concentration distribution can change accordingly. Figure 13(a) shows the electrostatic potential distribution for no signal charges. There is no potential well formed below any of the transfer gates. Figure 13(b) shows that a potential well is formed below G1 for storing signal charges. Figure 13(c) shows that a potential well is formed below G2 for storing signal charges transferred from G1. Figure 13(d) shows that a potential well is formed below G3 for storing signal charges transferred from G2.

4. Simulation results

4.1. Charge transfer efficiency

Charge transfer efficiency (CTE) is a key measure of CCD performance. CTE is defined as the ratio of the total charge successfully transferred out of a phase to the initial amount of charge present in the phase before the transfer^[5]. The formula of CTE is CTE = $[Q(G2)/Q(G1)] \times 100\%$, where Q(G1) is the initial amount of charge present in the phase before the transfer, and Q(G2) is the total charge successfully transferred out of a phase. Because several thousand transfers are required in a large sensor, designs typically require a CTE of 99.999% or higher^[5]. CTE is determined by many factors, including the size of the signal charge cell, the length of the phase, the presence of obstacles such as barriers and wells along with the charge transfer path, the time allowed for the transfer, etc^[17, 18].



Fig. 13. Electrostatic potential well below transfer gate is formed: (a) Electrostatic potential distribution for no potential well; (b) Potential well is formed below G1 for storing signal charges; (c) Potential well is formed below G2 for storing signal charges; (d) Potential well is formed below G3 for storing signal charges.



Fig. 14. Electron concentration distribution in G2 potential well with different sizes of signal charge cells: (a) Electron concentration is higher; (b) Electron concentration is high; (c) Electron concentration is low.

Table 1. Numerical simulation values of CTE wh	hen injecting different	signal charge cell size	s.
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Number of electrons in signal	Signal charges in the potential	Signal charges in the potential	Charge transfer efficiency
charges (10 ⁵)	well below G3 $(10^{-14}C)$	well below G5 $(10^{-14}C)$	(CTE) (%)
3.14004	5.02406926	5.02406719	99.999979
3.07312	4.91699750	4.91699508	99.999975
2.91971	4.67153469	4.67153132	99.999964
2.67753	4.28404506	4.28404000	99.999941
2.44174	3.90678786	3.90678170	99.999921
2.29555	3.67287438	3.67286801	99.999913
2.06665	3.30664124	3.30663489	99.999904
1.81792	2.90866784	2.90866087	99.999880
1.58144	2.53030279	2.53029462	99.999839
1.32209	2.11533745	2.11532804	99.999778
1.07356	1.71768996	1.71767999	99.999710
0.85220	1.36351666	1.36350496	99.999571
0.72029	1.15247122	1.15245924	99.999480
0.64691	1.03506288	1.03505115	99.999433
0.57913	0.92661346	0.92660190	99.999376
0.54025	0.86439318	0.86438091	99.999290
0.42956	0.68729086	0.68727891	99.999131
0.32236	0.51577545	0.51576318	99.998811
0.28620	0.45792367	0.45791136	99.998656
0.26680	0.42688704	0.42687472	99.998557
0.25621	0.40994394	0.40993161	99.998496
0.24557	0.39290985	0.39289750	99.998428
0.23041	0.36865200	0.36863964	99.998324



Fig. 15. CTE variation with signal charge cell size.

Table 2. Number of dark electrons in the potential well with different N-buried channel doping concentrations.

N-buried channel doping concentration $(10^{16} \text{ cm}^{-3})$	2.55	2.56	2.57	2.58	2.59	2.60
Number of dark electrons in	8522	6888	5256	3625	1994	361
the potential well (e ⁻)						

In this article, CTE which varies with signal charge cell size is presented. Table 1 presents the numerical simulation results of CTE when injecting different sizes of signal charge cells. Figure 14 shows the electron concentration distribution in G2 potential well with different sizes of signal charge cells. A signal charge cell is transferred twice, namely, the signal charge cell is transferred first from G1 to G2, and then from G2 to G3. So the formula of CTE is CTE = $[Q(G3)/Q(G1)]^{1/2} \times 100\%$.

Figure 15 shows how CTE varies with signal charge cell size. When the signal charge cell size is bigger, CTE is higher. Though the signal charge cell size is bigger, and perhaps the total charge remaining in the phase is greater, the ratio of the total charge remaining in the phase to the initial amount of charge in the phase before the transfer is still smaller. The experimental results of CTE are between 99.99% and 99.9999%, and the typical measurement value is 99.999%. CTE increases with signal charge cell size, as is well known. The experimental result of CTE in Ref. [19] also shows that CTE increases with signal charge cell size.

4.2. Dark electrons

Dark electrons are defined as the electrons accumulating in the potential well under the pixels even with no signal charge injection by both light and electricity. Table 2 presents the numerical simulation results of dark electrons when different N-buried channel doping concentrations are chosen. Figure 16 shows how dark electrons in the potential well below G2 vary with N-buried channel doping concentration. When N-buried channel doping concentration is 2.6×10^{16} cm⁻³, the dark electron experimental measurement is about 300 e⁻.

5. Conclusion

In this article, simulation models and methods for CCD are introduced. By using the semiconductor device



Fig. 16. Dark electrons in potential well below G2 vary with N-buried channel doping concentration.

simulation software MEDICI, the dynamic transfer process of CCD with a three-phase clock pulse driver is simulated. The dynamic process of signal charges formed and transferred is displayed by the 2D potential contours, the electron concentration distribution, and the electrostatic potential distribution. Finally, the variation of CTE with signal charge cell size and the variation of dark electrons in the potential well below G2 with N-buried channel doping concentration is also presented.

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