A 1.5 Gb/s monolithically integrated optical receiver in the standard CMOS process*

Xiao Xindong(肖新东)†, Mao Luhong(毛陆虹), Yu Changliang(余长亮), Zhang Shilin(张世林), and Xie Sheng(谢生)

(School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China)

Abstract: A monolithically integrated optical receiver, including the photodetector, has been realized in Chartered 0.35 μm EEPROM CMOS technology for 850 nm optical communication. The optical receiver consists of a differential photodetector, a differential transimpedance amplifier, three limiting amplifiers and an output circuit. The experiment results show that the receiver achieves an 875 MHz 3 dB bandwidth, and a data rate of 1.5 Gb/s is achieved at a bit-error-rate of 10^{-9}. The chip dissipates 60 mW under a single 3.3 V supply.

Key words: optical receiver; TIA; photodetector; CMOS
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1. Introduction

Internet and multimedia applications have demanded a network communication system to support high speed data transmission up to a Gbit/s range. For high speed data transmission systems, electrical interconnection was the bottleneck of high frequency application because of its intrinsic RC time constant transmission delay. Nowadays, because optical interconnection can overcome the bottleneck of electrical interconnection, research into optical receivers has seen much progress[1].

In recent years, a lot of research into optical receivers (not monolithically integrated) has been reported[2, 3], where OC-192 chips (10 Gb/s) have been obtained by 0.13 μm CMOS technology[4]. Nevertheless, photodetectors in these optical receivers are implemented in III–V materials for high performance, the high cost of which confines its applications to shorter transmission. Because the cost of packaging and fabricating is greatly reduced in the standard CMOS process, much more attention in optical receiver research has been given to monolithically integrated CMOS optical receivers. A 1 Gb/s optical receiver with a−6 dBm sensitivity for λ = 850 nm in the 0.35 μm standard CMOS process was first reported by the Bell laboratory[5]. The low sensitivity of the optical receiver does not satisfy the communication need. Also, a 3 Gb/s optical receiver with a−19 dBm sensitivity in the 0.18 μm standard CMOS process was implemented by Saša Radovanović[6]. Four equalizers of this optical receiver not only sacrifice a lot of area and power, but also lead to the instability of the receiver.

In this paper a design for a monolithically integrated CMOS optical receiver for 850 nm optical communication is presented. Section 2 presents the design and analysis of a differential photodetector which can improve the sensitivity of the receiver in the standard CMOS process. Section 3 presents the front-end circuit of the optical receiver, consisting of a differential transimpedance amplifer (TIA), three limiting amplifiers and an output circuit. The active inductor which occupies a very small area and dissipates little power is applied to enhance the bandwidth of the front-end circuit.

2. Design of optical detector

The whole architecture of the optical receiver is shown in Fig. 1, which integrates a differential photodetector, a differential TIA, three differential limiting amplifiers and an output buffer. A differential photodetector, which can provide differential input current for the TIA, consists of a P+/DNwell photodiode and an N+/DPwell photodiode. Due to the relatively low responsivity of the P+/DNwell photodiode and a N+/DPwell photodiode, an automatic gain control circuit is not needed in this architecture.

In a conventional differential optical receiver, only one illuminated photodetector provides input current for it. This asymmetry of the conventional architecture reduces the bandwidth of the optical receiver. A dummy diode or capacitor can be added to improve the receiver bandwidth by eliminating the

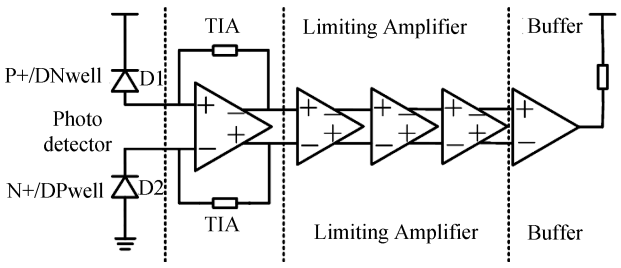

Fig. 1. Optical receiver with integrated photodiode architecture.

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† Corresponding author. Email: xxd@tju.edu.cn

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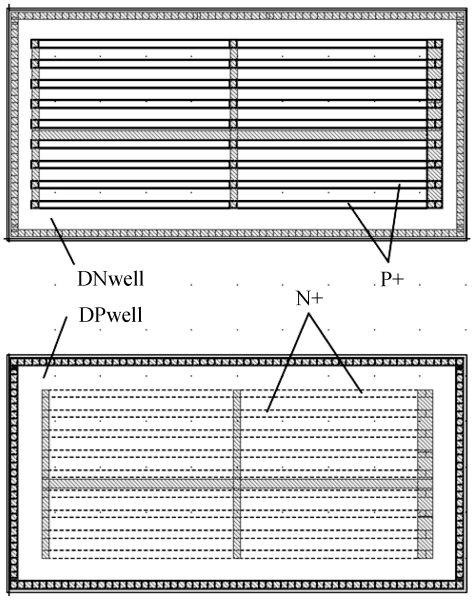

Fig. 2. Layout of the differential detector.

asymmetry. In order to boost the bandwidth and the sensitivity of the optical receiver, a differential detector consisting of two similar photodiodes is used in the differential receiver[7]. The layout of the differential detector is shown in Fig. 2. One 60×30 μm^2 P+/DNwell photodiode, D1 in Fig. 1, is connected to the positive input of the differential TIA, while another 60×30 μm^2 N+/DPwell photodiode, D2 in Fig. 2, is connected to the negative input of the differential TIA. The DNwell and DPwell diode, compared to the Nwell diode, has a higher responsivity. The P+ and N+ region is implemented by a finger structure to further enhance the responsivity of the photodiode. Because the two photodiodes are placed side by side in the layout, they can acquire light from only one laser light.

Slow carrier diffusion in deep substrate is avoided by the DNwell region to enhance the bandwidth of the P+/DNwell detector[8]. Reference [6] reported that the bandwidth of the P+/Nwell photodiode is 3 GHz in the 0.18 μm standard CMOS process. So, the bandwidth of the P+/DNwell photodiode and an N+/DPwell photodiode is in the gigabit range. However, because the slow carriers from the deep substrate do not contribute to the photocurrent, the responsivity of the detector is decreased.

3. Front-end amplifier

The schematics of the TIA, the limiting amplifier and the output buffer are shown in Figs. 3(a), 3(b), and 3(c), respectively. The differential TIA is used to convert the photocurrent into a voltage signal. The voltage signal from the TIA is further amplified by the limiting amplifier. The output buffer, a differential to single-ended circuit, is used to drive and match the measuring instrument.

To alleviate bandwidth degradation caused by the capacitance of the photodiode, a common source gain amplifier with a shunt-feedback resistor is adopted. The MOS resistors MR1 and MR2 are used to replace the conventional resistors in the

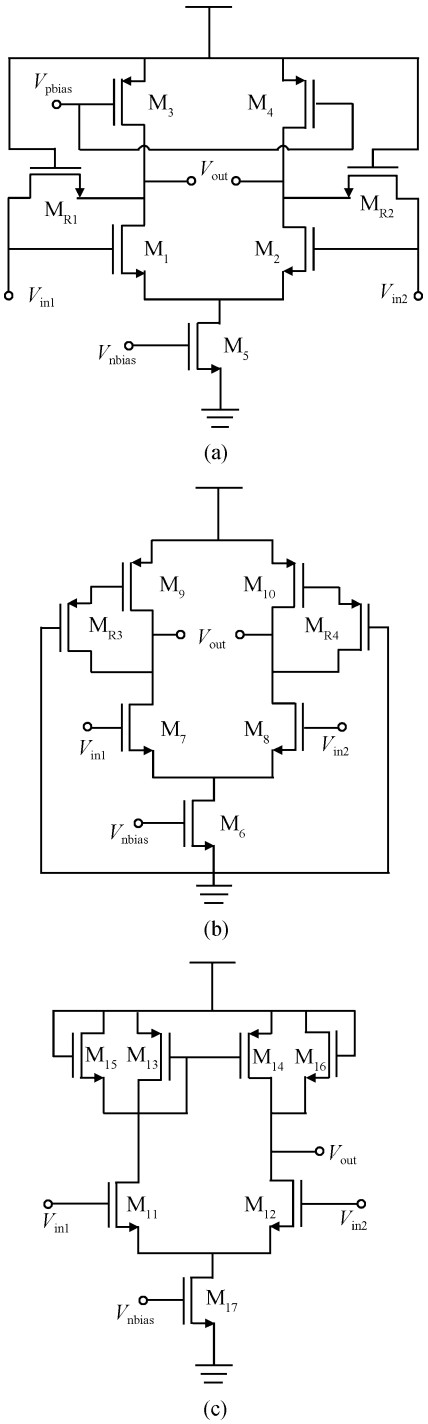

Fig. 3. (a) Schematic of the TIA; (b) Schematic of the one stage limiting amplifier; (c) Schematic of the output buffer.

TIA which are not accurate. Compared to the resistor in the CMOS process, the MOS resistor is more accurate and less influenced by process corner. The transimpedance gain is mainly offered by the MOS resistors MR1 and MR2. The bandwidth of the TIA is decided by the capacitance of the photodetector and the MOS resistors MR1 and MR2. Due to the simple architecture of the TIA, the input noise current of the receiver is very low. By increasing the W/L of the MOS transistor M1 and M2, increasing the MOS resistor MR1 and MR2 and decreasing the W/L of the MOS transistor M3 and M4, the input noise current could be minimized. The performance of the bit error rate is improved by reducing the TIA input noise current.

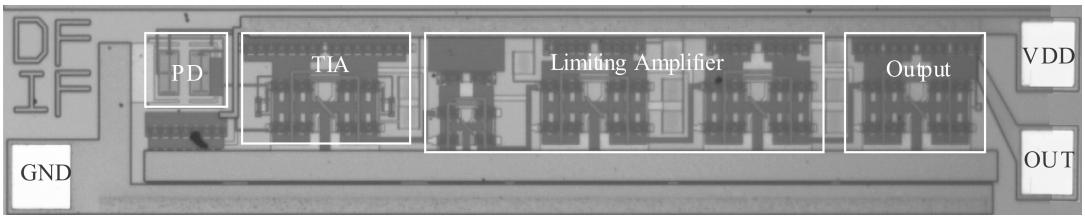

Fig. 4. Micrograph of the chip.

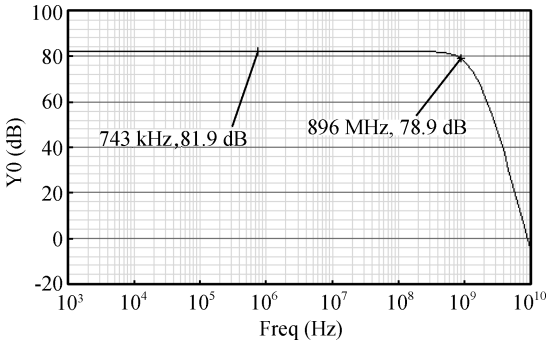

Fig. 5. Simulated frequency response of the receiver.

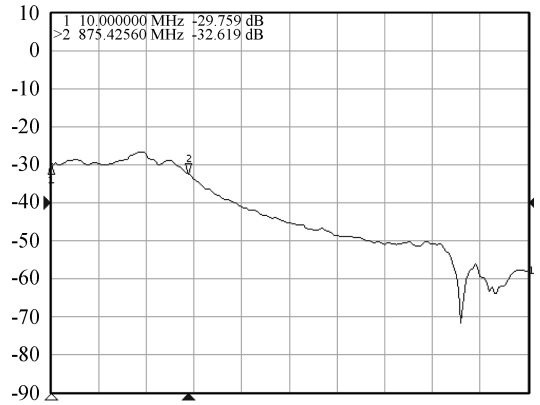

Fig. 6. Measured frequency response of the receiver.

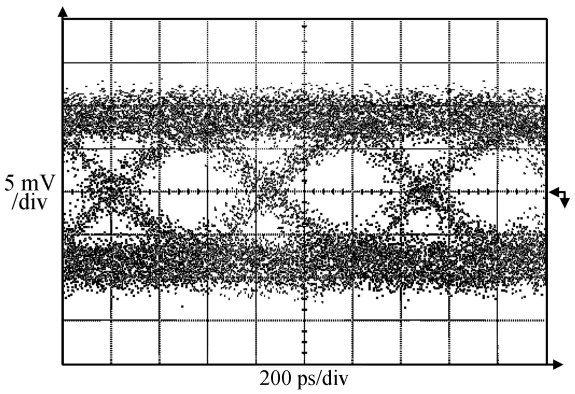

Fig. 7. Measured eye diagram at 1.5 Gb/s.

Considering the relatively low responsivity of the photodiode, the noise of the TIA should be low. On the other hand, the smaller MOS resistors MR1 and MR2 could increase the bandwidth of the receiver. Finally, the TIA provides a conversion gain of about 60 dBΩ for a trade-off consideration, and its 3 dB bandwidth is about 1.35 GHz.

In the three limiting amplifiers, the gain of every stage is the square root of e in order to alleviate the decreasing bandwidth of the multistage amplifier. In addition, folded active inductors[9] are applied in the limiting amplifier to increase its bandwidth. The conventional resistors in folded active inductors are replaced by the MOS resistors. Usually, the resistor in a folded active inductor occupies a lot of area and it is easily influenced by process conditions. The MOS resistor could save a lot of area compared with the poly resistor. The 3 dB bandwidth of the three limiting amplifiers is about 3.3 GHz, and the total gain is about 20 dB.

The high bandwidth of the differential to single-ended output buffer is realized by the two NMOS diodes in parallel with the current mirror. The differential to single-ended output buffer has the advantage of not decreasing the gain of the receiver compared with the conventional buffer. The bandwidth of the output buffer is 2.05 GHz, and its gain is about 2 dB.

4. Experimental results

The optical receiver with a monolithically integrated photodetector is realized in the Chartered 0.35 μm EEPROM CMOS process. No additional masks or reflective coatings have been used to improve the photodiode performance. The chip micrograph is shown in Fig. 4, where the core size is 1300×220 μm^2. The total power of the chip is 60 mW under a single 3.3 V supply. The simulated AC response results of the receiver are shown in Fig. 5, which are obtained by Cadence Spectre. In Fig. 5, the optical receiver provides a transimpedance gain of 81.9 dBΩ, and the overall 3 dB bandwidth is 896 MHz.

An Agilent E5062A network analyzer, Agilent ParBERT 81250, New Focus Model 1780 10Gb/s VCSEL and Agilent 86100C Infiniium DCA-J are used to measure the receiver performance. The measured frequency response result in Fig. 6 shows that the receiver achieves 875 MHz 3 dB bandwidth, which is basically consistent with the simulated result. Figure 7 shows the measured eye diagram at 1.5 Gb/s data rates for a $2^{31}-1$ pseudorandom bit sequence (PRBS). The eye diagram is wide open, and its amplitude is about 20 mV.

5. Conclusion

An optical receiver with a monolithically integrated differential photodetector has been implemented in an unmodified 0.35 μm CMOS process. A differential photodetector is adopted to increase the bandwidth and sensitivity of the optical receiver. The measured result shows that a bandwidth of 875 MHz and a transimpedance gain of 81.9 dBΩ are realized by the receiver. A data rate of 1.5 Gb/s is achieved by the receiver with a bit error rate of 10^{-9}.

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