A high performance 90 nm CMOS SAR ADC with hybrid architecture*

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Abstract: A 10-bit 2.5 MS/s SAR A/D converter is presented. In the circuit design, an R-C hybrid architecture D/A converter, pseudo-differential comparison architecture and low power voltage level shifters are utilized. Design challenges and considerations are also discussed. In the layout design, each unit resistor is sided by dummies for good matching performance, and the capacitors are routed with a common-central symmetry method to reduce the nonlinearity error. This proposed converter is implemented based on 90 nm CMOS logic process. With a 3.3 V analog supply and a 1.0 V digital supply, the differential and integral nonlinearity are measured to be less than 0.36 LSB and 0.69 LSB respectively. With an input frequency of 1.2 MHz at 2.5 MS/s sampling rate, the SFDR and ENOB are measured to be 72.86 dB and 9.43 bits respectively, and the power dissipation is measured to be 6.62 mW including the output drivers. This SAR A/D converter occupies an area of 238 × 214 μm^2. The design results of this converter show that it is suitable for multi-supply embedded SoC applications.

Key words: analog-to-digital converter; CMOS integrated circuits; level shifters; multi-supply SoC; high performance
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1. Introduction

With the improvement of system-on-chip (SoC) technology, A/D converters are widely used. SAR A/D converters are especially popular for SoC design due to their simple architectures, small areas and eaziness to be integrated with other IC blocks[1−7]. Either charge redistribution or voltage scaling method can be used to implement the internal D/A converter, which is an essential part of the SAR A/D converter. However, for these two types of SAR A/D converters, with the resolution increasing, the total number of passive components in their D/A converters will also increase exponentially. So many resistors or capacitors make it difficult for them to occupy a small area. For a voltage scaling SAR A/D converter with more than 8-bit resolution, high performance is always hard to achieve due to the correspondingly bad matching performance of resistors, which makes it unpopular for embedded SoC applications[8−10]. For a charge redistribution SAR A/D converter, to reduce the chip area, small capacitors must be used. But additional calibration techniques should be utilized to guarantee the linearity of the converter, thus increasing the total power dissipation and circuit complexity[11]. With silicon feature dimensions downscaling into the nanometer scale, more stringent requirements such as low power and small area must be satisfied simultaneously for data converters in SoC applications. But for most previous works, it is hard for them to satisfy these requirements simultaneously[3, 5]. Therefore, research is still needed on high performance SAR A/D converters.

In this paper, by using an R-C hybrid architecture D/A converter, pseudo-differential comparison architecture, and low power voltage level shifters, a 10-bit SAR A/D converter is realized based on 90 nm CMOS logic process. With the combination of a 7-bit resistor ladder and an 8:1 capacitor pair, 10-bit resolution is achieved. Due to the inherent sample and hold function of the capacitor, no additional S/H circuit is needed. Good matching performance is achieved by careful layout design where the resistor ladder is sided by dummies, and the capacitor array is routed with a common-central symmetry method. The measurement results show that this proposed converter achieves high performance and it is very suitable for multi-supply embedded SoC applications.

2. Basic principle of SAR ADC

A typical SAR A/D converter is illustrated in Fig. 1. It consists of an S/H circuit, a comparator, a SAR control unit and a D/A converter. Its operation is based on a "binary search" algorithm. The analog input is sampled and compared with the output of the D/A converter, which is under the control of the logic circuit. The reference voltage at particular stages de-

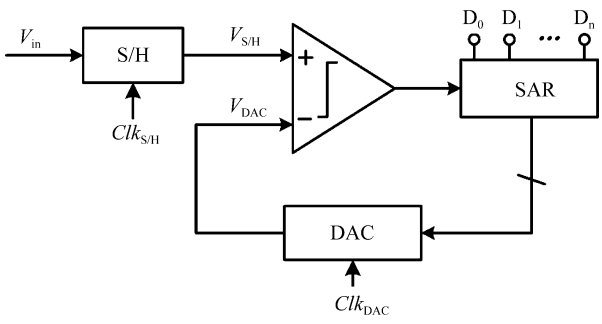

Fig. 1. Typical SAR ADC architecture.

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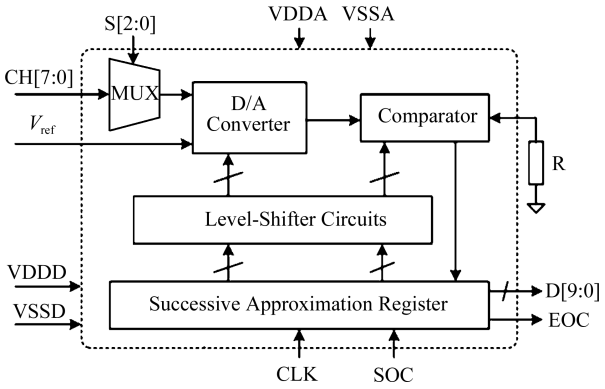

Fig. 2. Functional block diagram of the proposed SAR ADC.

pends on the value of the calculated bit. The reference voltage is calculated with the formula: $b_{n-1}V_{ref}/2^1 + b_{n-2}V_{ref}/2^2 + b_{n-3}V_{ref}/2^3 + \cdots + b_0V_{ref}/2^n$, where n is the resolution of the converter. The digital outputs can then be sequentially generated by these comparisons.

3. SAR ADC circuit design

As seen in Fig. 2, the main blocks of this proposed SAR ADC are level shifters, D/A converter, comparator and SAR control logic circuit. In Fig. 2, VDDA represents a 3.3 V analog supply while VDDD is the 1.0 V digital supply. CLK is the clock of this converter and SOC (start of conversion) represents the signal that controls sampling. CH [7:0] represents the eight input channels which are controlled by the selecting signal S [2:0]. V_{ref} represents the voltage reference of the converter. A 25 kΩ external resistor R is used to provide bias current for the comparator. EOC is used for ending the conversion and D [9:0] is the 10-bit digital output. The level shifters are used to convert the low voltage control signals to a higher level for the analog circuit application.

3.1. Low power voltage level shifter

The level shifter is an important building block for multi-supply SoC applications. As we know, with a given noise floor, a low operating voltage makes high dynamic range design difficult. To overcome the problem, operation under multiple supplies is a selection for nanometer scale SoC applications. In this design, to achieve high input dynamic range and high signal to noise ratio, a 3.3 V analog supply and 3.3 V voltage reference are used and the digital circuits operate under the 1.0 V digital supply. This makes the level shifters very important in this design, because many control signals generated by the SAR control logic should be used to control the operation of the internal DAC and comparator. Therefore, some low to high voltage level shifters should be utilized to convert these digital control signals to a higher analog voltage level. Low power level shifter design is also significant for reducing the power dissipation of the ADC.

Figure 3(a) is the traditional voltage level shifter structure. The disadvantages of this approach are low speed and high power dissipation. Due to their low speed of the input transistors M_3 and M_4, the PMOS M_7 cannot be turned off immediately when the node A_0 needs to discharge. Thus, a long time

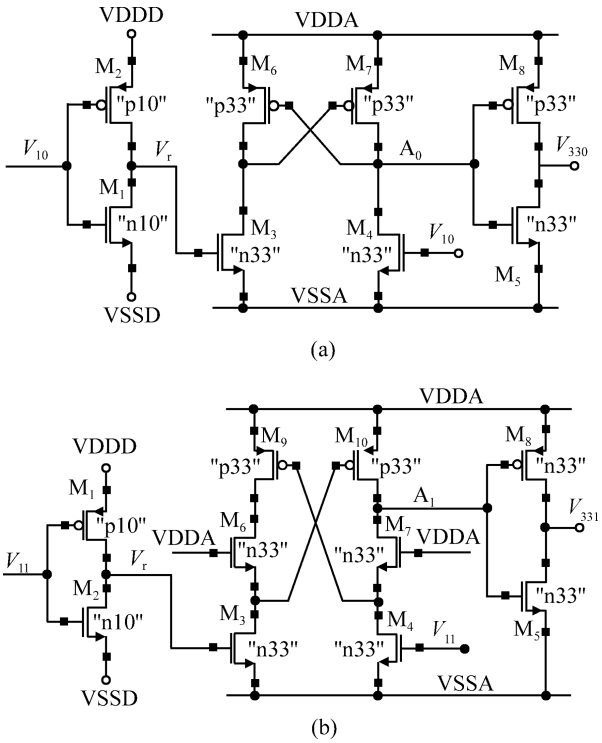

Fig. 3. Voltage level shifter. (a) Traditional structure. (b) Low power structure.

delay exists and it consumes too much power. In this paper, low power architecture is utilized, as shown in Fig. 3(b). The gate control voltages of M_9 and M_{10} are lower than those of M_6 and M_7 in Fig. 3(a). Then, when the node A_1 needs to discharge, M_{10} can be turned off with a higher speed. Therefore, this approach is characterized by high speed and low power dissipation. Figure 4 shows the simulation results based on 90 nm CMOS 3.3 V/1.0 V technology. From Fig. 4(a), the delay time of the level shifter with low power structure is very small. Figure 4(b) shows the variation of the current flow through the cross-coupled PMOS transistors in both structures. Since more transistors are stacked between the VDDA and VSSA, and conversion time has been dramatically reduced, the dynamic current and its duration are both less than the traditional approach. In this SAR A/D converter, eighteen voltage level shifters are utilized to convert the low voltage (1.0 V) control signals to a higher level (3.3 V) for analog circuit application.

3.2. Internal DAC design and discussion

In the SAR A/D converter, the D/A converter is one of the most critical blocks. As in the description in section 1, either charge redistribution or voltage scaling method can be used to implement the internal D/A converter. But both of these two approaches cannot easily realize low power dissipation and small area simultaneously. In this SAR A/D converter, a hybrid architecture D/A converter is utilized, as shown in Fig. 5. Compared with traditional topologies, this approach can obviously reduce the number of passive components and chip area, which is more significant in embedded SoC applications.

In Fig. 5, a 7-bit resistor ladder and an 8 : 1 capacitor pair are combined to realize 10-bit resolution. V_M represents the output of the 7-bit voltage scaling D/A converter while V_L is

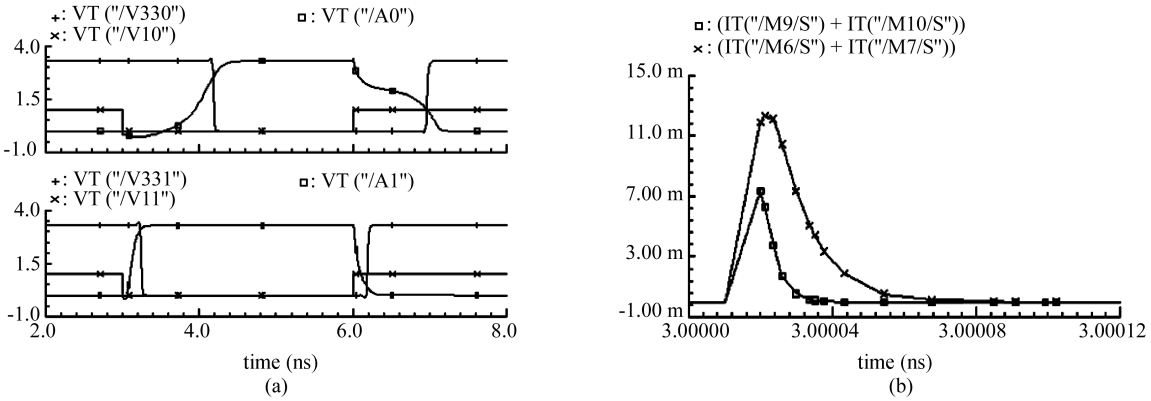

Fig. 4. Voltage level shifter simulation results with (a) speed and (b) power.

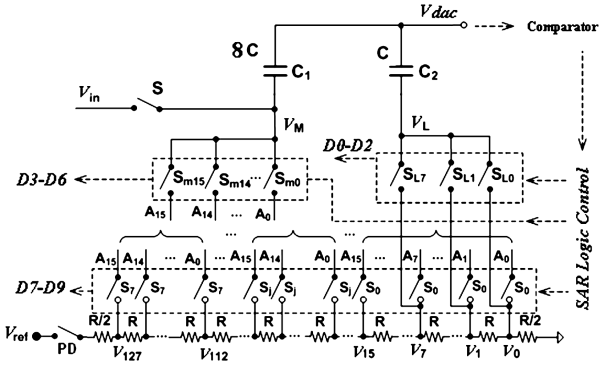

Fig. 5. Architecture of the internal D/A converter.

the output value of its last three bits, and $C_1 = 8C$, $C_2 = C$. Here, C represents the unit capacitor. In the sampling phase, with the switch S turned on, the analog input V_{in} is sampled by capacitor C_1 while V_{L} is connected to V_5 which has a voltage value of $9V_{\text{ref}}/256$. In the conversion phase, V_{M} is connected to C_1 and V_{L} is connected to C_2. Then, with the approximation principle of the SAR A/D converter, at the end of the conversion phase, we have:

$$V_{\text{in}} \times 8C + V_5 \times C = V_{\text{M}} \times 8C + V_{\text{L}} \times C. \tag{1}$$

After a rearrangement, we can get:

$$V_{\text{in}} = V_{\text{M}} + \frac{1}{8}(V_{\text{L}} - V_5). \tag{2}$$

With the substitution of $V_{\text{M}} = \frac{V_{\text{ref}}}{128}\left(\sum_{i=3}^{9} D_i \times 2^{i-3} + \frac{1}{2}\right)$ and $V_{\text{L}} = \frac{V_{\text{ref}}}{128}\left(\sum_{i=0}^{2} D_i \times 2^{i} + \frac{1}{2}\right)$ into Eq. (2), we can approximate V_{in} as below:

$$V_{\text{in}} = \frac{V_{\text{ref}}}{1024}\sum_{i=0}^{9} D_i \times 2^i. \tag{3}$$

The speed of the SAR A/D converter is mainly limited by the settling time of the D/A converter and the comparator. Within a specified time, they must settle to within the resolution of the overall A/D converter. For the topology, attention has been paid to ensuring that the capacitances of the lower plate switches do not affect the accuracy of the conversion because every node is driven to a final voltage, but the switch-on resistances of these switches can affect the conversion rate. Therefore, these switches should be optimized to avoid errors caused by long delay times.

Another consideration is that since the resistor ladder is inherently monotonic, the first 7-bits obtained from the resistor ladder are monotonic regardless of any resistor mismatch. This implies that the capacitor pair has to be ratio-accurate to only 3-bits and can still provide 10-bit monotonic conversion. Therefore, the matching requirements for capacitors are relaxed. Also, since only two capacitors are used in this approach, it is easy to satisfy the matching requirements for them. Thus, to reduce the chip area and increase the conversion rate, small capacitors can be selected. Though the resistor ladder is inherently monotonic and only 3-bit ratio-accuracy is needed for the two capacitors to satisfy the monotonicity, the values of these passive components still need to be carefully selected to satisfy the specified linearity. Attention should also be paid to the trade-off between conversion rate and power consumption, where large resistors and capacitors cannot realize a high conversion rate because of large time constants, and resistors that are too small will consume too large power dissipation and can hardly realize good linearity[12, 13]. Considering that the most significant bits are realized by the resistor ladder, we choose a larger R to improve the matching performance, which is allowable and reasonable for only $256 \times R/2$ is utilized in the 10-bit D/A converter.

3.3. Comparator design considerations

Besides the D/A converter, the comparator also has a crucial influence on the overall performance in the SAR A/D converter. In this paper, the comparator is realized with two cascaded preamplifier stages followed by a latch stage. Figure 6(a) is the comparator diagram. The negative port of the comparator is connected to the D/A converter while the positive port is connected to a dummy capacitor array. With this pseudo-differential architecture, the errors caused by clock feedthrough and charge injection can be considered as common-mode interferences, so the performance is improved.

In the sampling mode, the comparator is auto-zeroed with A_z turned on, $V_{\text{ip}} = V_{\text{in}}$. No additional sample-and-hold circuit is needed because C_1 is used as the sampling capacitor in this sampling mode. Shunt capacitors C_3 are operated as a ca-

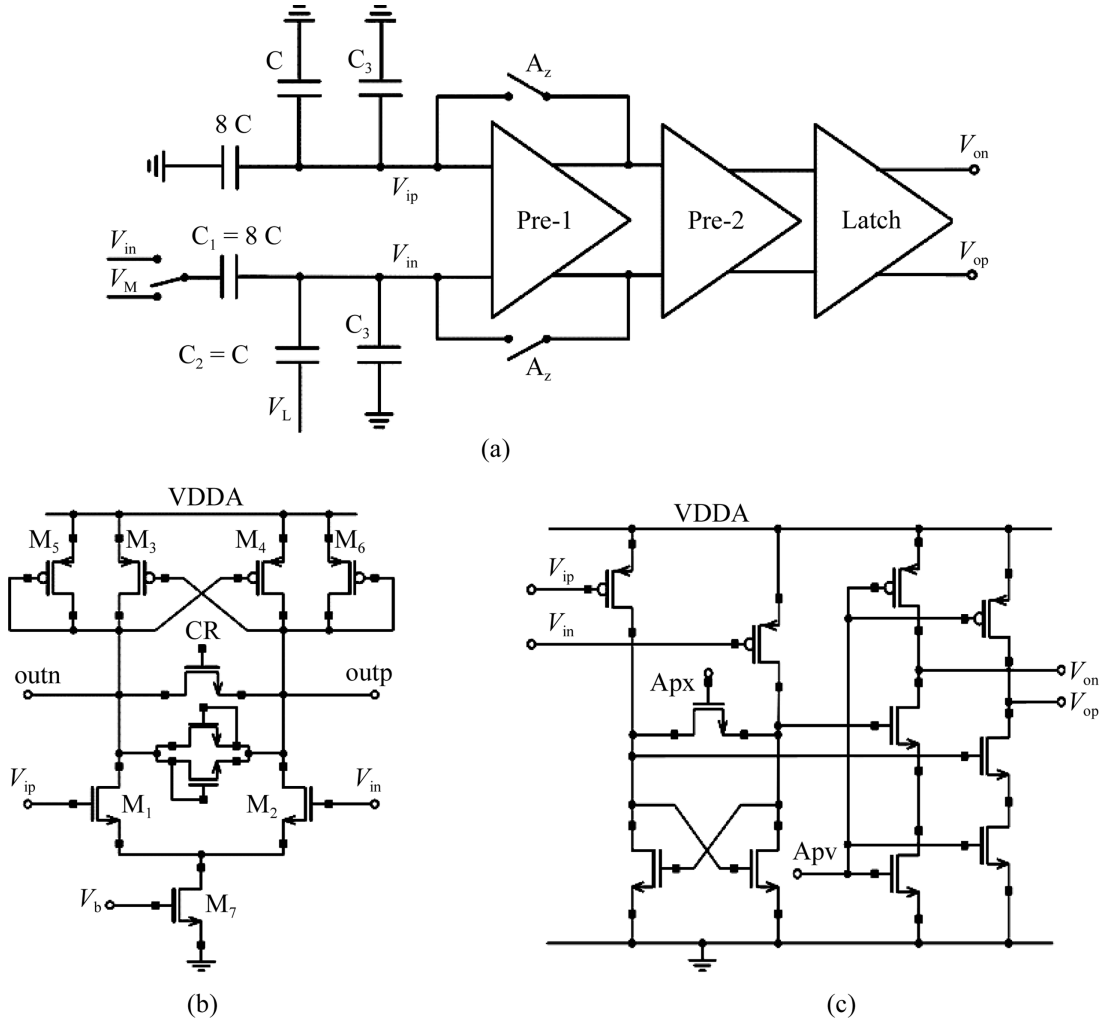

Fig. 6. (a) Comparator diagram with (b) preamplifier and (c) latch.

pacitive divider to adjust the input signals to guarantee proper comparator operation. By the end of the sampling mode, with A_z turned off, the information of the input signal has been held at the positive port as a charge form. In the comparison mode, based on the comparator output, the output of the D/A converter is controlled by the digital logic to approximate the sampled input successively.

The preamplifier is shown in Fig. 6(b). The cross-coupled positive feedback can effectively increase the gain, which can be shown as below:

$$A_{\text{pre}} = \frac{g_{\text{m1,2}}}{g_{\text{m5,6}}} \times \frac{1}{1 - g_{\text{m3,4}}/g_{\text{m5,6}}}. \tag{4}$$

Here, the second fraction represents the gain resulting from positive feedback. With different transistor sizes, the Pre-1 and Pre-2 have the same architecture. Two MOSFETs are connected as clamped transistors between the outputs of the preamplifier to improve the recovery speed of the comparator outputs. Shown in Fig. 6(c) is a latch which is applied to boost up the output of the second preamplifier to a desired output level.

Attention must be paid that the bias current of M_7 is a critical design variable for the comparator. The noise, speed and power consumption of the preamplifier are all related to the current. It is important to find an optimal compromise between a small bias current for low power dissipation and a large value to minimize noise and maximize the comparison rate. Comparator offset voltage adds directly to the total ADC offset[12]. In this design the offset mainly comes from the voltage threshold mismatch of the input devices in all these three stages and the mismatch of the two capacitor arrays connected to the comparator's negative and positive ports. Offset cancellation techniques were avoided to maintain low power dissipation and correspondingly higher speed, particularly because high matching performance has been realized with very careful layout routing.

3.4. Logic circuit design

The control logic block is used to realize the binary search algorithm, store the intermediate results and generate control signals for the analog block. Figure 7 shows some control signals employed in the SAR A/D converter, where SOC represents the start signal of the conversion and EOC represents the end signal of the conversion.

After the sample-and-hold process is completed in the first clock pulse, ten periods are subsequently used to realize the SAR algorithm and generate the outputs. Eleven clock cycles are required to complete one A/D conversion. At the 11th clock cycle, EOC turns to a high level, and the 10-bit output is avail-

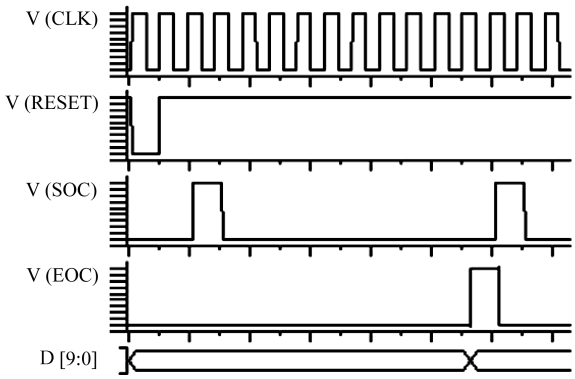

Fig. 7. Control signals in the SAR A/D converter.

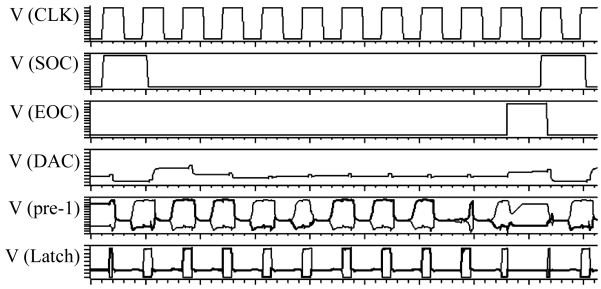

Fig. 8. Post-simulation result of the SAR A/D converter.

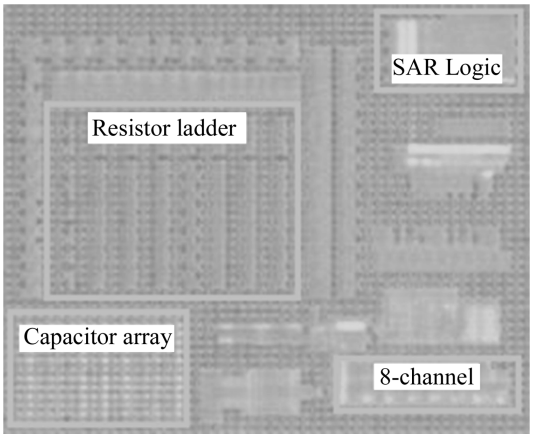

Fig. 9. Microphotograph of the proposed converter.

able. Before the converter begins to work, a RESET pulse is suggested to put before the first SOC pulse.

4. Design results and discussion

This R-C hybrid architecture SAR A/D converter is implemented in 90 nm CMOS logic process. Figure 8 is the post-simulation result. Based on the comparator output, the output of the D/A converter is controlled by the SAR logic circuit to approximate the value of the input signal. In each bit-cycle, eleven clock pulses are utilized where the first ten clock pulses are used for the ten bits' generation and the last single pulse is used for ending the conversion.

A microphotograph of the proposed SAR A/D converter is shown in Fig. 9 where it just occupies an area of 238 × 214 μm^2. This converter is realized in the MPW (multi project wafer) fabricated based on the 1P9M CMOS logic process. However, this converter just utilizes the poly layer and the first five metal layers, so the microphotograph is not very clear. Therefore, a layout photograph is shown in Fig. 10 as a comparison with Fig. 9. In this converter, as discussed in section 3.2, the 7-bit resistor ladder with intrinsic monotonicity and just 3-bit ratio accuracy is necessary for the capacitors to guarantee the monotonicity of the entire A/D converter. However, the matching performance of these passive components is still very significant because any mismatch between two resistors or two capacitors can result in nonlinearity. For the layout design, P+ diffusion resistors and finger-cap capacitors are used. Also, to

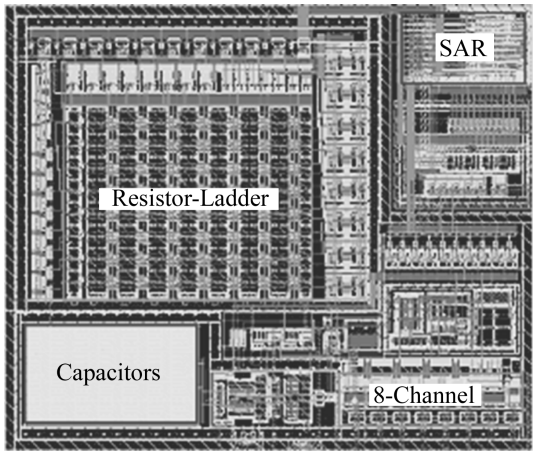

Fig. 10. Layout photograph of the proposed converter.

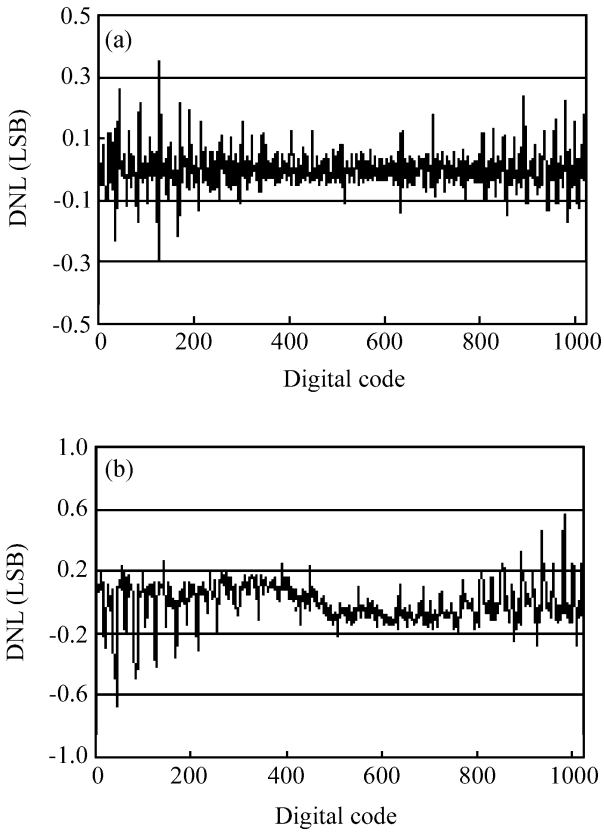

Fig. 11. Measured DC characteristics. (a) DNL. (b) INL.

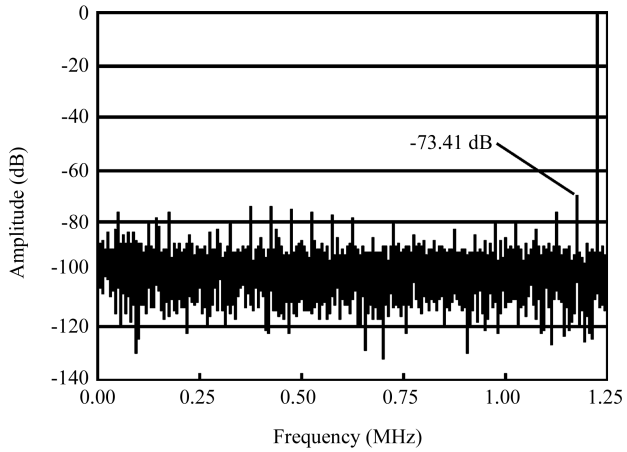

Fig. 12. 12000 points DFT @ 2.5 MS/s with 1.2 MHz Input.

Table 1. Performance summary of the A/D converter.

Parameter	Value
Technology	90 nm CMOS logic
Supply voltages	1.0 V, 3.3 V
Voltage reference	3.3 V
Input range	1.65 ± 1.634 V
Sampling rate	2.5 MS/s
ENOB (f_{in} = 1.2 MHz)	9.43 bits
SINAD (f_{in} = 1.2 MHz)	58.53 dB
SFDR (f_{in} = 1.2 MHz)	72.86 dB
THD (f_{in} = 1.2 MHz)	64.83 dB
DNL	0.36 LSB
INL	0.69 LSB
Power dissipation	6.62 mW
Active area	238×214 μm^2

Table 2. Comparison with some previous work.

References	Resolution (bits)	DNL (LSB)	INL (LSB)	Area (mm^2)	FOM (pJ/conversion step)
[3]	8	0.18	0.87	0.14	9.0
[4]	10	0.5	0.5	0.4	5.9
[5]	10	0.4	0.5	5.0	442
[6]	12	—	$< \pm 2$	—	< 14.6
Proposed	10	0.36	0.69	0.051	3.84

achieve a good performance, the resistor ladder is sided by dummies to maintain the same environment on both sides, and the capacitor pair is routed with a common-central symmetry method to reduce the gradient mismatch and random mismatch. Dummy capacitors are also placed on the perimeter of the capacitor array. Since not too many capacitors are used in the design, the wiring complexity caused by the common-central symmetry method is acceptable.

Figure 11 shows the static characteristics obtained from the measurement of the converter. The DNL and INL of this converter are measured with the histogram testing method[14]. After the massive sampled data are processed with the "Matlab" program, the DNL and INL plots are generated from "Microsoft Office Excel". With an input signal of about 301 kHz sampled at 2.5 MS/s, about 2 M data are sampled and processed. This data record size can provide a confidence level of more than 99%. The DNL and INL are measured to be 0.36 LSB and 0.69 LSB respectively. But as shown in Fig. 11, the DNL and INL are not very well at small and large digital codes. This is due to the fact that the comparator offset is not constant with different input amplitudes. At small and large digital codes, the comparator offset is worse than that around mid-scale. To overcome this shortcoming is the aim of some of our future work.

The AC characteristics are measured at 2.5 MS/s sampling rate. Figure 12 is a 12000 points DFT spectrum for a 1.2 MHz single-ended sine input signal sampled at 2.5 MS/s. During the AC performance measurement, the non-coherent sampling method is utilized. Also, before DFT, the windowing technique is used to avoid spectral leakage. The ENOB is 9.43 bits and the SFDR is measured to be 72.86 dB. The overall performance of the proposed A/D converter is summarized in Table 1.

To enable a comparison with previous work, the FOM (figure of merit)

$$\mathrm{FOM} = \frac{P_{\mathrm{diss}}}{2^{\mathrm{ENOB}} \times f_{\mathrm{sample}}}$$

is used. Here, P_{diss} is the power dissipation of the converter, and ENOB is measured at the sampling rate f_{sample}. For this proposed converter, the typical power dissipation is 6.62 mW including the output drivers and the ENOB is 9.43 bits measured with a 1.2 MHz single-ended sine wave sampled at 2.5 MS/s. Table 2 gives a comparison with some previous works[3−6]. From the comparison, it can be seen that this proposed converter features high performance.

5. Conclusion

Based on 90 nm CMOS logic process, by using an R-C hybrid architecture D/A converter, pseudo-differential comparison architecture and low power voltage level shifters, a 10-bit 2.5 MS/s SAR A/D converter is realized. With reasonable layout routing topology, good static characteristics are achieved. The DNL and INL are measured to be 0.36 LSB and 0.69 LSB, and the power dissipation is measured to be 6.62 mW including the output drivers. The total area of this converter is just about 0.051 mm^2. The measurement results show that this converter achieves high performance and is very suitable for multi-supply embedded SoC applications.

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