Short channel effect in deep submicron PDSOI nMOSFETs

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Abstract: Deep submicron partially depleted silicon on insulator (PDSOI) nMOSFETs were fabricated based on the 0.35 μm SOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). Mechanisms determining short-channel effects (SCE) in PDSOI nMOSFETs are clarified based on experimental results of threshold voltage dependence upon gate length. The effects of body bias, drain bias, temperature and body contact on the SCE have been investigated. The SCE in SOI devices is found to be dependent on body bias, drain bias and body contact. Floating body devices show a more severe reverse short channel effect (RSCE) than devices with body contact structure. Devices with low body bias and high drain bias show a more obvious SCE.

Key words: short channel effect; PDSOI; MOSFET
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1. Introduction

Reduced body effects, freedom from latch-up, and excellent soft-error immunity have made silicon-on-insulator (SOI) technologies very attractive for future high-speed operation of complementary metal–oxide–semiconductor field effect transistors (CMOSFETs)[1]. SOI MOSFETs also offer significant power reduction as compared with bulk MOSFETs due to the reduced parasitic capacitance. Meanwhile, with the continual scaling down of device feature size, the short channel effect (SCE) becomes more and more prominent[2]. SCE causes the dependence of device characteristics, such as threshold voltage, upon channel length. This leads to scatter of the device characteristics because of the scatter of the gate length produced during the fabrication process. Moreover, the SCE degrades the controllability of the gate voltage to drain current, which leads to degradation of the subthreshold slope and an increase in drain off-current[3]. It is therefore technologically important to study the characteristics of short-channel SOI MOSFETs.

Previously, there have been many studies about the SCE and reverse short channel effect (RSCE)[1−6]. The SCE and RSCE depend on the process greatly. The SCE and RSCE of a deep submicron PDSOI nMOSFET are investigated in this paper; we present the effect of body bias (V_{ps}), the drain bias (V_{ds}), temperature and body contact on the SCE by using measured data, and the detailed physics is explained.

2. Experiment

The PDSOI nMOSFETs were fabricated using the 0.35 μm SOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). They were fabricated on UNIBOND SOI wafers. The thickness of the buried oxide, the top silicon film and the gate oxide was 400, 175 and 13 nm. Local oxidation of silicon (LOCOS) was performed to fully consume the active silicon layer in the isolation region. Back channel implantation of B^+ ions was performed to avoid back channel leakage. Arsenic was implanted at an energy of 100 keV to form the source/drain. $TiSi_2$ was formed in the source/drain region. nMOSFETs with two different body contact structures, i.e. H-gate, body tied to source (BTS), and floating body nMOSFETS, were fabricated. Figure 1 shows the layout of the body contact nMOSFETs.

The threshold voltage used in this paper was measured at V_{ds} = 0.1 V (3.6 V) at the intercept point on the axis V_g of the I_d versus V_g curve extrapolated from the point of maximum slope by a model builder program (MBP).

3. Results and discussion

Because we mostly use H-gate devices in our design, we mainly investigated the SCE of H gate nMOSFETs. Three dies were measured, and they all present the same phenomena as follows. The data of the die that presents the most obvious phenomena are chosen to demonstrate the phenomena most clearly.

Figure 2 shows the measured threshold voltage as a function of channel length for the H-gate SOI nMOSFETs. The width of the devices is 20 μm, and the body contacts are connected to ground. The results show an obvious RSCE. There are two main reasons for the RSCE. Firstly, Frenkel pairs (interstitial-vacancy) are induced by ion implantation in the source/drain region, and then laterally diffuse into the chan-

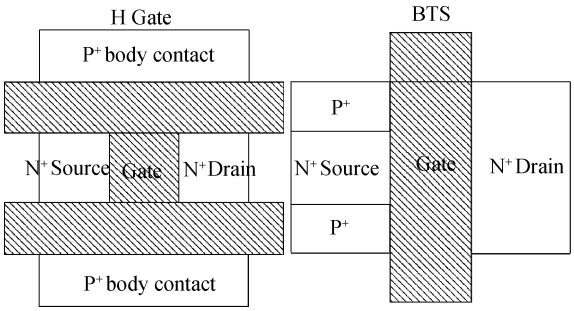

Fig. 1. Layout of H-gate and BTS nMOSFETs.

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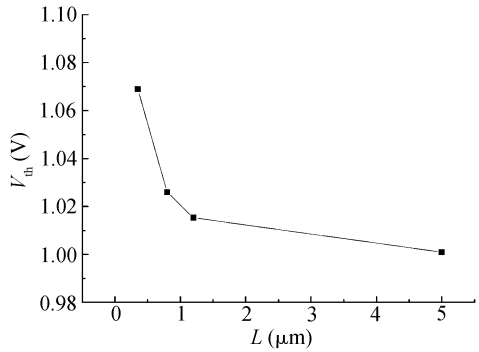

Fig. 2. Threshold voltage versus channel length for an SOI nMOSFET.

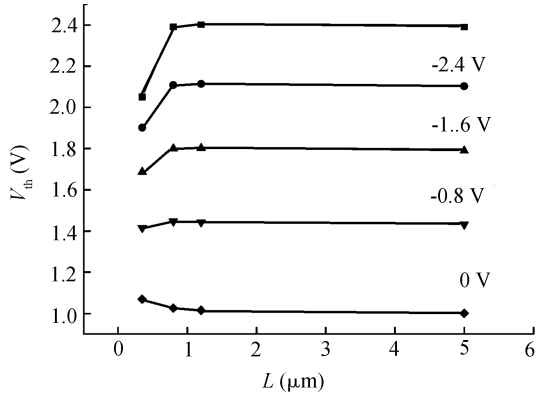

Fig. 3. Threshold voltage versus channel length for SOI nMOSFETs with different V_{ps}.

nel region during annealing. This will enhance the diffusion of the channel dopant and cause an increase in the surface concentration of the channel dopant, especially at the source/drain edge; the surface concentration at the channel center becomes larger in proportion as the gate length is reduced. This phenomenon causes reverse short-channel effects on the threshold voltage. Secondly, the injection of vacancies and lattice strain during $TiSi_2$ formation in the source/drain region cause defect-enhanced boron diffusion which also results in threshold increase in short channel devices[6].

Figure 3 shows the measured threshold voltage as a function of channel length for the H-gate SOI nMOSFETs at different V_{ps}. The width of the devices is 20 μm. As the body bias becomes more negative, the SCE appears instead of the RSCE, and the SCE becomes more severe. The reason for this is that the charge sharing effect is enhanced when the body bias becomes more negative, and we can explain this phenomenon from Fig. 4. Q, Q_1 and Q_2 are the charge in the depletion region controlled by the gate, source and drain separately. Due to the body effect, the depth of the depletion region will increase with decreasing V_{ps}, and then $(Q_1 + Q_2)/Q$ will increase with decreasing V_{ps}. This will lead to a more severe SCE. This phenomenon can also be explained as follows.

The threshold voltage reduction due to the short channel effect can be modeled as

$$\Delta V_{th} = \theta_{th}(L)[2(V_{bi} - \phi_s) + V_{ds}], \tag{1}$$

where V_{bi} is the built-in voltage of the PN junction between the source and the body, and ϕ_s is twice as large as the Fermi potential (ϕ_B). The expression $\theta_{th}(L)$ is a short channel effect coefficient, which has a strong dependence on the channel length and is given by

$$\theta_{th}(L) = [\exp(-L/2l_t) + 2\exp(-L/l_t)], \tag{2}$$

$$l_t = \sqrt{\frac{\varepsilon_{si} T_{ox} X_{dep}}{\varepsilon_{ox}\eta}}, \tag{3}$$

where X_{dep} is the depth of the depletion region, and X_{dep}/η represents the average depletion depth along the channel. X_{dep} is given by

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}\phi_s - V_{bs}}{qN_{ch}}}. \tag{4}$$

As the body bias becomes more negative, the depletion width will increase. Hence ΔV_{th} will increase, and then lead to a more severe SCE.

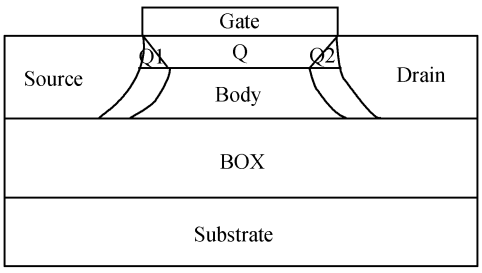

Fig. 4. Charge sharing model.

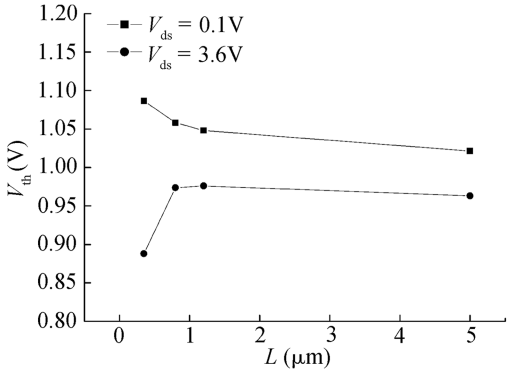

Fig. 5. Threshold voltage versus channel length for SOI nMOSFETs with different V_{ds}.

Figure 5 shows the measured threshold voltage as a function of channel length for the H-gate SOI nMOSFETs at different V_{ds}. The width of the devices is 5 μm, and the body contacts are connected to ground. Instead of the RSCE, the SCE appears when $V_{ds} = 3.6$ V. The reason for this is also that the charge sharing effect is enhanced when the drain bias increases. When the depletion region near the drain expands further[8], Q_2 will be larger, and $(Q_1 + Q_2)/Q$ will increase. This will lead to a more severe SCE.

This phenomenon can also be explained by Eq. (1). ΔV_{th} will increase with the increase of V_{ds}, and then lead to a more severe SCE.

Figure 6 shows the measured threshold voltage as a function of channel length at different temperatures for the H-gate

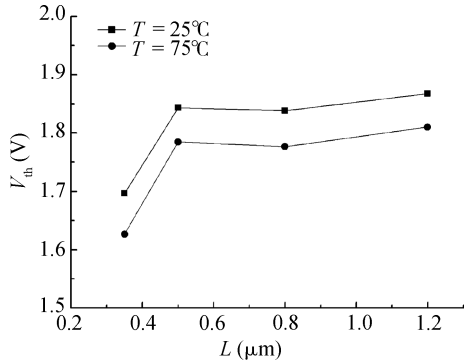

Fig. 6. Threshold voltage versus channel length at different temperatures.

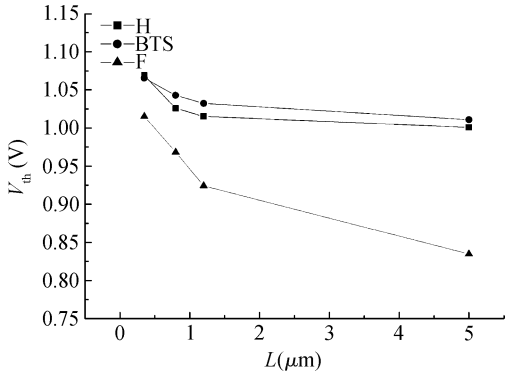

Fig. 7. Threshold voltage versus channel length for body contact and floating body SOI nMOSFETs.

SOI nMOSFETs. The width of the devices is 10 μm, and the $V_{ps} = -1.6$ V. The relation between threshold voltage and temperature is shown in Eq. (5). Because $E_g(T=0)/2q$ is greater than the Fermi potential, the Fermi potential decreases as the temperature increases, and the threshold voltage decreases as the temperature increases.

$$\frac{\mathrm{d}V_T}{\mathrm{d}T} = \frac{\mathrm{d}\phi_B}{\mathrm{d}T}\left(2 + \frac{1}{C_i}\sqrt{\frac{\varepsilon_i q N_A}{\phi_B}}\right), \tag{5}$$

where

$$\frac{\mathrm{d}\phi_B}{\mathrm{d}T} = -\frac{1}{T}\left[\frac{E_g(T=0)}{2q} - |\phi_B(T)|\right], \quad T > 0, \tag{6}$$

$$\frac{\mathrm{d}\phi_B}{\mathrm{d}T} = +\frac{1}{T}\left[\frac{E_g(T=0)}{2q} - |\phi_B(T)|\right], \quad T < 0. \tag{7}$$

Since the ratio of the charge controlled by the source and drain to the charge controlled by the gate cannot be affected by temperature, the extent of the SCE stays nearly the same at different temperatures.

Figure 7 shows the measured threshold voltage as a function of channel length for the H-gate, BTS and floating body SOI nMOSFETs. The width of the devices is 20 μm, and the body contacts of the H-gate and BTS SOI nMOSFETs are connected to ground. Due to the kink effect, the threshold voltages of the floating body devices are lower than those of the body contact devices. The RSCE of the floating body structure is more severe than the body contact structures. The reason for this is that due to the floating body effect, the body potential of the floating body structure is higher than that of the body contact structures. We can easily see that the devices with lower body potential have a more severe SCE from Fig. 3. Moreover, since the floating body devices with long channel lengths show a more severe floating body effect than short ones, the decrease in the threshold voltage for long devices is larger than short ones[9]. All of these factors make the floating body devices show a more severe RSCE.

4. Conclusion

In this paper, we have investigated the effects of V_{ps}, V_{ds}, temperature and body contact on the SCE of deep submicron PDSOI nMOSFETs. The floating body devices show a more severe RSCE than the devices with body contact structure, and the devices with low V_{ps} and high V_{ds} show a more obvious SCE. This work provides great help in the extraction of model parameters.

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