A 4224 MHz low jitter phase-locked loop in 0.13-μm CMOS technology*

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Abstract: A 4224 MHz phase-locked loop (PLL) is implemented in 0.13 μm CMOS technology. A dynamic phase frequency detector is employed to shorten the delay reset time so as to minimize the noise introduced by the charge pump. Dynamic mismatch of charge pump is considered. By balancing the switch signals of the charge pump, a good dynamic matching characteristic is achieved. A high-speed digital frequency divider with balanced input load is also designed to improve in-band phase noise performance. The 4224 MHz PLL achieves phase noises of –94 dBc/Hz and –114.4 dBc/Hz at frequency offsets of 10 kHz and 1 MHz, respectively. The integrated RMS jitter of the PLL is 0.57 ps (100 Hz to 100 MHz) and the PLL has a reference spur of –63 dB with the second order passive low pass filter.

Key words: PLL; in-band noise; dynamic mismatch; RMS jitter
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1. Introduction

Integrated phase-locked loops (PLLs) play an important role in the applications of clock generation and frequency synthesis. A PLL can generate a high-speed internal clock from a low frequency external reference clock while meeting tight jitter requirements. Low jitter PLLs have aroused significant interest as the operating speed of digital circuits increases, particularly for high frequency clock generators aimed at high-speed and high-resolution digital circuits[1, 2].

In some papers, a high frequency input reference is employed to allow the use of very high PLL bandwidths, achieving minimum jitter for low-noise input clock sources[2, 3]. In this work we mainly focus on in-band noise optimization. To maintain low in-band noise, high-speed digital blocks are employed and charge pump noise current injection is reduced. Dynamic matching of charge pump is another issue we consider. Unlike conventional matching techniques, by simply reducing the turn on time of the charge pump when the PLL is locked, dc mismatch caused by short channel effects is alleviated. By dynamic matching of the charge pump, the sideband of the PLL can be kept at a relatively low level.

In this paper a low jitter and low spur PLL aimed at a subsampling impulse radio ultra wideband (IR UWB) receiver[4] is presented. The PLL generates a 4224 MHz clock for the high-speed sampler employed in the receiver. A block diagram of the phase locked loop is shown in Fig. 1. A 33 MHz TCXO is used as an external reference clock. This paper also discusses design considerations and describes the implementation of major circuit blocks.

2. Design considerations

2.1. In-band noise optimization

In an integer-N PLL clock generator architecture (see Fig. 1), the output jitter is caused by both the VCO phase noise and the noise of the other PLL components. The out-of-band phase noise of the PLL is dominated by the VCO while the in-band phase noise is mainly contributed by the other components such as charge pump and dividers. In-band noise generally results in at least 50% of the total jitter[3]. Low in-band phase noise is therefore an important issue. The sources of the in-band noise are jitter in the digital logic, mismatch and noise of the charge pump, reference noise, and attenuated VCO noise[5]. To reduce the overall in-band noise, the noise of each block must be kept low.

The phase frequency detector (PFD) and charge pump (CP) contribute the majority of the in-band noise. The PFD/CP combination exhibits non-ideality: a dead zone. To eliminate the dead zone, the two PFD outputs produce narrow pulses at every phase comparison instant even if the input phase difference is zero. The delay reset pulses avoid phase noise degeneration caused by the dead zone, but introduce significant current noise at the same time. The longer the delay reset time is, the more noise current injects into the loop.

The noise current model of the charge pump is shown in Fig. 2, where $i_{n,\,total}$, $i_{n,\,up}$ and $i_{n,\,dn}$ represent the total output noise current, the charge and discharge noise current, respec-

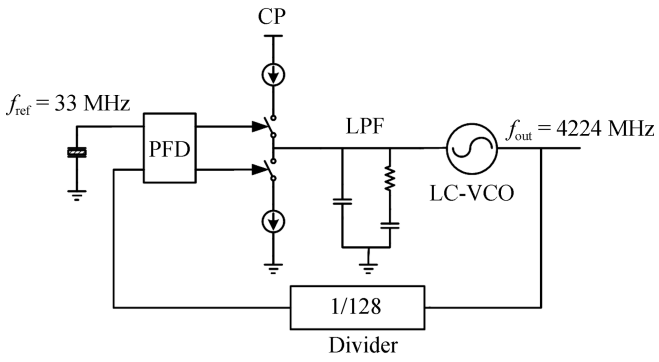

Fig. 1. Block diagram of PLL.

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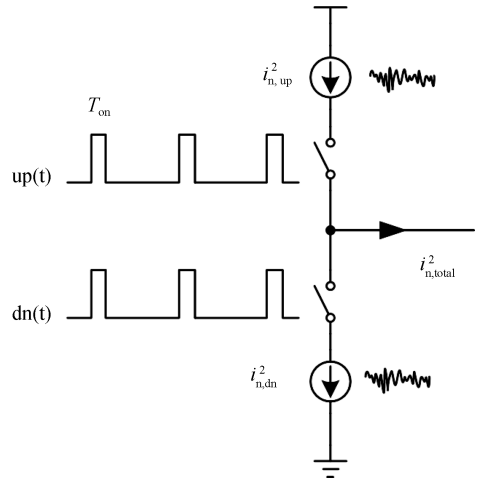

Fig. 2. Output noise sampling model of charge pump.

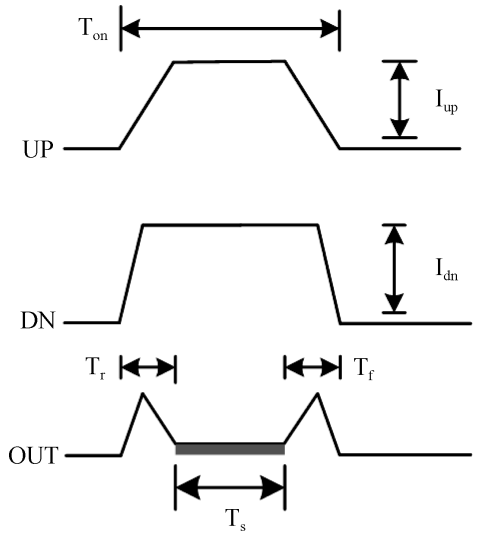

Fig. 3. Non-ideal charge and discharge current.

tively. Up(t) and dn(t) are the switch signals. T_{on} is the width of the delay reset pulse. The output noise current equals the sum of charge and discharge current noise sampled by the delay reset pulse every reference cycle.

$$i_{n,\,total}(t) = i_{n\,,up} \times up(t) + i_{n,\,dn} \times dn(t). \tag{1}$$

The total output noise spectral density $S_{n,\,total}(f)$ is:

$$\begin{aligned} S_{n,\,total}(f) &= S_{i_{n,\,up}}(f) * S_{up}(f) + S_{i_{n,\,dn}}(f) * S_{dn}(f) \\ &= \int_{-\infty}^{+\infty} S_{i_{n,\,up}}(x)\, S_{up}(f-x)\mathrm{d}x \\ &\quad + \int_{-\infty}^{+\infty} S_{i_{n,\,dn}}(x)\, S_{dn}(f-x)\mathrm{d}x. \end{aligned} \tag{2}$$

$S_{n,\,up}$ and $S_{n,\,dn}$ are the spectral density of $i_{n,\,up}$ and $i_{n,\,dn}$, * is a convolution operator, $S_{up}(f)$ and $S_{dn}(f)$ denote the spectral density of up(t) and dn(t).

$$S_{up}(f) = S_{dn}(f) = \sum_{n=-\infty}^{+\infty} c_n^2 \delta\,(f - nf_{ref}.) \tag{3}$$

Here, n is the harmonic number, and c_n is the Fourier coefficient:

$$c_n = \frac{\sin\,(n\pi T_{on} f_{ref})}{n\pi} \approx T_{on} f_{ref} = \frac{T_{on}}{T}. \tag{4}$$

Then Equation (2) can be rewritten as:

$$\begin{aligned} S_{n,\,total}(f) &= c_0^2 \left(S_{i_{n,\,up}}(f) + S_{i_{n,\,dn}}(f)\right) \\ &\quad + 2\sum_{n=1}^{\infty} \left|c_n^2\right| \left(S_{i_{n,\,up}}(f - nf_{ref}) + S_{i_{n,\,up}}(f - nf_{ref})\right). \end{aligned} \tag{5}$$

From Eqs. (4) and (5) we can conclude that reducing the width of the delay reset pulse will decrease c_n proportionally and thus achieve lower output noise spectral density. In order to minimize the noise contributed by PFD & CP, the delay reset pulse should be made as short as possible.

The divider is another issue that should be taken care of when optimizing the in-band noise. According to Ref. [6], the noise current pulses applied at the zero crossing have the maximum effect on the exceed phase and the minimum effect on the amplitude. On the other hand if the impulses are applied at the peak of the voltage across the capacitor, there will be no phase shift and only an amplitude change will result. So we should make our divider fast enough to suppress possible noise injection at the zero crossing.

2.2. Dynamic mismatch of CP

Ideally, the charge and discharge currents are exactly the same. Therefore zero static phase error can be obtained in the locked state. In fact, due to non-ideal effects such as device mismatch and channel length modulation, mismatch exists. Mismatch of charge pumps can not only result in unwanted spurs but also deteriorates the spectral performance.

Mismatch of a CP can be categorized into two types: steady mismatch and dynamic mismatch. Steady mismatch is mainly due to dc current mismatch between charge and discharge currents while dynamic mismatch is caused by different dynamic responses of PMOS and NMOS transistors. Several methods have been presented to reduce the CP mismatch in the steady state[7, 8]. In Ref. [7] an error amplifier and reference current sources are used to achieve perfect current match characteristics. In Ref. [8] a digital calibration technique is employed to compensate for the mismatch of the up and down current. However, in these papers, mismatch optimization mainly concentrates on steady matching and both techniques improved the charge pump performance at the cost of either circuit complexity or extra power and noise.

Figure 3 illustrates the mismatch of the charge pump when all signals are no longer considered ideal. T_{on}, T_s, T_r, T_f are the turn on time, static current duration, current rise time and fall time, respectively. Current mismatch is composed of two parts: steady mismatch and dynamic mismatch. ΔQ_s and ΔQ_t are extra charges produced by steady mismatch and dynamic mismatch, respectively.

$$\Delta Q_s = (I_{dn} - I_{up})T_s, \tag{6}$$

$$\Delta Q_{\rm t} = \int_0^{T_{\rm r}} \left(I_{\rm r,\,dn}(t) - I_{\rm r,\,up}(t)\right) {\rm d}t + \int_0^{T_{\rm f}} \left(I_{\rm f,\,dn}(t) - I_{\rm f,\,up}(t)\right) {\rm d}t. \quad (7)$$

Extra charge provided by the charge pump every period causes phase offset in PLL and the amount of phase offset is given by

$$|\varphi_\varepsilon| = 2\pi f_{\rm ref}\frac{\Delta Q}{I_{\rm s}} = 2\pi f_{\rm ref}\left(\frac{\Delta Q_{\rm t}}{I_{\rm s}} + \frac{\Delta Q_{\rm s}}{I_{\rm s}}\right). \quad (8)$$

Phase offset generates a spur at the output of the PLL and the amount of the reference spur, $P_{\rm r}$ in the third-order PLL is approximately given by[8]

$$P_{\rm r} = 20\lg\left(\frac{\sqrt{2}\dfrac{I_{\rm cp}R}{2\pi}\varphi_\varepsilon K_{\rm VCO}}{2f_{\rm ref}}\right) - 20\lg\frac{f_{\rm ref}}{f_{\rm P1}}{\rm dBc}, \quad (9)$$

where R, $K_{\rm VCO}$, $f_{\rm ref}$ and $f_{\rm P1}$ are the resistor value in the loop filter, the VCO gain, the reference frequency for the PFD and the frequency of the pole in the loop filter, respectively.

According to Eq. (8), smaller φ_ε can achieve better spur performance. To reduce φ_ε, the amount of mismatch charge injected into the loop per cycle should be minimized. Equations (6) and (7) show that $\Delta Q_{\rm s}$ is proportional to the turn on time while $\Delta Q_{\rm t}$ is only related to the dynamic response of the control signals $I_{\rm r}$(t) and $I_{\rm f}$(t). Shortening the turn on time can not only reduce noise injection but also solve the steady mismatch problem. To minimize $\Delta Q_{\rm t}$ we should balance the up and down control signals perfectly.

3. Circuit description

3.1. Phase frequency detector (PFD)

The PFD is built with a state machine with DFFs. A dynamic logic style PFD is employed in this design[9]. The circuit of PFD is shown in Fig. 4. Conventional static logic circuitry is replaced by dynamic logic gates. Compared with static logic, the dynamic type PFD has a much shorter critical path. The reduced feedback path delay allows a shorter delay reset time to reduce the noise introduced by PFD/CP when PLL is locked.

3.2. Charge pump (CP)

Figure 5 shows the schematic of the charge pump. For the purpose of keeping non-ideal switching errors from reaching the output node, switches are placed on the source side of the current source devices, M5 and M6. MCP and MCN are added to reduce the charge coupling to the gate and help to enhance the switching speed[10]. M2 and M3 can eliminate the charge sharing effects and also improve the speed of charge pump[11].

As discussed in Section 2, in order to optimize in-band noise and reduce steady mismatch, the delay reset time is minimized to several hundreds of pico-seconds, so that the dynamic mismatch becomes the main issue in this design.

Dynamic matching requires the charge and discharge currents to have the same rising and falling edges which are properly aligned. The phase aligning problem can be solved by incorporating buffers between PFD and CP to make the UP and

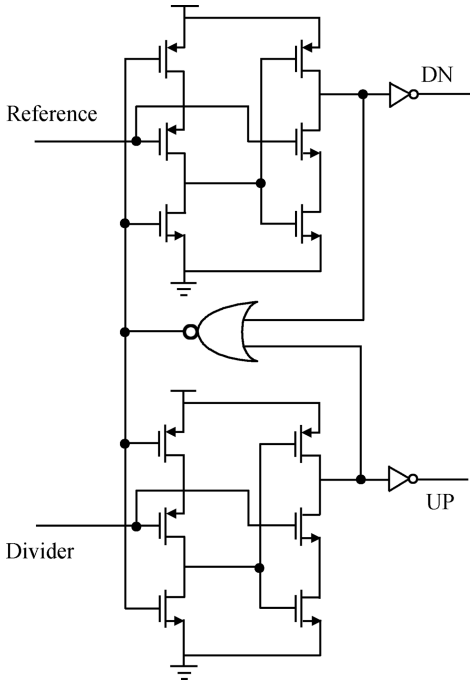

Fig. 4. Schematic of phase frequency detector.

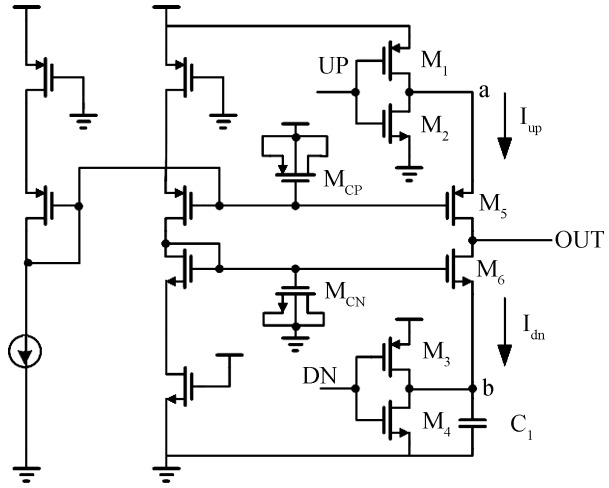

Fig. 5. Schematic of charge pump.

DN signal be in the same phase. The dynamic behavior of the current flow to the output is controlled by the source voltage of the current source transistors, which is $V_{\rm a}$ at node a and $V_{\rm b}$ at node b. The scales of M1, M2, M3 and M4 are carefully chosen to balance the drive strength of the inverter buffer to guarantee that the edges of $V_{\rm a}$ and $V_{\rm b}$ are matched. Since NMOS transistors have fewer parasitic capacitances, C_1 is placed at node b to make the load of M3 and M4 equal to the load of M1 and M2, further matching the dynamic charge and discharge current.

3.3. Frequency divider

A high-speed divide-by-two circuit (DTC) with balanced input load (BIL) is shown in Fig. 6. The loads of D and DB are balanced, since they are both equal to the sum of the gate capacitances of M1a, M4a, M9a and M10a. M5a and M6a are cross-coupled, which form the regeneration part, closing the positive feedback loop with the main amplifier constituted by

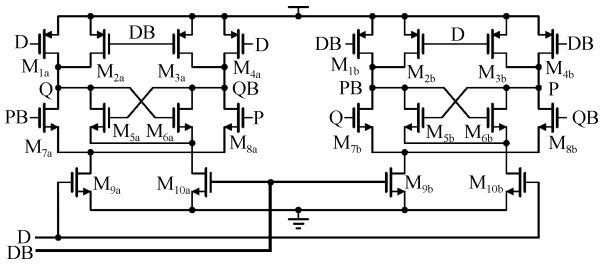

Fig. 6. BIL-DTC.

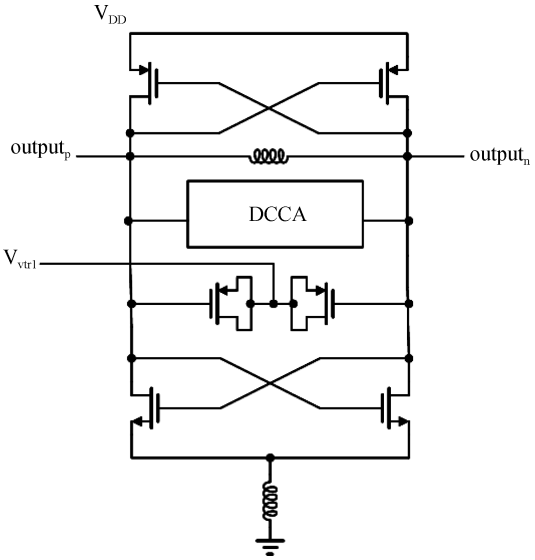

Fig. 7. Schematic of LC-VCO.

M1a, M4a, M7a–M10a. The tail transistor M10 is used to reduce the signal swing at the internal nodes Q1, Q1_bar, Q2 and Q2_bar, thus speeding up the change of the states[12]. A large M10 size, as designed in Ref. [11], only increases the clock load which is undesired. In our design, M10 is only 37% as large as M9, and the input clock loads are balanced. However, a small M10 aspect ratio speeds up the change of states, which reduces both the swing at the internal nodes and the parasitic capacitances at those nodes.

3.4. Voltage-controlled oscillator (VCO)

The VCO adopts a complementary cross-coupled pair topology for current reuse. Current tail is not used in order to eliminate the noise from the MOSFETs of the current mirror. A digital controlled capacitor array (DCCA) is employed to compensate process variation while maintaining a low VCO frequency tuning gain $K_{\rm vco}$. A small $K_{\rm vco}$ is beneficial in achieving low phase noise and spurs. Inversion mode PMOS varactors are used. A filtering technique is used to lower the phase noise of the LC VCO[13]. The passive filter is composed of an inductor and the parasitic capacitor of the NMOS. The circuit of the VCO is shown in Fig. 7.

4. Experiment results

The proposed 4224 MHz Integer-N PLL is fabricated in the 0.13-μm CMOS process. The chip core occupies an area of 0.9 $\times$ 0.9 mm^2 excluding pads. The reference input is 33 MHz.

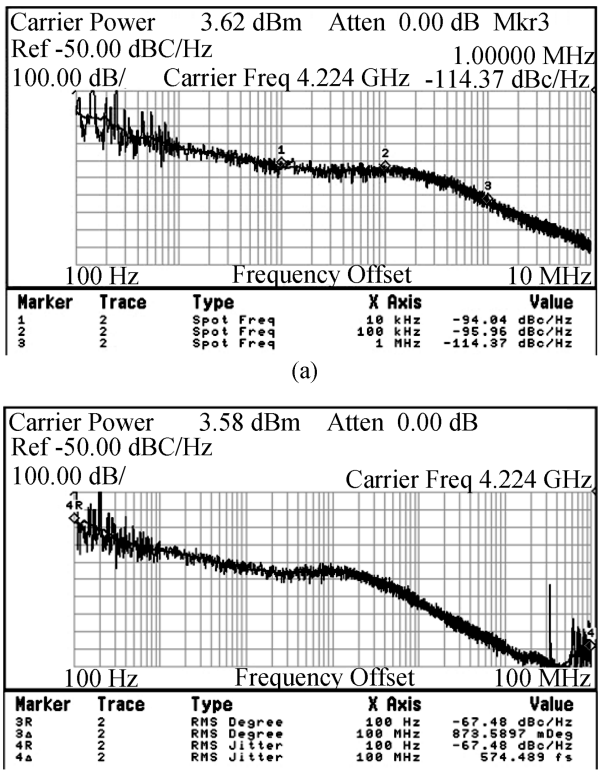

Fig. 8. (a) Measured PLL spot phase noise. (b) PLL integrated phase noise.

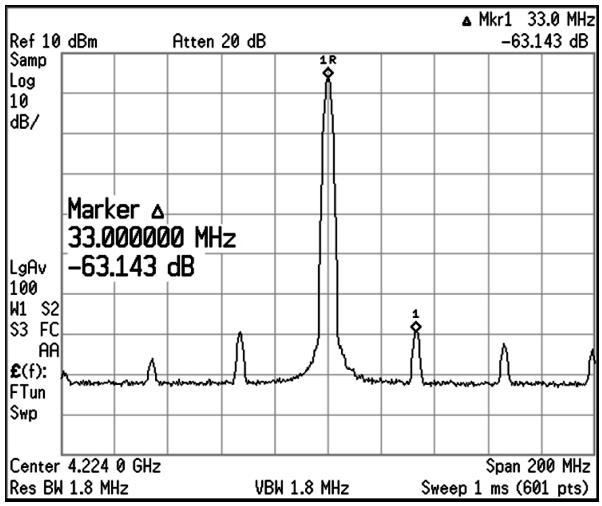

Fig. 9. PLL output spectra.

The output range of the wideband VCO is 3.74 to 5.16 GHz. Test results show that the proposed PLL exhibits good noise performance. The spot phase noise is shown in Fig. 8(a) when it is locked at 4224 MHz. The spot phase noise is –94 dBc/Hz at 10 kHz offset and –114.4 dBc/Hz at 1 MHz offset. The good in-band noise performance proves that the noise contributed by the charge pump and the frequency divider is well suppressed. Figure 8(b) shows that the RMS jitter integrated from 100 Hz to 100 MHz is 0.57 ps. The spectral performance is shown in Fig. 9. One can see that the spur level is is −63 dB. The chip consumes currents of 15 mA.

Table 1. Performance summary and comparison.

Parameter	Ref. [2]	Ref. [3]	This work
Process	0.12-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Supply voltage (V)	1.5	1.8	1.2
Chip core area (mm^2)	0.7	0.71	0.81
Reference frequency (MHz)	311	2488	33
VCO output range (GHz)	N/A	N/A	3.74–5.16
Output frequency (GHz)	3.11	9.953	4.224
Bandwidth (kHz)	1000–15000 programmable	N/A	300
Phase noise (dBc/Hz)	–104 @ 10 kHz–114.5 @ 1 MHz	–83 @ 10 kHz–107 @ 1 MHz	–94 @ 10 kHz–114.4 @ 1MHz
RMS jitter (ps) (100 Hz–100 MHz)	0.86	0.22 (10 kHz – 80 MHz)	0.57
Reference spur (dB)	N/A	N/A	−63
Power consumption (mW)	35	81	18

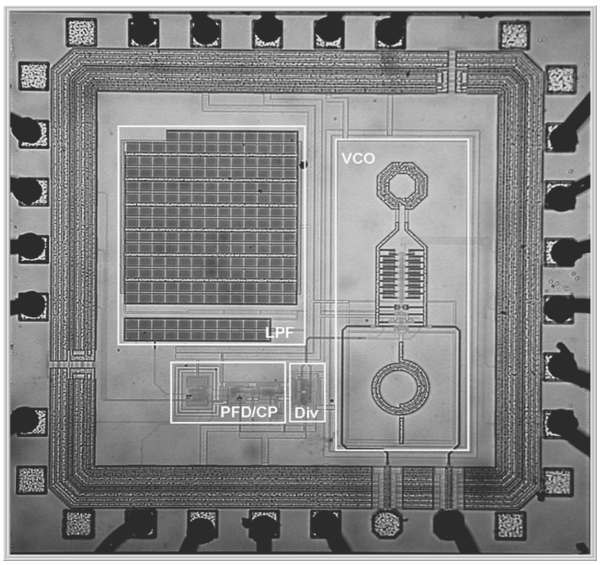

Fig. 10. Chip photo.

The die photograph is shown in Fig. 10. The measured results are summarized in Table 1 and a performance comparison is given too.

5. Conclusion

This paper presents a low jitter low spur PLL for high-speed clock generation. Jitter performance is optimized by employing a high-speed PFD and FD, and reducing the delay reset time of the charge pump. Steady mismatch and dynamic mismatch are analyzed. The measured jitter performance of the fabricated PLL proves that the noise optimization strategies are effective. After a further discussion of the mismatch characteristic of charge pumps, by simply reducing the turn on time of the PFD/CP to reduce dc current mismatch and balance the load of the UP and DOWN signals to improve the dynamic matching characteristic, the spur level of the PLL is kept at a relatively low level without any extra complicated matching techniques.

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