Full on-chip and area-efficient CMOS LDO with zero to maximum load stability using adaptive frequency compensation*

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Abstract: A full on-chip and area-efficient low-dropout linear regulator (LDO) is presented. By using the proposed adaptive frequency compensation (AFC) technique, full on-chip integration is achieved without compromising the LDO's stability in the full output current range. Meanwhile, the use of a compact pass transistor (the compact pass transistor serves as the gain fast roll-off output stage in the AFC technique) has enabled the LDO to be very area-efficient. The proposed LDO is implemented in standard 0.35 μm CMOS technology and occupies an active area as small as 220 × 320 μm^2, which is a reduction to 58% compared to state-of-the-art designs using technologies with the same feature size. Measurement results show that the LDO can deliver 0–60 mA output current with 54 μA quiescent current consumption and the regulated output voltage is 1.8 V with an input voltage range from 2 to 3.3 V.

Key words: low-dropout regulator; frequency compensation; full on-chip; system-on-chip
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1. Introduction

The low-dropout linear regulator (LDO) is a versatile power converter adopted in battery-powered mobile systems to provide a low-noise and stable supply voltage to subsequent circuits. In order to reduce the power-line cross-talk between different circuit blocks, it is preferable to have a separate LDO to power-up each sub-block of a system. For example, in Ref. [1] which introduced a highly integrated power-management IC, up to 18 LDOs are used in the entire chip. In this case, the size of a single LDO should be compact to prevent an excessively large chip area.

Conventional LDO structures often require a bulky off-chip capacitor at the output of each LDO to form the dominant pole[2−5]. When multiple LDOs are used on a single chip, elimination of these off-chip capacitor could be a huge advantage since the number of external pins and also on-board elements can be reduced significantly. Considering this, there has been a trend to integrate the LDO fully on-chip[6]. Three-stage amplifier based pole-splitting structures[6, 7] and a transient-improved structure[8] have already been proposed with good results. However, problems still remain in these designs. In Refs. [6, 7], the Q of the non-dominant complex poles in the LDO loop is inversely proportional to the output current. So a minimum output current requirement exists for the Q not to become too high to make the LDO unstable. In Ref. [8], since a single-stage error amplifier is used for stability considerations, cascode structures are used in the error amplifier to make the LDO have a higher loop gain. This will restrict its application in low-voltage conditions.

Based on the above analysis, it is desirable to have an area-efficient and full on-chip LDO developed for highly integrated power-management applications. Preferably, this LDO should also be stable in the full output current range and low-voltage compatible. In this paper we will present an LDO structure that meets the above requirements. By using both active compensation and gain fast roll-off at the output stage of the LDO, the Q of the non-dominant complex poles adaptively changes from first increasing to subsequently decreasing with increasing the load current. This enabled the full on-chip LDO to be stable from zero to maximum load. Meanwhile, low-voltage compatibility is not compromised because of the adopted two-stage error amplifier. Moreover, the use of a compact pass transistor (PT), which serves as the gain fast roll-off output stage, makes the LDO area-efficient.

2. Proposed LDO circuit

The LDO with AFC is shown in Fig. 1(a) while Figures 1(b) and 1(c) show detailed transistor-level implementation of the capacitive-coupled feedback (CCFB) stage and the two-stage error amplifier. The CCFB stage is an active Miller compensation approach with similar principles to those in Refs. [9, 10] but much larger feedback transconductance g_{mf} is available in the adopted topology. The small-signal equivalent input impedance R_a and feedback transconductance g_{mf} are expressed as:

$$R_a = 1/\left(g_{m,n1} + g_{m,p1}\right), \tag{1}$$

$$g_{mf} = \left(g_{m,n1} + g_{m,p1}\right) R_f \left(g_{m,n2} + g_{m,p2}\right), \tag{2}$$

where $g_{m,n1(2)}$ and $g_{m,p1(2)}$ represents the transconductance of Mn1(2) and Mp1(2) shown in Fig. 1(b), respectively.

When I_L is low, C_m and the CCFB stage can perform the active Miller compensation[10, 11]. By using this active approach, the NDCPs will have Q reducing with decreasing I_L (proved later from Eq. (3) to Eq. (10)), resulting in a stable feedback loop even with zero I_L as shown in Fig. 2(a). However, the effect of the active approach will be twofold. The sole use of active compensation will result in the increase of Q and

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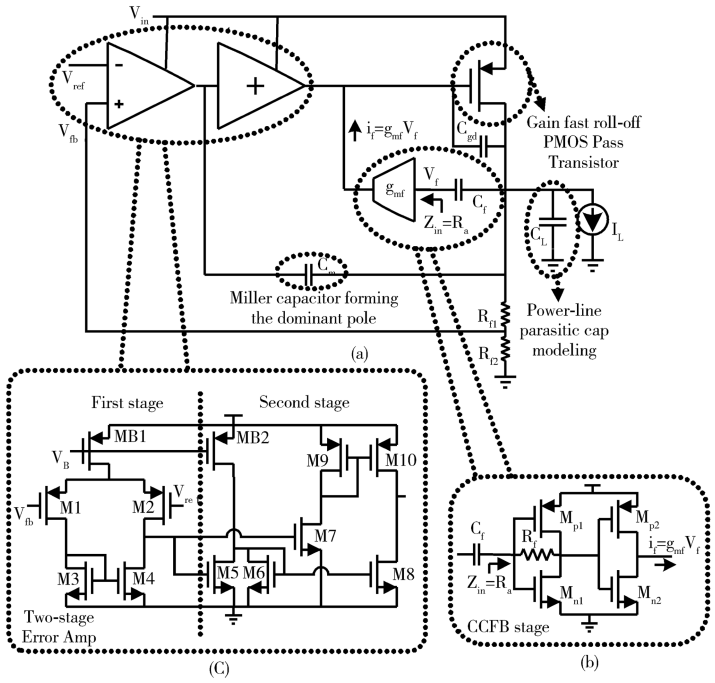

Fig. 1. Proposed LDO structure. (a) Conceptual structure. (b) Transistor-level implementation of the CCFB stage. (c) Transistor-level implementation of the two-stage error amplifier.

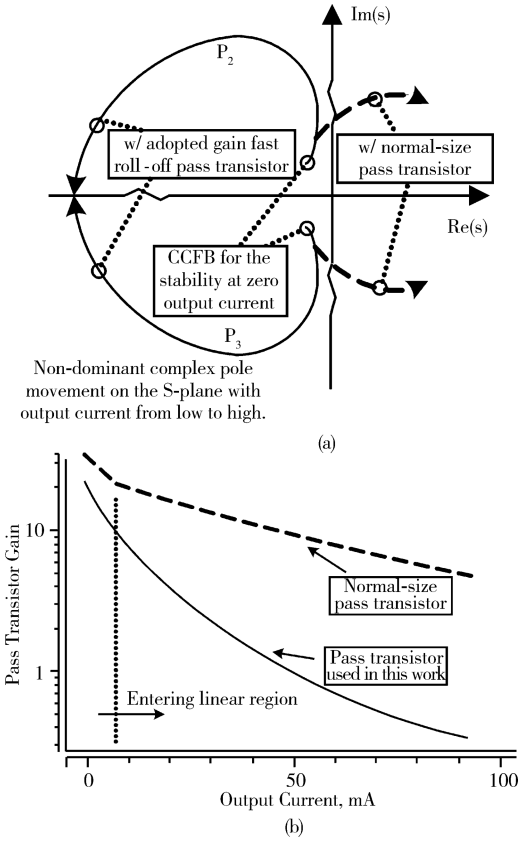

Fig. 2. Non-dominant complex pole movement with output current and associated PT gain roll-off. (a) Non-dominant complex pole movement. (b) Gain fast roll-off pass transistor.

finally right-half-plane (RHP) poles when I_L is high enough (the dashed line in Fig. 2(a)). To solve this problem, the gain

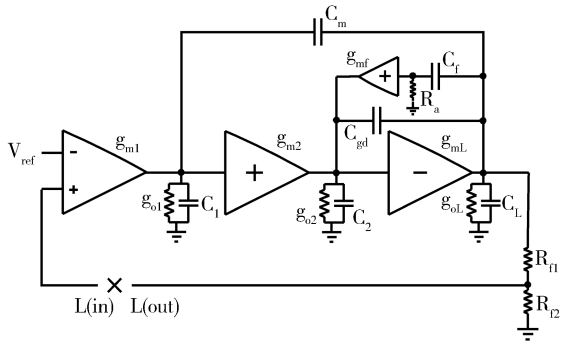

Fig. 3. Equivalent small-signal model of the proposed LDO circuit for loop-gain analysis.

fast roll-off PT is introduced into the system. The W/L ratio of the PT is reduced by several times the value usually adopted. The increase of I_L will force the transistor to enter the linear region quickly as shown in Fig. 2(b). The CCFB stage becomes less effective with increasing I_L and to some extent the active compensation approach is "disabled" when I_L is high enough. The Q will then decrease and finally the complex poles become a single pole far beyond the unity-gain bandwidth. As a result the LDO is stable with increasing I_L(solid line in Fig. 2(b)).

3. Detailed stability analysis

In order to determine the circuit parameters in the design, more precise analysis of the LDO's frequency response is derived below based on the equivalent small-signal model shown in Fig. 3. In the analysis, g_{m1}, g_{m2}, and g_{mL} represent the transconductance of the first and second stages of the error amplifier and pass transistor as in Fig. 1(a), respectively. g_{o1}, g_{o2},

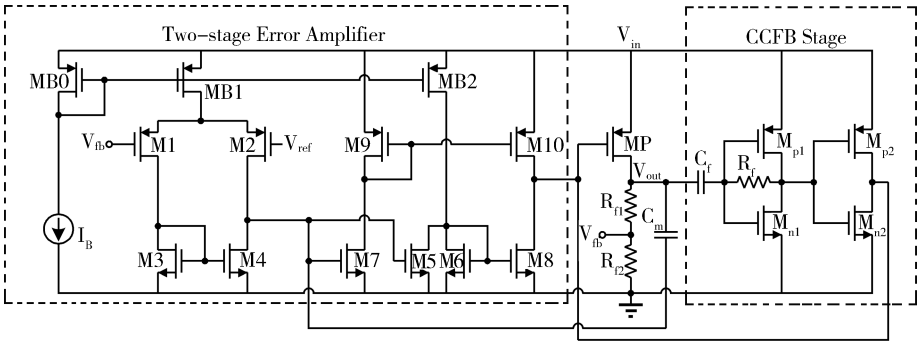

Fig. 4. Complete transistor-level schematic of the LDO.

and g_{oL} are the conductance seen at the output of each stage. C_1, C_2 and C_L are the parasitic capacitors at the output of each stage and C_{gd} is the drain-gate parasitic capacitor of the pass transistor. Specifically, C_L is for the modeling of the power-line parasitic and can be up to 100 pF. C_m, C_f are the two compensation capacitors and R_{f1}, R_{f2} are the two feedback resistors as in Fig. 1(a).

The loop transform function of the LDO can then be expressed as

$$L(s) \simeq \frac{FA_{DC}\left(1+sR_aC_f\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+\frac{sC_A}{g_{m2}}\right)\left[1+s\left(\frac{1}{\omega_2}+\frac{1}{\omega_3}\right)+\frac{s^2R_aC_f}{\omega_2}\right]}, \tag{3}$$

where $C_A \simeq (g_{0L}/g_{mL})C_2 + g_{mf}R_aC_f$, $F = R_{f2}/(R_{f1}+R_{f2})$, $A_{DC} = g_{m1}\,g_{m2}\,g_{mL}/g_{o1}g_{o2}\,g_{oL}$ and $p_{-3dB} = g_{o1}\,g_{o2}\,g_{oL}C_m g_{m2}g_{mL}$ are the feedback factor, the forward gain and the dominant pole of the LDO loop, respectively. ω_2, ω_2 is equal to

$$\omega_2 = C_A g_{mL}/\left(C_2+C_{gd}\right)C_L, \tag{4}$$

$$\omega_3 = C_A g_{mL}/\left(C_2+C_{gd}\right)g_{oL}R_aC_f. \tag{5}$$

As can be seen from Eqs. (4) and (5), a higher load current results in larger g_{mL} and thus ω_2 will be at a higher frequency. Meanwhile, ω_3 will be at a lower frequency due to the decrease of g_{mL}/g_{oL} when the PT begins the gain roll-off. So the two frequencies change in different directions with load current.

Based on Eq. (3), besides the dominant pole p_{-3dB}, the LDO also has a non-dominant pole $p_1 = -g_{m2}/C_A$, a left-half-plane (LHP) zero $z_1 = -1/R_aC_f$ as well as a pair of non-dominant complex poles $p_{2,3}$. Since p_1 will decrease the phase margin while z_1 can increase it, by choosing their locations to be approximately equal to each other, the phase margin will not be affected by them. Then the stability of the loop will mainly be determined by the location of $p_{2,3}$. Letting

$$\omega_{adpt} = \omega_2\omega_3/(\omega_2+\omega_3), \tag{6}$$

we have

$$p_{2,3} = -\frac{\omega_2}{\omega_{adpt}2R_aC_f}\left(1 \pm j\sqrt{\frac{4R_aC_f\omega_{adpt}^2}{\omega_2}-1}\right). \tag{7}$$

The Q value of $p_{2,3}$ is

$$Q = \sqrt{\left(4R_aC_f\omega_{adpt}^2/\omega_2\right)-1}. \tag{8}$$

Based on Eqs. (6)–(8), the location and the Q of the complex poles are adaptively changing with ω_{adpt} and will be analyzed in low, medium and high load current conditions, respectively. First, when the load current is low, $\omega_2 \ll \omega_3$. According to Eq. (4), $\omega_{adpt} \simeq \omega_2$. Then, replacing ω_{adpt} in Eq. (8) with ω_2, we get

$$Q = \sqrt{4R_aC_f\omega_2 - 1}. \tag{9}$$

This will decrease as the load current decreases. When the Q and $|p_{2,3}|$ values are chosen considering the total quiescent current and phase margin constraints, the LDO can be stable without a minimum load current requirement. Second, when the load current continues to increase and the PT enters the linear region, ω_3 will become smaller and comparable with ω_2. Substituting the ω_{adpt} in Eq. (6) with $\omega_2\omega_3/(\omega_2+\omega_3)$, we have

$$Q = \sqrt{\left[4R_aC_f\omega_1\omega_2^2\Big/(\omega_1+\omega_2)^2\right]-1}. \tag{10}$$

Q will stop increasing and subsequently decreasing due to the gain roll-off of the PT. Since $|p_{2,3}|$ continues to increase its magnitude, the worst-case phase margin happens when Q is still increasing. Third, when the load current is very high, $\omega_2 \gg \omega_3$. $p_{2,3}$ will be replaced by a single pole $\omega_{adpt} = \omega_3$. This pole will be far beyond the loop unity gain-bandwidth (UGB) of the LDO and can be neglected.

Figure 4 shows the complete transistor-level implementation of the proposed LDO circuit. In the two-stage error-amplifier, a transconductance-enhancement circuit based on M5, M6 and M8 is introduced to boost the g_m of the second stage[6]. Also, it can improve on the slew rate at the gate of MP and in turn makes the LDO have small output-voltage ripples when fast load current variations exist. The resistor R_f is connected between the gate and drain of both Mp1 and Mn1. This makes the feedback transconductance more controllable as indicated in Eq. (2). It also makes the gate biases of Mp1 and Mn1 equal to their respective drain-source voltages. The gate biases of Mp2 and Mn2 are the same as those of Mp1 and Mn2.

Simulation results of the LDO's loop frequency response are given in Fig. 5. With the use of the AFC technique, a phase margin larger than 80° can be achieved with a load current range from 0 to 100 mA. The UGB is approximately 200 kHz. The DC loop-gain is 101 dB at 0 mA and 73 dB at 60 mA.

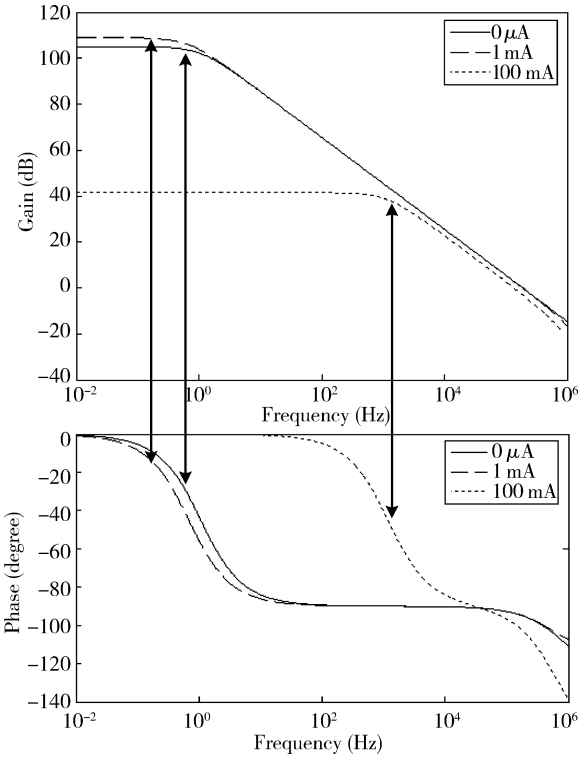

Fig. 5. Simulation results of the LDO's loop frequency response.

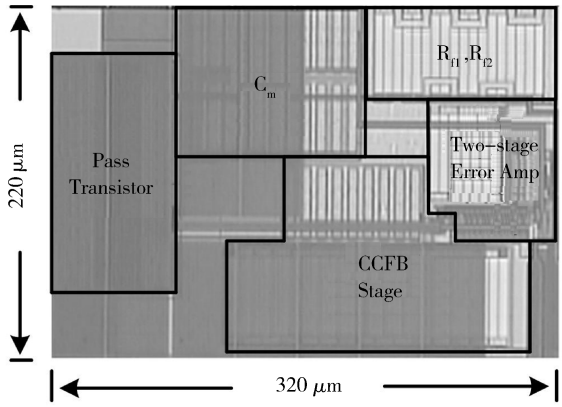

Fig. 6. Micro-photograph of the LDO.

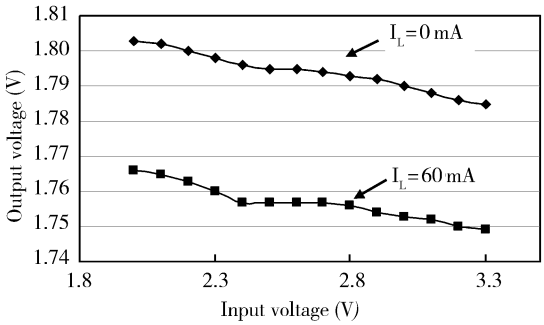

Fig. 7. Measured line regulation of the LDO.

4. Experimental results

The LDO with AFC is fabricated in a standard 0.35 μm CMOS process. A micro-photograph of the chip is shown in Fig. 6. It can deliver up to 60 mA load current with a quiescent ground current of 54 μA. The measured line regulation of the LDO with an input voltage from 2 to 3.3 V is shown in Fig. 7, and is 13.8 mV/V and 13.1 mV/V at 0 mA and 60 mA load current condition respectively. A detailed summary of the LDO's regulated output voltage error due to line and load variation is listed in Table 1. Figure 8 shows the LDO's transient response with the load current switching between 0 and 60 mA. The output capacitor for the modeling of the power-line parasitic is set to be 100 pF. It can be seen that the LDO is stable and can settle within 10 μs. The power-supply rejection ratio (PSRR) of the LDO with 20 mA load current is measured and the results are given in Fig. 9. The PSRR at 1 kHz is −40.6 dB. In the test setup, the input voltage was set to have a DC value of 2.1 V together with a 1 kHz 200 mV peak-to-peak rip-

Table 1. Summary of the LDO's line regulation and load regulation performances.

Parameter	Preset V_{out} (V)	V_{out} variation (mV)	Error (%)
V_{in} from 2 to 3.3 V @ 0 mA I_L	1.8	18	1
V_{in} from 2 to 3.3 V @ 60 mA I_L	1.8	17	0.94
I_L from 0 to 60 mA @ 2 V V_{in}	1.8	37	2.06
I_L from 0 to 60 mA @ 3.3 V V_{in}	1.8	36	2

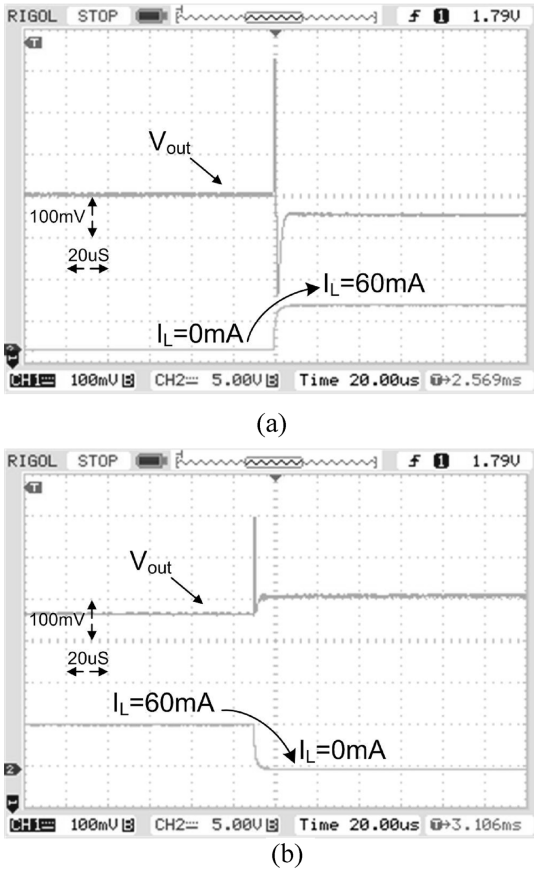

Fig. 8. Transient response of the LDO. (a) Load current switching from 0 to 60 mA. (b) Load current switching from 60 to 0 mA.

Table 2. Performance summary and comparison.

Parameter	JSSC'07[7]	TCAS-I'07[8]	This work
Technology	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.35 μm
Active chip area (mm^2)	0.12	0.12	0.07
Output current (mA)	0.1–100	0–50	0–60
Quiescent current (μA)	100	65	54
Input voltage range (V)	1.2–3.3	3–4	2–3.3
Output voltage (V)	1	2.8	1.8
Dropout voltage (mV)	200	200	200
Transient output voltage variation (Full-load transient) (mV)	—*	< 90	< 350
Transient output voltage settling (Full-load transient) (μs)	—*	< 15	< 10
Load regulation (mV/mA @ minimum V_{in})	–0.338	–0.8	–1.05
Line regulation (mV/V @ maximum I_L)	0.344	–2.5	–13.1
Maximum error due to line and load variation (%)	3.38	1.43	2.06

*This is not included for the full-load transient comparison because a minimum output current of 100 μA is required.

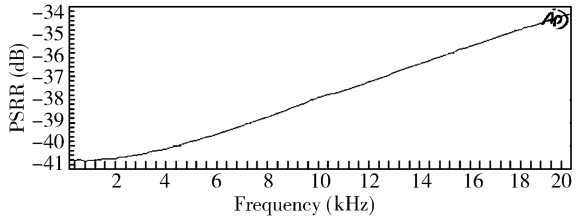

Fig. 9. Measured PSRR performance of the full on-chip LDO.

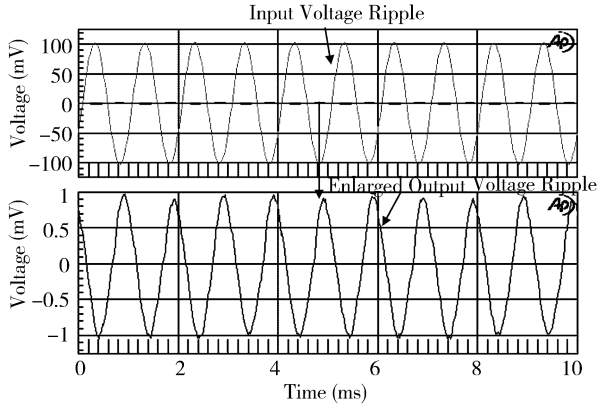

Fig. 10. Output ripple voltage of the LDO with 200 mV peak-to-peak input ripple voltage.

ple voltage. The output voltage is 1.8 V with a 2 mV ripple (shown in Fig. 10). As a result the output voltage ripple coefficient is 0.0011. Since our target is focused on full on-chip integration, the measured PSRR is acceptable in applications where the noise performance requirement is not as stringent as the cost constraint.

The LDO's main performances are summarized in Table 2 and compared with other recently published full on-chip LDOs[7, 8]. The output voltage error due to line regulation and load regulation is still within 2.1% with V_{in} changing from 2 to 3.3 V and I_L from 0 to 60 mA, though it is poorer compared to Refs. [7, 8]. Considering this, the LDO is suitable for moderate-precision applications where the board-level cost is a major concern. The active chip area is reduced to 58% compared to both Refs. [7, 8], showing a very compact LDO structure. Furthermore, there is no minimum output current requirement compared with Ref. [7] (100 μA minimum in Ref. [7]). In addition, the proposed structure is more suitable for low-voltage applications compared to Ref. [8].

5. Conclusion

In this paper a full on-chip and area-efficient CMOS LDO is proposed and successfully verified by experimental results. Full on-chip integration and the LDO's stability in the full load current range are achieved by using the proposed adaptive frequency compensation technique. The LDO's area efficiency is also significantly improved (reduced to 58% compared to state-of-the-art designs using technologies with the same feature size) by the introduction of a small-size gain fast roll-off PMOS pass transistor, making it very suitable for highly integrated system-on-chip applications.

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References

[1] Shi C L, Walker B C, Zeisel E, et al. A highly integrated power management IC for advanced mobile applications. IEEE J Solid-State Circuits, 2007, 42(8): 1723

[2] Rincon-Mora G A, Allen P E. A low-voltage, low quiescent current, low drop-out regulator. IEEE J Solid-State Circuits, 1998, 33(1): 36

[3] Leung K N, Mok P K T, Lau S K. A low-voltage CMOS low-dropout regulator with enhanced loop response. IEEE Symposium on Circuits and Systems, Vancouver, 2004, 1: 385

[4] Al-Shyoukh M, Lee H, Perez R A. Transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation. IEEE J Solid-State Circuits, 2007, 42(8): 1732

[5] Lau S K, Leung K N, Mok P K T. Analysis of low-dropout regulator topologies for low-voltage regulation. IEEE International Conference on Electronic Device and Solid-state Circuits, Hong Kong, 2003: 379

[6] Leung K N, Mok P K T. A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation. IEEE J Solid-State Circuits, 2003, 38(10): 1691

[7] Lau S K, Mok P K T, Leung K N. A low-dropout regulator for SoC with Q-reduction. IEEE J Solid-State Circuits, 2007, 42(3): 658

[8] Miliken R J, Silva-Martínez J, Sánchez-Sinencio E. Full on-chip CMOS low-dropout voltage regulator. IEEE Trans Circuit Syst I, 2007, 54(9): 1879

[9] Ahuja B K. An improved frequency compensation technique for CMOS operational amplifiers. IEEE J Solid-State Circuits, 1983, 18(6): 629

[10] Lee H, Mok P K T. Active-feedback frequency-compensation technique for low-power multistage amplifiers. IEEE J Solid-State Circuits, 2003, 38(3): 511

[11] Peng X, Sansen W. Transconductance with capacitances feedback compensation for multistage amplifiers. IEEE J Solid-State Circuits, 2005, 40(7): 1514