Low-power variable frequency PFC converters*

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Abstract: Based on the SinoMOS 1 μm 40 V CMOS process, a novel power factor corrention (PFC) converter with a low-power variable frequency function is presented. The circuit introduces a multi-vector error amplifier and a programmable oscillator to achieve frequency modulation, which provides a rapid dynamic response and precise output voltage clamping with low power in the entire load. According to the external load variation, the system can modulate the circuit operating frequency linearly, thereby ensuring that the PFC converter can work in frequency conversion-mode. Measured results show that the normal operating frequency of the PFC converter is 5–6 kHz, the start-up current is 36 μA, the stable operating current is only 2.43 mA, the efficiency is 97.3%, the power factor (PF) is 0.988, THD is 3.8%, the load adjust rate is 3%, and the linear adjust rate is less than 1%. Both theoretical and practical results reveal that the power consumption of the whole supply system is reduced efficiently, especially when the load varies. The active die area of the PFC converter chip is 1.61×1.52 mm^2.

Key words: power factor correction; pulse width modulation; variable frequency; multi-vector error amplifier; programmable oscillator

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1. Introduction

At present, environmentally-friendly power-saving power supply design is introducing great challenges to power factor correction (PFC) converters. In order to comply with IEC61000-3-2 limits for harmonic current emissions and, at the same time, to process low cost and high performance to meet the demands of electrical equipment (including ballasts, notebook adapters, LCD TV and LCD displays, etc.) to be light, thin, small, and especially low-power, the one cycle control (OCC) PFC technique has been generally studied. Some companies, such as Infineon and TR, have developed OCC PFC chips. Compared with the conventional control technique, it is contended that OCC leads to reductions in complexity, cost and design time without a sacrifice in performance[1]. However，it is still currently facing the problem of how to improve the efficiency of a PFC converter in the entire load and reduce its power consumption. For PFC converters, the major power losses are switching and conduction losses, which are influenced by the system dynamic characteristics and switching frequency[2]. If the load lightens suddenly, the output voltage will rise sharply, along with an increase in the operating frequency, which leads to more power loss. On the other hand, in heavy loads, the output voltage decreases correspondingly, which induces a larger conduction angle and longer current interval time, thereby causing more power loss and zero-crossing distortion[3, 4].

In this paper, a novel PFC converter with a low-power electric-saving function is presented, which operates in the variable frequency mode; namely, the PFC converter can modulate the operating frequency according to the external load so as to obtain a rapid dynamic response and less power loss[5]. The basic principle of the variable frequency mode is as follows: under light loads, the switching frequency is reduced linearly by extending the turn-off time of PFC converter; when there is no load, the system works in interval operating mode and the PWM output is cut off completely until the external storage inductor releases all the energy; under heavy loads, the switching frequency is improved by the oscillator, thereby compensating energy consumption on the external storage components (inductor and capacitance) and avoiding a large current interval time in time. The variable frequency mode enables the PFC converter to respond to load changes in a timely manner and minimize the standby power.

2. System description

The topology of the PFC converter with the low-power variable frequency function is shown in Fig. 1. The pulse width modulation (PWM) technique is used to control the PFC switch. The system is composed of a multi-vector error amplifier (EA), a programmable oscillator, a periodic self-starting circuit, zero-current detection, synchronization slope compensation, a leading-edge blanking block, an output power limit circuit, over-current and over-temperature protection blocks, an under voltage lockout circuit, etc.

The inverting input of the multi-vector EA is referenced to INV sensed from the linear rectifier output voltage. The output of the EA is referenced to COMP between which and ground a compensation network is suggested to create a precise clamping protection. The output of the EA is used to determine the on-time of the PWM output and hence regulates the output voltage. To avoid an extra low operating frequency and achieve

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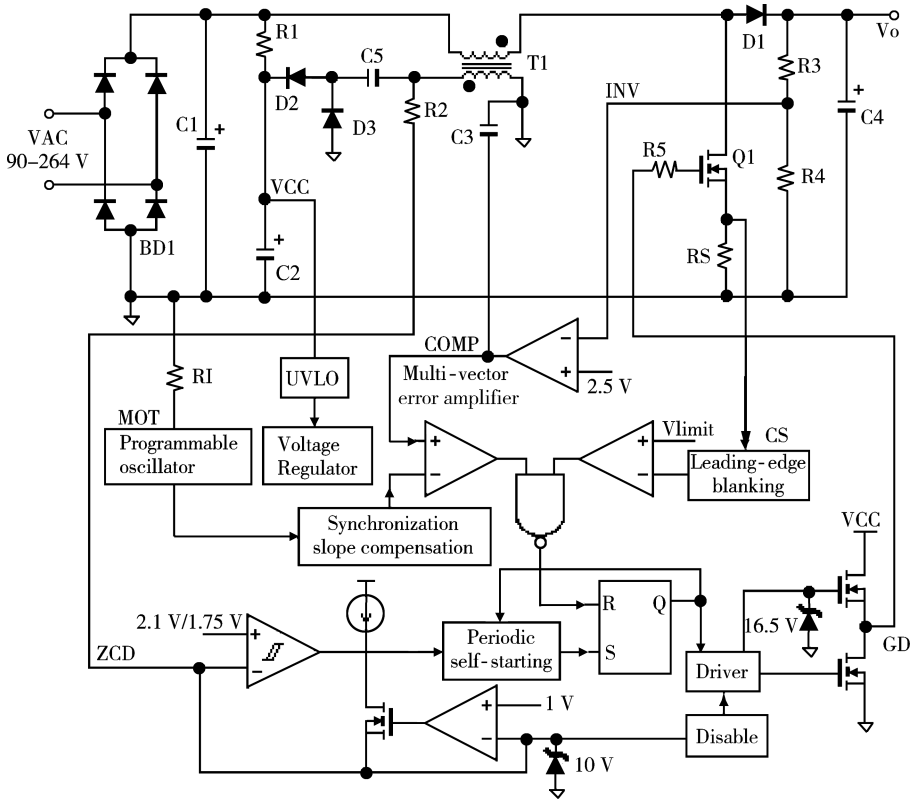

Fig. 1. PFC converter topology.

brownout protection, the maximum on-time is programmed by one adjustable resistor RI connected between MOT and ground, that is, the slope rate of the sawtooth wave generated by oscillator is determined by RI. The operating frequency of the programmable oscillator is controlled by a sampled signal derived from the load current. This sampled current signal is also fed into the CS pin. A high voltage on the CS pin will terminate a switching cycle immediately and the one cycle current limit is achieved. The zero-current detection of the inductor is achieved using its auxiliary winding. When the stored energy of the inductor is fully released to output, the voltage on ZCD will go down and a new switching cycle will be enabled after a ZCD trigger, thus switching loss and noise can be minimized. An inherent periodic self-starting block is built in to ensure proper start-up operation. The GD pin is the driver output, which adopts totem-pole driver output to drive the external power MOSFET.

When the system operates in a steady state, the output signal bandwidth of the EA is limited to below 20 Hz in order to achieve a low input current total harmonic distortion (THD) within one input period of 90–264 V_{AC}. When the external load varies suddenly, the multi-vector EA will generate a high-frequency dynamic response signal superimposed on the low-frequency output signal, and so provides a rapid transient response and precise output voltage clamping. The frequency of the oscillator follows the load changes. PWM control is achieved by both the multi-vector EA and the programmable oscillator. Under heavy loads, the output current rises, leading to a higher PWM frequency; under light loads, the on-time duty cycle of PWM is reduced with a lower operating frequency; if there is no load, PWM is cut off entirely and the system goes into interval operating mode. A ZCD signal triggers a new switching cycle once the stored energy of the external components is fully released to output.

The converter works in boundary mode such that the peak inductor current is always exactly twice the average current, and noise on the current sense or control signal can cause significant pulse width jitter. Slope compensation and a built-in debounce circuit can be used to alleviate this problem. In order to avoid a turn-on spike when the power MOSFET is switched on, it is necessary to employ leading edge blanking to generate a blanking period of around 400 ns.

3. Variable frequency PWM control

3.1. Multi-vector error amplifier

To realize the low-power electric-saving function, a multi-vector error amplifier is suggested. Compared to traditional EAs, its advantages lie in the fact that it will provide a high frequency transient response signal superimposed on a low frequency signal generated by traditional EAs, thereby avoiding significant phase delay and reducing the power consumption for detecting the input voltage required by the traditional PWM control circuit. Specifically speaking, the multi-vector EA possesses such characteristics as follows: in a steady state, the EA will output a control signal with a bandwidth of less than 20 Hz, which enables the turn-on time of the PWM output to vary in a slightly smaller range for a low input current THD[6] (the PWM output signal should have a high enough switching frequency to meet the demands of EMI testing and to decrease the development costs, and the second harmonic included in the PWM signal should be less than 150 kHz). As the load increases, the

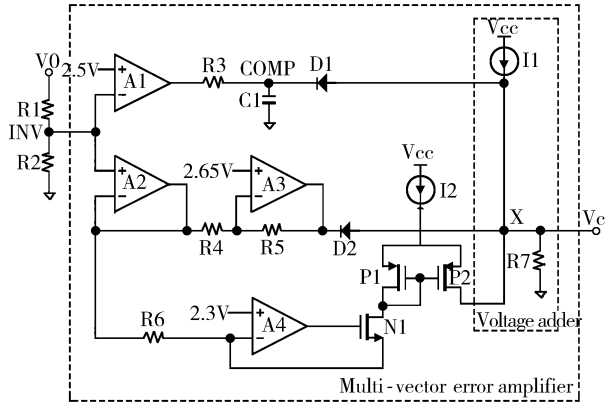

Fig. 2. Multi-vector error amplifier.

output voltage of the EA rises, which reduces the on-time duty ratio of the switch with a higher operating frequency improved by the oscillator, and the system goes into variable frequency mode; conversely, under light loads, the output voltage of the EA decreases, the on-time duty ratio of the switch increases relatively, and the PWM frequency is reduced and remains consistent with the oscillator. It should be noted that the lowest PWM operating frequency should be higher than the audio frequency. In addition, the maximum on-time is programmed by RI (as mentioned above) to avoid an extra low operating frequency and achieve brownout protection.

The multi-vector EA is shown in Fig. 2. The linear rectifier output voltage is pulled down to an appropriate scope by divider resistors R1 and R2, and is fed into INV. It is clear that THD is an important indicator for the reliability of the power system. To achieve a low input current THD, a stable low frequency output signal must be produced by the EA in one AC cycle. When the system operates normally, the feedback voltage is in the range of 2.3–2.5 V, all current of current source I_1 flows through the resistor R7, and the PFC converter works in a steady state. With the decrease of load, the feedback voltage rises. If the feedback voltage reaches a range of 2.5–2.65 V, the comparator A1 will extract current from I_1 and so the voltage V_o across R7 reduces: the system is in variable frequency mode which will lead to a longer turn-on time and a lower switching frequency. When the load lightens continuously until the feedback voltage is higher than 2.65 V, both A1 and A3 extract current from I_1, V_o decreases rapidly, the system goes into interval operating mode and the external energy storage components release the energy fully. On the other hand, a heavy load forces the feedback voltage to decrease; once the feedback voltage is lower than 2.3 V, the comparator A4 will make the transistor N1 open, thus there will be a current path between the power V_{CC} and R7 through the current mirror P1-P2. Accordingly V_o is improved linearly, and there is a shorter turn-on time and a higher switching frequency.

The multi-vector EA is equivalent to a current adder, which adds three branch currents vectorially at point X. The control voltage V_o that is determined by the vectorial sum of the three currents through R7 can be expressed as:

$$V_o = R_7 \times \left[I_1 - G_{m1} V_{IN1} - G_{m3} V_{IN3} + \frac{1}{2} I_2 \right], \quad (1)$$

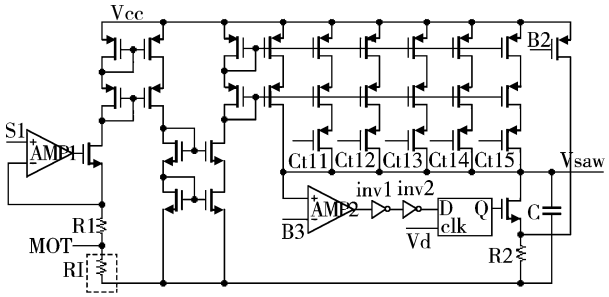

Fig. 3. Programmable oscillator.

where G_{m1} and G_{m3} are equivalent trans-conductances of the trans-conductance amplifiers A1 and A3 respectively, and V_{IN1} and V_{IN3} are the input signals of A1 and A3. This adder outputs varied control signals with the corresponding gain and bandwidth in the light of different sampling voltages at INV, thereby providing a better transient response and achieving the goal of low-power design. The resistor R3 and capacitance C1 are suggested at the COMP pin which could limit the bandwidth of A1 below 20 Hz. A3 or A4 provides the high frequency dynamic response added on the output signal of A1, and R4, R5 and R6 are used to regulate the gain of the high-bandwidth signal generated by A3 or A4. At the same time, voltage buffer A2 is proposed to eliminate the high-impedance voltage divider network caused by R1 and R2.

3.2. Programmable oscillator

Compared with the other general oscillators, the programmable oscillator makes the range of charge current of oscillator capacitor C a function of the load current, that is, the range of charge current of C is programmed by sampling the load current, then controlling the output PWM frequency of the converter. The topology is shown in Fig. 3. RI is an external adjustable resistor and helps to manually regulate the charge current of the oscillator capacitor. The S1 signal is sampled from the load current which is sensed by one resistor and serves as real time load monitoring to be used to regulate the charge current of the oscillator. Under a heavy load, the S1 signal rises, and the charge current of the oscillator increases too, thereby resulting in a higher frequency. As the load decreases, the S1 signal drops, and the oscillator works at a lower frequency; in particular, under no-load, the oscillator stops and the system is in interval operating mode. To accurately regulate oscillation frequency a programmable PMOS array is built-in, which can adjust the charge current slightly by signals Ctl1–Ctl5. The bias signal B2 provides 1 V compensation voltage for sawtooth wave output. If the output control signal V_o of the multi-vector EA is below 1 V, the switching frequency will fall to the minimum, namely, the oscillator stops. 1 V compensation helps to avoid false brownout protection and to increase the response speed of the capacitor. The bias signal B3 limits the peak of the sawtooth wave to 3 V. If V_o is higher than 3 V the switching frequency will rise to the maximum. It is clear that B2 and B3 decide the scope of the switching frequency. The power MOSFET driver signal V_d is fed back to control the discharge time of the capacitor, and then forces the system to operate in one cycle mode. In addition, the cascade structure is introduced to improve the linear adjust rate of the system.

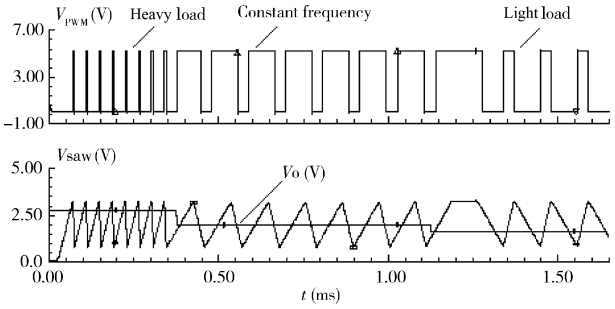

Fig. 4. PWM variable frequency operating mode.

The capacitor of the oscillator can be obtained from the following expression:

$$C = \frac{DI_{\mathrm{C}}}{f(V_{\mathrm{sawh}} - V_{\mathrm{sawl}})}, \tag{2}$$

where D is the duty cycle of the PWM signal, I_{C} is the charge current, V_{sawh} and V_{sawl} are the maximum and minimum output sawtooth voltages respectively, and f is the operating frequency. The longest turn-on time of PWM depends on the boost inductor, the smallest AC line voltage and the maximum output power.

$$T_{\mathrm{ON\,(max)}} = \frac{2LP_{\mathrm{o}}}{V_{\mathrm{rms}}^2}. \tag{3}$$

The control signal V_{o}, sampling current signal CS and output sawtooth of the programmable oscillator together determine the operating frequency of the PFC converter. In order to ensure the stability of the boundary current control, it is necessary to introduce a synchronization slope compensation circuit to prevent the turn-on time of PWM being too long.

3.3. Periodic self-starting circuit

Under no-load the power MOSFET turns off completely and the system moves into interval operating mode. To ensure proper start-up operation and minimize switching loss and noise, a periodic self-starting circuit is proposed. If the turn-off time of the switch is longer than 350 μs, no matter if the stored energy of the inductor is fully released or not, the periodic self-starting circuit will trigger a new switching cycle. The periodic self-starting circuit enables the PFC converter to operate efficiently between variable frequency mode and interval mode.

4. Results and discussion

Based on the SinoMOS 1.0 μm 40 V CMOS process BSIM3V3 Spice model, the feasibility of the low-power variable frequency PFC converter has been verified by the simulated and measured results. Figure 4 shows the simulated output signals of the multi-vector EA and programmable oscillator and the PWM signal in variable frequency mode. Under heavy loads, the control signal V_{o} is close to 3 V, and the sawtooth frequency remains 22.67 kHz. With decreasing load, the PWM frequency reduces. Under normal conditions, the system operates at a constant frequency which is also 5.17 kHz; at this time the PWM duty cycle is maximum. Under light loads, due to the reduction of the charge current for the oscillator the PWM duty cycle decreases correspondingly with a lower frequency. Figure 5 depicts the measured PWM waves under conditions of V_{cc} = 15 V and output power P_{o} = 36 W. Figure 5(a) illustrates the PWM output signal at a constant frequency with INV = 2.45 V. It is obvious that the rise time is twice that of the sawtooth fall time after slope compensation, and the measured turn-on time of the gate driver signal is 114.8 μs: the system works in a stable state. Figure 5(b) shows the PWM signal with INV = 2.55 V. To reduce the load current, the turn-on time of the gate driver signal drops to 19 μs significantly, and the system has a good dynamic respond speed.

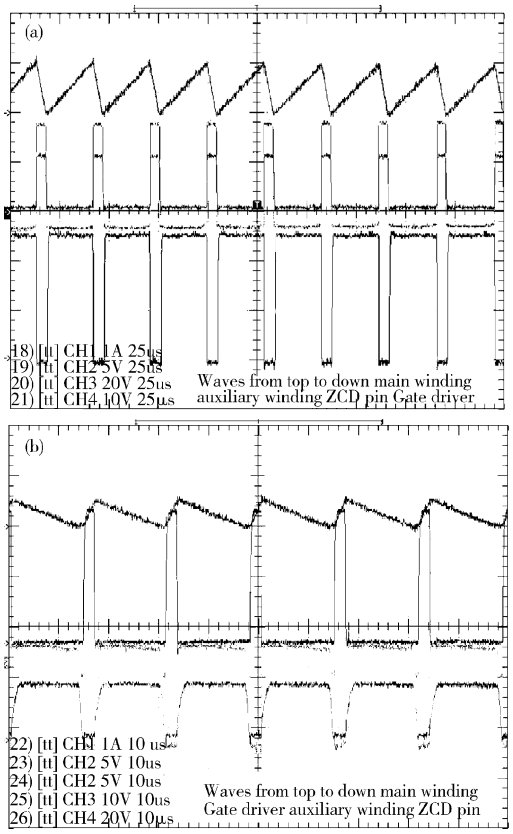

Fig. 5. PWM converter system test results. (a) Constant frequency operating state. (b) Light load operating state.

Table 1. Performance summary of the low-power variable frequency PFC converter. V_{cc} = 15 V, P_{o} = 36 W.

Parameter	Value
PF	0.988
THD	3.8%
η	97.3%
Start-up current	36 μA
Operating current	2.43 mA
Linear adjust rate	$\leqslant$ 1%
Operating frequency	5–6 kHz
Load adjust rate	3%
Die area	1.61 × 1.52 mm^2

Table 1 lists the actual measured results of the PFC converter, which demonstrate that the rectified line current can automatically follow the sinusoidal line-voltage with a low input current THD at 60 Hz 220 V_{AC}. Referring to the other PFC chips introduced in Refs. [1, 3, 4, 6], this low-power variable

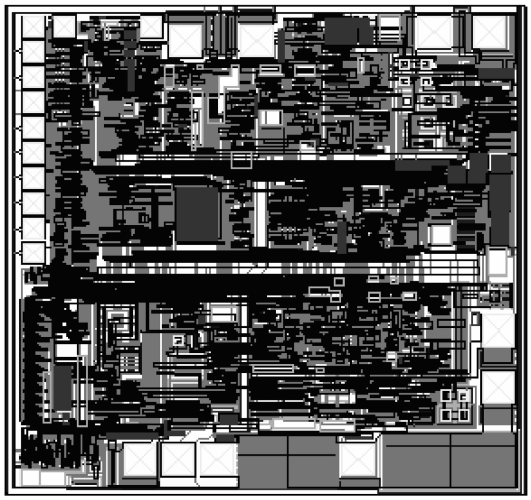

Fig. 6. Low-power variable frequency mode PWM converter layout.

frequency PFC converter has good enough PF and THD to be consistent with IEC61000-3-2 limits and reduce dissipation in the rectifier bridge, as well as good linear and load adjust rates. Furthermore, it has lower start-up and operating current. Also, its efficiency is higher than that traditional complete PFC by 2%–3%, even at very light loads. The low current consumption minimizes the power dissipated by both the start-up resistor and the self-supply circuit, and the high efficiency at different load conditions ensures low switching losses in the MOSFET. Speeding up the control loop leads to a compromise between an acceptably rapid transient response and a reasonably high PF. Therefore it can be concluded that the PFC converter meets the requirements of low-power electric-saving design.The low-power variable frequency mode PWM converter layout is shown in Fig. 6. The active die area of the PFC converter ship is $1.61 \times 1.52\,\mathrm{mm}^2$.

5. Conclusions

A novel method for reducing the power dissipation and improving the efficiency of a switching power supply system is presented. Based on the SinoMOS 1.0 μm 40 V CMOS process, a low-power variable frequency PFC converter is described. The multi-vector EA and programmable oscillator enable the system to modulate the PWM switching frequency in a timely manner in terms of external load. The PFC converter can transform efficiently between variable frequency and interval mode, hence reducing the power dissipation of the whole power system and increasing the useful power, especially under heavy or light loads. The normal operating frequency is 5–6 kHz, the system start-up current is 36 μA, the stable operating current is only 2.43 mA, efficiency is 97.3%, PF is 0.988, THD is 3.8%, the load adjust rate is 3% and the linear adjust rate is less than 1%. All these parameter indicators meet the requirements of a low-power electric-saving PFC converter. The active die area is $1.61 \times 1.52\,\mathrm{mm}^2$.

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