A 4 GHz quadrature output fractional-N frequency synthesizer for an IR-UWB transceiver*

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Abstract: This paper describes a 4 GHz fractional-N frequency synthesizer for a 3.1 to 5 GHz IR-UWB transceiver. Designed in a 0.18 μm mixed-signal & RF 1P6M CMOS process, the operating range of the synthesizer is 3.74 to 4.44 GHz. By using an 18-bit third-order Σ–Δ modulator, the synthesizer achieves a frequency resolution of 15 Hz when the reference frequency is 20 MHz. The measured amplitude mismatch and phase error between I and Q signals are less than 0.1 dB and 0.8° respectively. The measured phase noise is –116 dBc/Hz at 3 MHz offset for a 4 GHz output. Measured spurious tones are lower than –60 dBc. The settling time is within 80 μs. The core circuit conupSigmaes only 38.2 mW from a 1.8 V power supply.

Key words: frequency synthesizer; dual-modulus prescaler; Σ–Δ modulator; QVCO
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1. Introduction

In 1993, Professor Scholtz proposed impulse-radio ultra-wideband (IR-UWB) technology. IR-UWB technology has advantages in complexity and power, because it does not need fast Fourier transform (FFT), and circuits can be shut down between impulse intervals[1]. In recent years, IR-UWB technology has attracted more and more interest since the FCC released an unlicensed spectrum of 3.1–10.6 GHz for UWB applications. Considering the limitation of the UWB systems' working spectrum, the IR-UWB transceivers usually employ frequency conversion architecture that needs local oscillator (LO) signals as the carrier wave. The transmitter adopts BPSK modulation, and the receiver adopts quadrature coherent demodulation that exposes a requirement on the design of carrier-synchronization arithmetic and quadrature LO signals. The carrier-synchronization arithmetic requires a programmable carrier frequency, and the frequency resolution is limited to 5 kHz. In addition, in wireless communication, phase noise and spurious tones of synthesizer will degrade the channel signal to noise ratio (SNR) and increase the bit error rate (BER) during data transmission, consequently, the main challenge of the synthesizer in the IR-UWB system is the difficulty in enabling its output resolution under 5 kHz and keeping the quadrature LO signals' phase noise and spur as low as possible. Recently, CMOS technology has gained a great deal of attention due to its high integrity and low cost. Along with its rapid progress, the cutoff frequency of the deep submicron CMOS devices has achieved 100 GHz. Hence, it is possible to implement the IR-UWB transceiver in the CMOS process[2]. In this paper, a 4 GHz fractional-N frequency synthesizer is designed in a 0.18 μm mixed-signal & RF CMOS process.

2. Frequency synthesizer architecture

Figure 1 illustrates the structure of the Σ–Δ fractional-N frequency synthesizer. This synthesizer is composed of a phase frequency detector (PFD), a charge pump (CP), a third-order loop filter, a voltage controlled oscillator (VCO) and a programmable fractional frequency divider. The programmable fractional divider includes a divide-by-$M/M+1$ dual-modulus prescaler (DMP), a programmable counter P, a swallow counter S, and a k-bit Σ–Δ modulator. The division ratio is in the range from 185 to 215 since the comparison frequency is 20 MHz and the output frequency range is from 3.7 to 4.3 GHz. We have chosen to directly synthesize the 4 GHz signal for better spectrum purity without frequency multiplication. In integer-N architecture, the reference frequency must be equal to the desired frequency resolution, because the programmable divider changes division ratio N only in integer steps. In this paper, we have chosen a fractional-N synthesis technique since fractional-N synthesis allows a synthesizer to achieve arbitrarily fine frequency resolution.

The DMP is able to divide by M and $M+1$ with some additional logic. When the DMP modulus bit MC is high, the

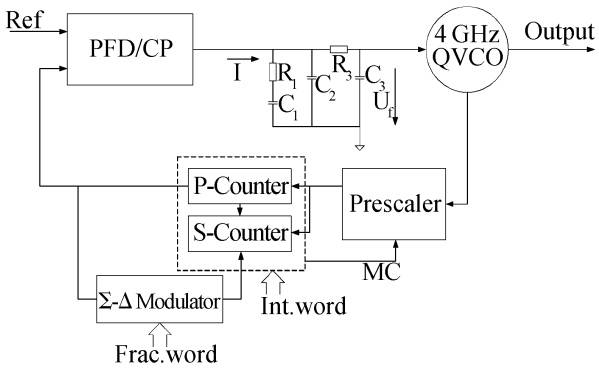

Fig. 1. Fractional-N frequency synthesizer architecture.

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DMP divides by $M + 1$ and the S-counter counts the output pulses, until a number S is reached. It then changes MC to low, resetting the prescaler division to M. The P-counter also counts the DMP output pulses, until a number P is reached. It then resets both the S- as the P-counter, and the division process is restarted. This means that during one output period of the full divider, the DMP has divided S times by $M + 1$ and $P - S$ times by M, such that the overall division number becomes:

$$N = (M + 1) S + M (P - S) = PM + S. \quad (1)$$

If S is variable between 0 and $M - 1$, the complete range of division numbers can be realized. For a proper reset by the P-counter, P must be larger than the largest value of S. For a given minimum synthesizable frequency, the prescaler division number is limited, since the smallest obtainable division number is

$$N_{\min} = M^2. \quad (2)$$

Generally, M is chosen to be 2^n according to the structure of the DMP. We have chosen n to be 3, resulting in M to be 8 that makes $N_{\min}$ smaller than 185. P-counter and S-counter have been chosen to be 5-bit programmable counters which have been realized by digital CMOS design flow. When a digital word K is applied to the k-bit Σ–Δ modulator, a carry signal is produced on average every $K/2^k$ cycles of the reference frequency. This carry signal controls the divider modulus that results in an average division number:

$$N_{\text{frac}} = N + \frac{K}{2^k}. \quad (3)$$

We have chosen K to be 18 with the less significant bit (LSB) to be applied by dithering signal[3]. When the reference frequency is 20 MHz, the output resolution can achieve:

$$F_{\text{resolution}} = \frac{1}{2^{17}} F_{\text{ref}} \approx 15 \text{ Hz}. \quad (4)$$

There are three main solutions to generate quadrature local oscillator signals: VCO combined with the phase shifting filter, VCO working at double required frequency and followed by divider by two or quadrature VCO (QVCO). Phase shifting usually has serious quadruature phase mismatch that interferes with the performance of quadrature demodulation. Frequency division needs a double required frequency oscillator and divider that results in much more power conupSigmaption. In this paper, QVCO is employed to achieve low conupSigmaption and low quadrature phase mismatch. The QVCO output drives the dual-modulus prescaler via a buffer, another buffer supplies the quadrature output of the synthesizer.

The noise contributions mainly include VCO noise, charge pump noise, and Σ–Δ shaped noise[4]. Moreover, the fractional-N synthesizer suffers from fractional spur since the fractional-N synthesis technique modulates the instantaneous division ratio. To optimize the phase noise of the VCO and charge pump, we have chosen the VCO gain and current of CP to be 80 MHz/V and 200 μA. To suppress the high frequency noise generated by the third-order Σ–Δ modulator, we have chosen a third-order loop filter. The bandwidth is designed to be 145 kHz that is enough to realize a settling time of less than 80 μs. Table 1 lists some important loop parameters.

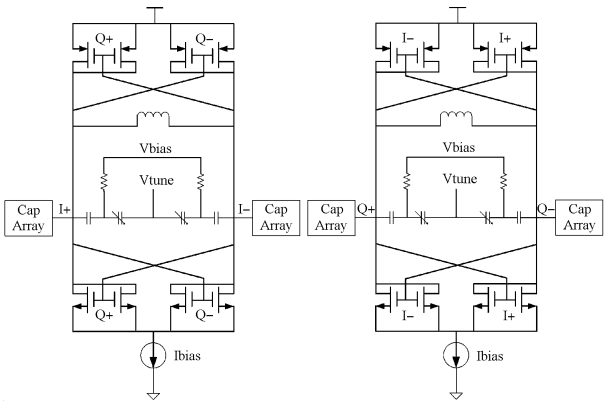

Fig. 2. Schematic of LC-tank QVCO.

3. Key circuit design

3.1. Quadrature VCO

Figure 2 shows the schematic of the LC-tank QVCO that is designed to provide the I/Q local oscillator signals to the mixer and prescaler[5]. To achieve low power conupSigmaption and low phase noise performance in an LC VCO, the most effective way is to maximize the quality factor of the tank circuit: basically the inductor. We use single layer octagonal inductors in a mixed-signal & RF CMOS process with 2.17 μm thick Al metal, because they have a higher quality factor compared to square spirals for the same inductance value. To enhance the Q factor, we use a broken guard ring around the inductor that avoids the generation of induced currents in the ring. To suppress the phase noise, we design a symmetrical layout. The inductor is designed and simulated in commercial electromagnetic simulator HFSS. Simulated results show the quality factor is about 8 over the frequency range from 3.7 to 4.45 GHz. On-chip varactors for VCOs are implemented using A-MOS varactors. Compared to p–n junctions or I-MOS varactors, the A-MOS varactor displays the lower power conupSigmaption and phase noise at larger offset frequencies from the carrier. The parasitic series resistance in the gate access terminal is particularly critical and requires careful layout.

3.2. Dual-modulus prescaler

Figure 3 shows the block diagram of the divide-by-8/9 dual-modulus prescaler[6]. The prescaler consists of a divide-by-4/5 synchronous divider, a divide-by-2 divider, and a modulus control block. The high speed 4/5 synchronous divider consists of three differential CML D flip-flops and two OR gates for modulus selection. The first two flip-flops with a negative feedback form an injection-locked frequency divider (ILFD) which can operate as a divide-by-4 divider, while the third flip-flop adds an extra clock period delay for divide-by-5. To better balance the propagation delays among the three flip-flops, the output of the first flip-flop is used to drive the divide-by-2 divider because the second flip-flop output drives both the first and the third flip-flops. The divide-by-2 divider is a D flip-flop with a negative feedback that forms an ILFD. In the modulus control circuit, an AND gate is used to generate the mod-

Table 1. Loop parameters of frequency synthesizer.

Loop parameter	Value	Loop filter component	Value
Reference clock	20 MHz	R_1	12 kΩ
Loop bandwidth	145 kHz	C_1	330 pF
Phase margin	57 degree	C_2	22 pF
Current of CP	200 μA	R_2	18 kΩ
VCO gain	80 MHz/V	C_3	2.2 pF

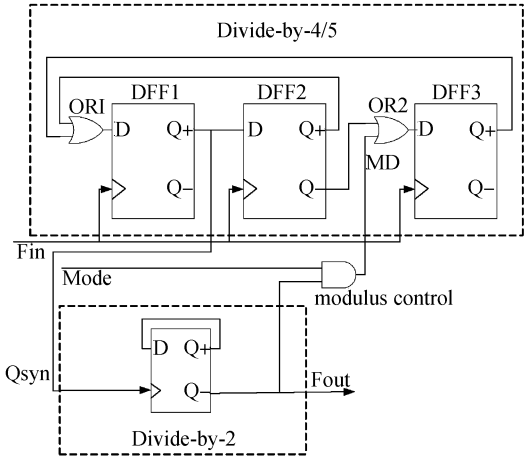

Fig. 3. Prescaler block diagram.

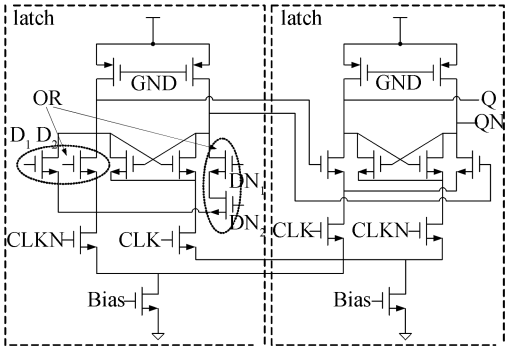

Fig. 4. Schematic of CML D flip-flop with merged OR gate.

ulus control signal of the synchronous divider (Ctrl), which is decided by the output signals of the divide-by-2 divider and the modulus control signal of the prescaler (MC). When the MC is high, during a divide-by-2 operation by the divide-by-2 divider, the Ctrl signal has one pulse, which makes the synchronous circuit divide by 5 for one time and results in a total divide ratio of 9.

The CML D flip-flop in Fig. 4 is composed of two D latches connected in a master/slave configuration. Each D latch contains a differential pair and a cross-coupled pair. The proposed D flip-flop is based on the dynamic flip-latch which uses different current sources between the differential pair and the cross-coupled pair. Compared to the conventional circuit, the proposed dynamic circuit can ameliorate the tradeoff between the operation frequency band and the output swing. The OR gate for modulus selection of the synchronous divider is merged into the D flip-flop to reduce the propagation delay and increase the maximum operating frequency as depicted in Fig. 4. The maximum operating frequency and power conupSigmaption of

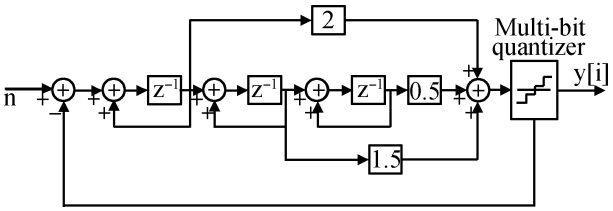

Fig. 5. Equivalent model of Σ–Δ modulator.

the flip-flop are determined by the transistor sizes, capacitive load and resistive load. The simulated differential pair to cross-coupled pair transistor size ratio for achieving the highest operating frequency is 6/5[7].

3.3. Σ–Δ modulator

We have employed an 18-bit third-order single-loop Σ–Δ modulator to produce a 2-bit output to control the multi-modulus divider (MMD) that consists of the divide-by-8/9 dual-modulus prescaler and the programmable pulse-swallow counter. Figure 5 shows the equivalent model of the modulator[8].The modulator consists of a single, third-order discrete time filter, feedforward and feedback coefficients. The value of the coefficients is derived from a third-order, high-pass Butterworth filter implementation. The cut-off frequency of the Butterworth filter is chosen to be sufficiently lower than half of the reference frequency, such that the coefficients are close to powers of two. The implemented filter has a cut-off frequency of 0.167 times that of the reference frequency, leading to the noise transfer function (NTF) of Eq. (5). To enable the integration of the digital filter in plain CMOS technology without implementing multipliers, the coefficients in the denominator are approximated such that the implemented feedback coefficients are power of two. The resulting NTF is given in Eq. (6), which is close to the Butterworth NTF, with preservation of the stability and causality conditions.

$$H_{\mathrm{qn}},\mathrm{b}(z)=\frac{(1-z^{-1})^3}{1-0.968z^{-1}+0.587z^{-2}-0.106z^{-3}}, \quad (5)$$

$$H_{\mathrm{qn}},\mathrm{b}(z)=\frac{(1-z^{-1})^3}{1-z^{-1}+0.5z^{-2}}. \quad (6)$$

3.4. Charge pump

Figure 6 shows the charge pump circuits. Basically, the charge pump is one of the most important blocks in the performance of the synthesizer. It is very important to match the up/down currents of the charge-pump. The phase noise and frequency spurious characteristic of the synthesizer is degraded

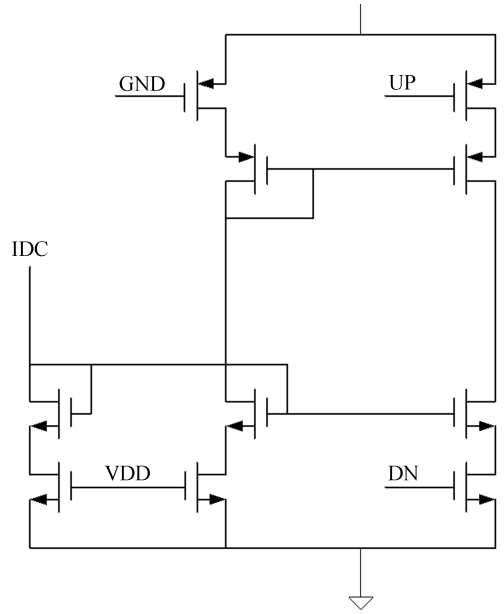

Fig. 6. Schematic of CP.

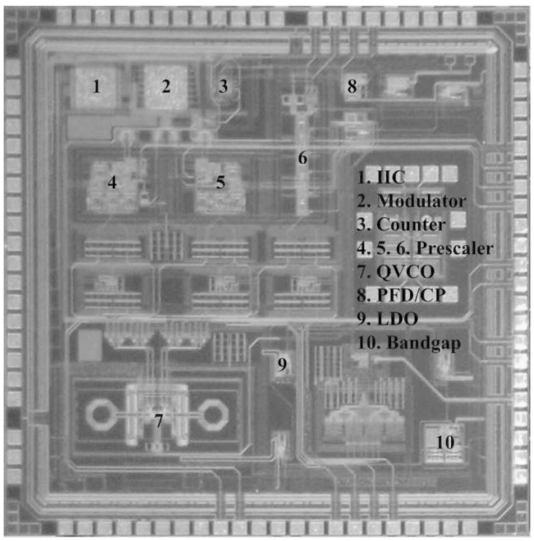

Fig. 7. Microphotograph of the frequency synthesizer.

due to up/down current mismatch. In addition, an ideal synthesizer does not suffer from unwanted charge injection in the loop filter when the loop is locked. In lock, both up and down current sources are off. By introducing the zero-dead-zone PFD, the additional delay in the PFD reset path turns both current sources on, even in lock, for an equal amount of time[8]. At the switching moments unwanted charge is injected, leading to high spurious tones at the reference frequency in the synthesizer output spectrum. To remedy this, several precautions are taken. First, as shown in Fig. 6, four symmetrical MOS are used to prevent charge injection from on-off MOS to the loop filter. Secondly, delay units that consist of NOT gates are used in the signal path to minimize the delay mismatch of up and down signals. Thirdly, layout is designed carefully to minimize the mismatch.

Table 2. Area and power of each block in frequency synthesizer.

Circuit blocks	Area (mm^2)	Power (mA)
QVCO	1×0.4	11
Divide-by-8/9 prescaler	0.35×0.3	5.2
PFD/CP	0.13×0.17	1
Synthesizer	2.1×1.6	21.2

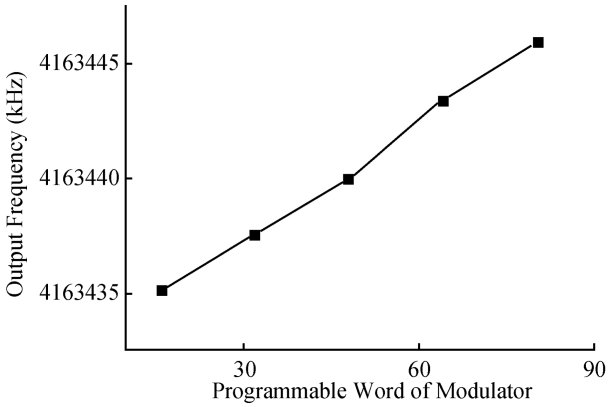

Fig. 8. Measured output frequency versus programmable word of modulator.

4. Measurement results

The fractional-N synthesizer was fabricated using the SMIC 0.18 μm 1P6M RF CMOS process. Each building block is encircled by a double guard ring to minimize the substrate noise. The VDD/GND separates five-groups which consist of the QVCO, output buffer, prescaler, charge pump and digital circuits. Electro static discharge (ESD) is also taken into consideration. Figure 7 is a chip microphotograph (including a DAC and an amplifier not used in synthesizer, and a divide-by-16/17 dual-modulus prescaler and a divide-by-8 prescaler for other requirements) that has key circuit blocks labeled. The chip has 86 pads due to the use of many pads for enhanced programmability. The area and power of each block and the whole synthesizer is listed in Table 2. The synthesizer utilizes a third-order loop filter, consisting of R1, C1, C2, R2 and C3 configured for a 145 kHz open-loop unity-gain bandwidth. All component values were calculated by hand. The 20 MHz reference used by the system is derived off-chip from a signal generator Tektronix AFG3252. The synthesizer is tested on a four-layer FR4 printed circuit board (PCB).

Measurement results show that the synthesizer output tuning range is from 3.74 to 4.44 GHz with a frequency resolution of 15 Hz. Universal/RF Counter Agilent 53131A has been employed to represent the output frequency while we change the 18-bit digital word of Σ–Δ modulator, as shown in Fig. 8.

The transient response of a 20 MHz frequency step was observed by adding the divider ratio by one and vice versa. Signal source analyzer Agilent E5052B has been employed to represent the transient response. The measured settling time was within 80 μs for a 20 MHz step in frequency. Figure 9 shows the measurement results.

Figure 10 shows the measured time-domain output waveforms of the two quadrature output by using the digital signal analyzer Agilent DSA91304A. Figure 11 shows the measured

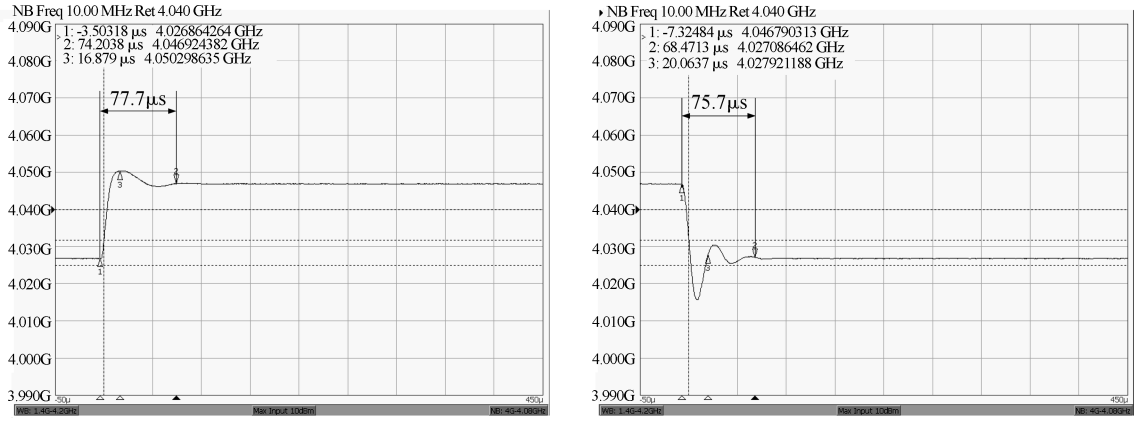

Fig. 9. Measured settling transient response.

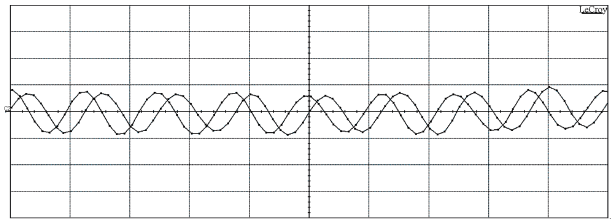

Fig. 10. Measured output waveforms of the I and Q channels (200 ps/div, 50 mV/div).

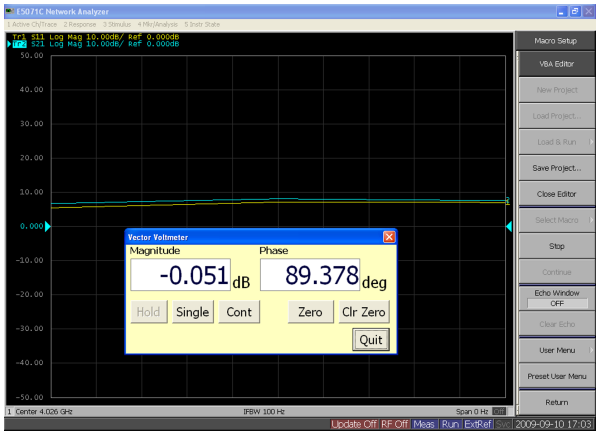

Fig. 11. Measured output amplitude and phase difference of the I and Q channels.

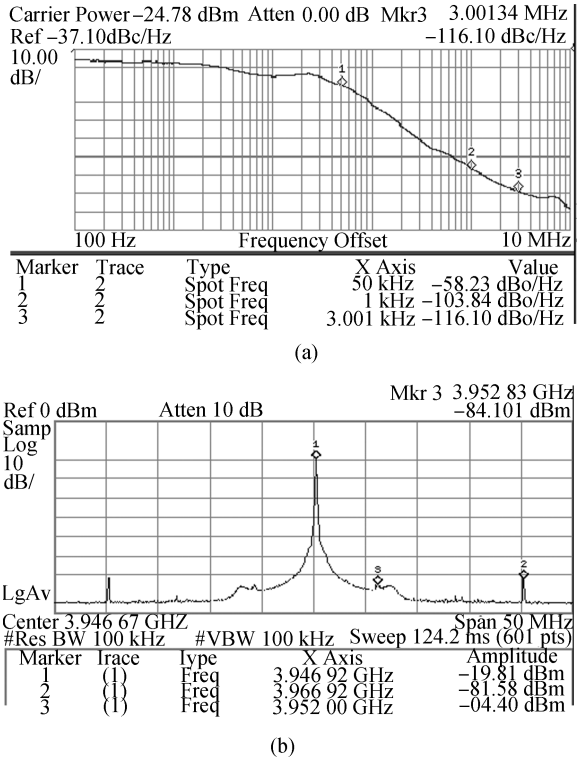

Fig. 12. (a) Measured phase noise performance. (b) Measured spur performance.

amplitude and phase difference of the two quadrature output by using network analyzer Agilent E5071C.

Figure 12(a) shows the measured noise performance of the fractional-N synthesizer. At low-frequency offsets below bandwidth, $1/f$ noise from the reference input and charge pump dominates. At frequency offsets above bandwidth, noise generated from QVCO dominates. Overall, we see that this prototype fractional-N synthesizer exhibits excellent phase noise performance (–116 dBc/Hz @ 3 MHz). Figure 13(b) shows the measured frequency spur performance of the fractional-N synthesizer. Reference spur at frequency offsets 20 MHz is –62 dBc. When the fractional part of the division ratio is 0.34375, the fractional spur at frequency offsets 6.875 MHz is –65 dBc. The measured performance of the synthesizer is upSigmamarized in Table 3. Table 4 compares with some other fractional synthesizers recently published in the literature.

Table 3. Summary of measurement results.

Parameter	Value
Locking range	3.74–4.44 GHz
Frequency resolution	15 Hz
Phase noise	< -116 dBc/Hz @ 3 MHz
Spur	< -60 dBc
Quadrature amplitude mismatch	< 0.1 dB
Quadrature phase error	$< 0.8°$
Settling time	< 80 μs
Power conupSigmaption	38.2 mW

Table 4. Comparison table.

Parameter	This work	Ref. [9]	Ref. [10]	Ref. [11]
Process	0.18 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Output frequency (GHz)	4	2.4	3.6	11
Phase noise (dBc/Hz)	–116 @ 3 MHz	–97 @ 1 MHz	–98 @ 100 kHz	–80 @ 1 MHz
Spur (dBc)	–60	–55	–45	–44
Core power conupSigmaption (mW)	38.2	49.5	110	94.5

5. Conclusion

In this paper, we have proposed a fractional-N frequency synthesizer that produces 3.74 to 4.44 GHz quadrature carriers for an IR-UWB transceiver. The synthesizer adopts an 18-bit third-order Σ–Δ modulator to achieve a 15 Hz frequency resolution and a fractional spur of less than –60 dBc. QVCO is employed to generate the quadrature local oscillator signals and enhance the quadrature accuracy. Measurement results show that the amplitude mismatch and phase error between I and Q signals are less than 0.1 dB and 0.8° respectively, and the performance of phase noise is less than –116 dBc/Hz @ 3 MHz. The settling time is within 80 μs. The core circuits conupSigmae only 21.2 mA from a 1.8 V supply.

References

[1] Xia Lingli, Li Weinan, Huang Yumei, et al. A 3–5 GHz amplitude and spectrum tunable impulse radio UWB transmitter. IEEE Asia Pacific Conference on Circuits and Systems, 2008: 160

[2] Zheng H, Luong H C. A 1.5 V 3.1 GHz–8 GHz CMOS synthesizer for 9-band MB-OFDM UWB transceivers. IEEE J Solid-State Circuits, 2007, 42(6): 1250

[3] Arora H, Klemmer N, Morizio J C, et al. Enhanced phase noise modeling of fractional-N frequency synthesizer. IEEE Trans Circuits Syst, 2005, 52(2): 379

[4] Lee J. A 3-to-8-GHz fast-hopping frequency synthesizer in 0.18-μm CMOS technology. IEEE J Solid-State Circuits, 2006, 41(3): 566

[5] Yuan Haiquan, Fu Zhongqian, Lin Fujiang, et al. A 4-GHz CMOS quadrature VCO with 20% tuning range for UWB system. Asia-Pacific Microwave Conference, 2008: 1

[6] Guo Shita, Huang Lu, Bai Xuefei. A 4-GHz CMOS dual-modulus prescaler with enhanced input sensitivity over extended operation range. IEEE International Conference on Communication Technology, 2008: 331

[7] Ding Y, Kenneth K O. A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS. IEEE J Solid-State Circuits, 2007, 42(6): 1240

[8] De Muer B, Steyaert M. CMOS fractional-N synthesizers. Kluwer Academic Publishers, 2003

[9] Shu Z, Lee K L, Leung B H. A 2.4-GHz ring-oscillator-based CMOS frequency synthesizer with a fractional divider dual-PLL architecture. IEEE J Solid-State Circuits, 2004, 39(3): 452

[10] Meninger S E, Perrott M H. A 1-MHz bandwidth 3.6-GHz 0.18-μm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise. IEEE J Solid-State Circuits, 2006, 41(4): 966

[11] Solomko V A. Weger P. 11 GHz CMOS Σ Δ frequency synthesizer. IEEE Electron Lett, 2006, 42(21): 1199