A 2.4 GHz power amplifier in 0.35 μm SiGe BiCMOS

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Abstract: This paper presents a 2.4 GHz power amplifier (PA) designed and implemented in 0.35 μm SiGe BiCMOS technology. Instead of chip grounding through PCB vias, a metal plate with a mesa connecting ground is designed to decrease the parasitics in the PCB, improving the stability and the gain of the circuit. In addition, a low-pass network for output matching is designed to improve the linearity and power capability. At 2.4 GHz, a P_{1dB} of 15.7 dBm has been measured, and the small signal gain is 27.6 dB with $S_{11} < -7$ dB and $S_{22} < -15$ dB.

Key words: 2.4 GHz; PA; SiGe BiCMOS; parasitics
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1. Introduction

SiGe BiCMOS has become an important contender for RF PA in recent years. SiGe HBTs have many attractive features, such as very high f_T and f_{max}, high current gain, and good substrate thermal conductivity[1−3]. Additionally, due to its full compatibility with the standard silicon process, SiGe BiCMOS technology enables IC designers to easily integrate PA with other modules to realize better chip performance and lower system costs[4]. However, SiGe/Si HBTs also have disadvantages: SiGe HBTs have relatively low breakdown voltages[5], which are detrimental to the gain, linearity, and dynamic range of the power amplifier. In addition, the substrate is very conductive, adding significant parasitics to both active and passive components of the power amplifier. These are adverse characteristics for circuit design.

A 2.4 GHz PA circuit is designed in 0.35 μm SiGe BiCMOS technology. However, this process technology is used for analog/mixed-signal applications without through-wafer via technology, and PA design work using it has not been found. In this paper, some circuit design methods are presented to resolve the problems caused by parasitics.

2. Circuit design

A kind of high breakdown voltage HBT is used with $BV_{ceo} = 9$ V. To achieve the desired output power and gain, a three-stage cascade configuration is designed. An RC feedback network is used in the first stage to obtain both linearity and stability. Base-ballasting resistors are used in all three stages. The emitter area of every HBT is 17.6 μm^2, and 40 HBTs are paralleled for the third stage to deliver the output power. The chip area is 1×1 mm^2. The topology of the whole circuit is shown in Fig. 1. The output match is implemented off-chip using high-Q surface mount devices (SMD) on PCB. The bonding wires and the microstrip lines serve as RF chokes in the first and second stages. Due to the process not using a through-wafer via, all grounding pads of the chip are connected with bonding wires.

Since the whole circuit includes on-chip and off-chip circuits, the on-chip circuit should be designed well before designing the off-chip circuit. In addition, the silicon substrate is conductive, so it is necessary to extract the parasitic resistors and capacitors.

For the on-chip circuit design, a fully integrated and ideally-grounded circuit is designed and simulated first. In this case, all components are selected from design-kits. Figure 2 shows the simulated results of the conditions before and after extracting parasitic resistors and capacitors. It can be found that S_{21} decreases by several dB after extraction, but the two S_{21} curves are similar. In addition, the matching does not change clearly from the S_{11} curve. In other words, the parasitics in the chip does not cause a clear deterioration in circuit performance.

In fact, the chip will be stuck on the PCB before testing, so the off-chip circuit should also be designed well. As shown in Fig. 3, all pads connecting to ground are bonded with two wires to decrease the negative feedback of grounded bonding wires. The parameters of the bonding wires such as span, height and spacing can be evaluated by simulation tools. In this case, the effect of PCB vias cannot be avoided because the chip connects the real ground through these vias, so it needs to calculate the inductor values from the PCB vias. The PCB type is FR4, and the board thickness is 0.5 mm. For a PCB via with a central aperture size of 10 mil, the via inductor can be calculated by the equation[6]: $L = 5.08h\,[\ln(4h/d) + 1]$ (nH), where h is the via length and d is the diameter of the central aperture in

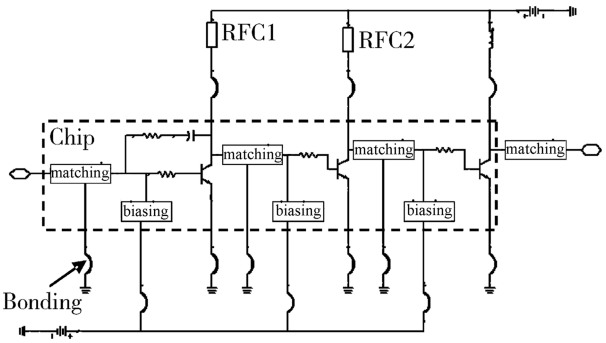

Fig. 1. Simplified schematic of a 2.4 GHz PA. The on-chip components are surrounded by a dashed line.

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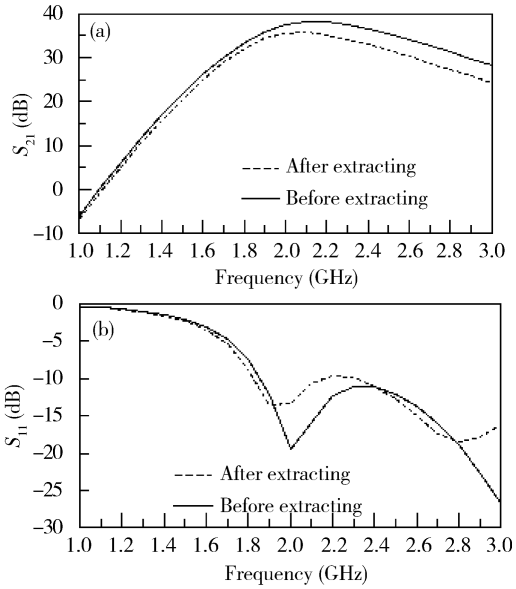

Fig. 2. Simulation result comparison between the conditions before and after extracting parasitics in fully integrated circumstances. (a) S_{21}. (b) S_{11}.

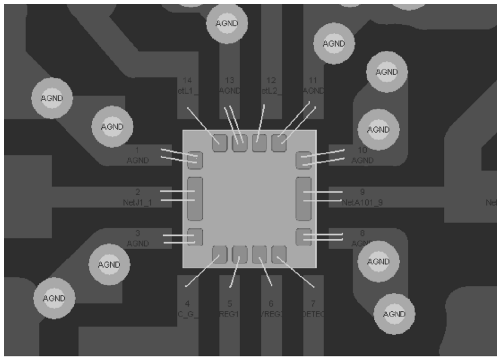

Fig. 3. Bonding wires of the chip stuck on the PCB.

inches; as a result, the parasitic inductor of one PCB via is about 0.3 nH.

Simulation results from a real testing environment are presented in Fig. 4 based on the matching in the schematic chip circuit. There is a big difference between the simulated results of conditions before and after extracting parasitics. S_{21} is about 30 dB before extraction and the curve is flat; however, there is an obvious raised point at 2.3 GHz after extracting parasitics, and positive values appear in the S_{11} curve. Accordingly, the circuit oscillates easily under these conditions.

From a comparison of Figs. 2 and 4, it can be seen that the off-chip circuit design on the PCB is critical. The components including the parasitics in the chip will interact with those in the PCB, the optimal matching frequency point would move and oscillation would happen easily in such circumstances. So it is important to optimize the design of the periphery circuit of the chip on the PCB.

The main factors outside the chip that would affect the circuit performance include: bonding wires, PCB vias, output matching network, PCB routing and filtering. The effect of the parasitic inductors from the PCB vias is the most important of

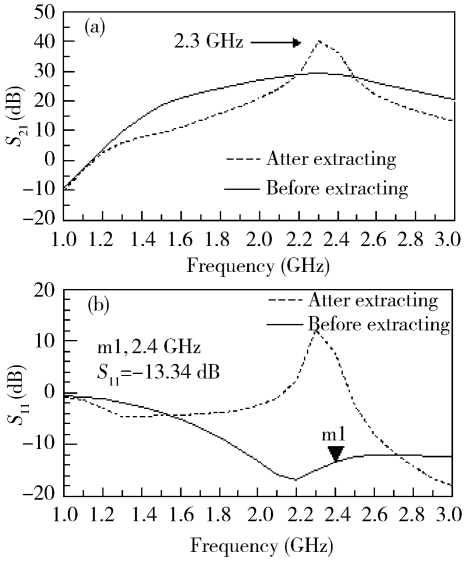

Fig. 4. Simulation result comparison between the conditions before and after extracting parasitics in a real testing environment. (a) S_{21}. (b) S_{11}.

these factors, because these via-inductors not only relate to the chip grounding but also grounding of the components in the matching networks on the PCB, thus the vias will cause negative feedback and change the matching. So the effect of the via-inductors should be decreased by all means. In addition, the output matching network is another important aspect, which determines the impedance matching and power delivering ability. From the above analysis, the optimization of the periphery circuit is focused on the PCB vias and output matching network.

3. Optimization of test components

3.1. Design of a metal plate with a mesa

In order to avoid the PCB vias, a kind of metal plate with a mesa is designed for connecting the chip grounding pads, and the area sticking the chip on the PCB is cut out. The mesa is smaller than the corresponding area on the PCB, so the metal plate can be embedded into the PCB through the mesa and they can be soldered together. The chip is stuck on the mesa, so the bonding wires can be bonded from the grounding pads on the chip to the mesa directly, avoiding grounded through the PCB vias. The mesa area is 1.6×1.6 mm^2 and easy to bond, as shown in Fig. 5(a), the height of the mesa is determined by the thicknesses of the PCB and the chip and, finally, the surfaces of the chip and the PCB should be roughly on the same level. So the via-inductors are avoided, and the effect of parasitics on the grounding path is decreased. It can be found from Fig. 5(b) that the peak on the S_{21} curve is eliminated, and the curve becomes flat. In addition, linear gain is increased by 3.5 dB at 2.4 GHz.

It is worth mentioning that bonding wires start at the grounding pads along the side of the chip and arrive at the metal mesa, which could shorten the length of the wires compared with the usual bonding wires, as shown in Fig. 6. In this case, the shape and length of the bonding wires could be controlled

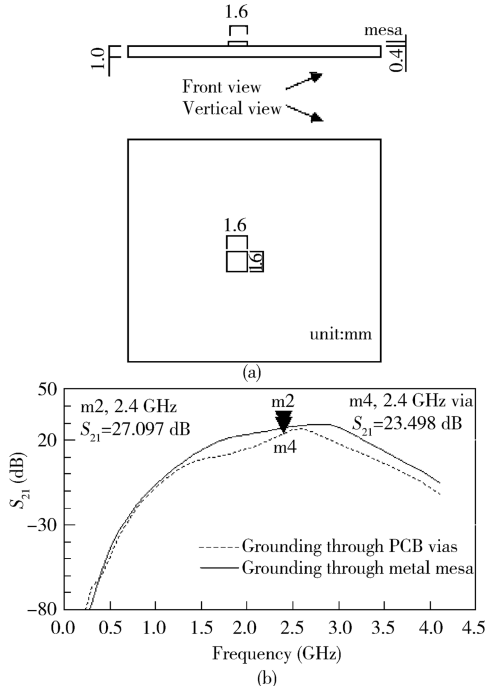

Fig. 5. Design of the metal plate with a mesa and the improvement of simulation results. (a) Metal plate with a mesa. (b) S_{21} in two types of grounding.

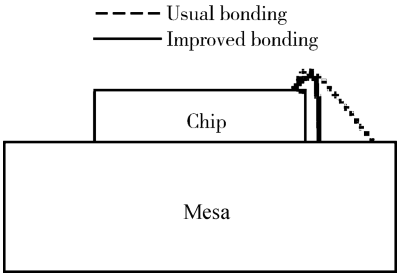

Fig. 6. Improved bonding for grounding wires.

well and kept coherent.

3.2. Design of output matching circuit

SMD components such as capacitors and inductors are selected from Johanson 0402, whose models can be found in simulation. For the output matching circuit,as shown in Fig. 7, two types of networks are designed, and the corresponding simulation results are shown in Fig. 8. It can be found that the matching of the first circuit type is better than the second one, and its S_{22} is about −16 dB; however, the output power at the −1 dB compression point and the second harmonic suppression of the first circuit type are worse than those of the second, as shown in Fig. 9. In fact, the second type is a low-pass matching network, which could compress the harmonics, and the second harmonic compression is below −47 dBc from the simulation results, which increases the linearity of the circuit. Finally, the second type of output matching network is selected and optimized, and L1 is replaced by a microstrip line on the PCB.

The above are the main measures used in the optimization of the periphery circuit on the PCB. In addition, the RF choke in every stage is also designed and optimized, and the RF chokes

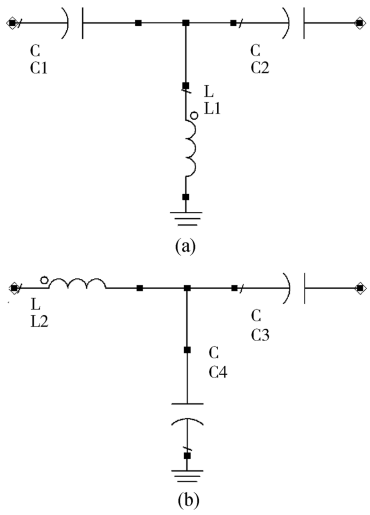

Fig. 7. Two types of output matching network. (a) The first type. (b) The second type.

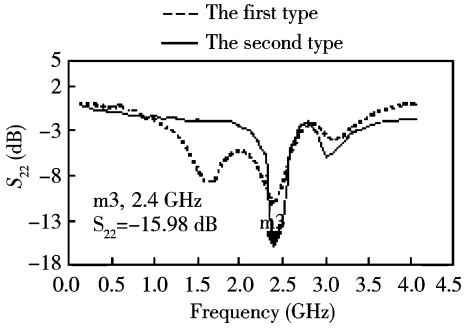

Fig. 8. S_{22} simulation of two types of output matching circuits.

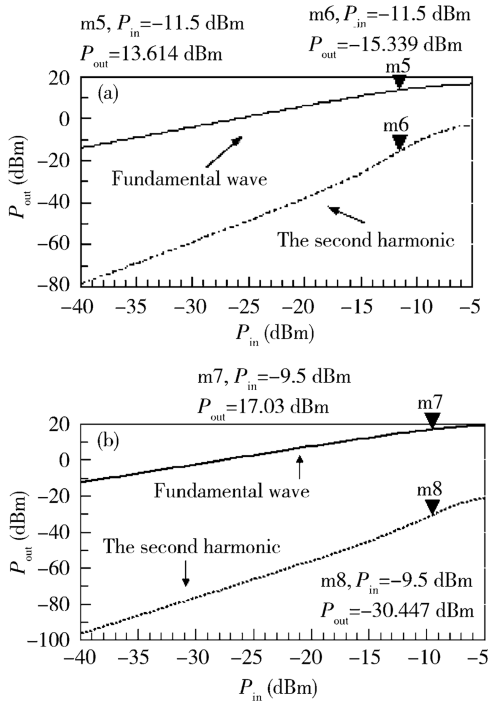

Fig. 9. Simulation of output power in two types of output matching. (a) The first type. (b) The second type.

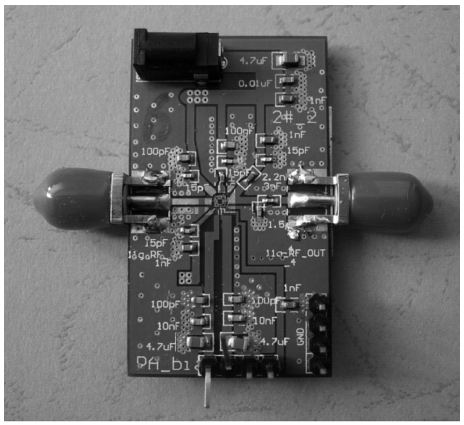

Fig. 10. Test component.

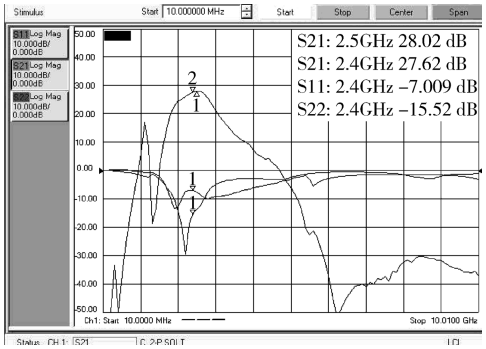

Fig. 11. Measured S parameters.

in the first and second stages are implemented with microstrip lines on the PCB and bonding wires after optimization.

4. Measured results

The test component is shown in Fig. 10. Multiple different capacitors are placed in every DC path for filtering. Under 3.3 V power supply, the total current consumption is 115 mA. With a vector network analyzer Agilent E8363B, a linear gain of 27.6 dB at 2.4 GHz is measured, and S_{11} and S_{22} are below -7 dB and -15 dB respectively, as shown in Fig. 11. Figure 12 shows that the measured output power at the -1 dB compression point is 15.7 dBm, and the saturated power is 20 dBm.

5. Conclusion

A 2.4 GHz PA circuit is designed and implemented in

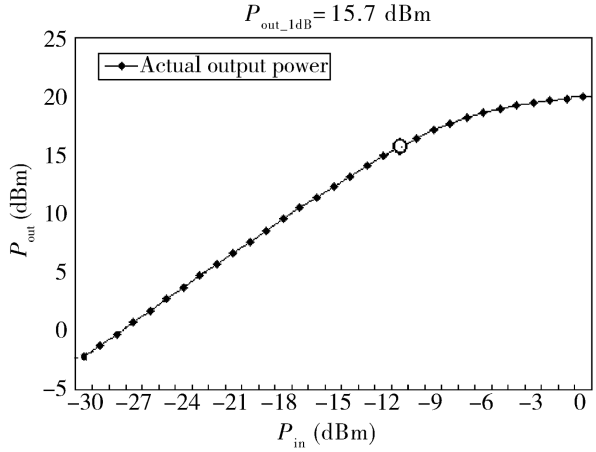

Fig. 12. Measured $P_{\rm out}$ at the –1 dB compression point.

0.35 μm SiGe BiCMOS technology. In order to decrease the parasitics of chip grounding, and especially the effect of the PCB vias, a metal plate with a mesa for chip grounding is designed, improving the circuit gain and matching. In addition, the output matching network on the PCB is optimized and improves the linearity of the circuit. The measured results obtained from this PA show a linear gain of 27.6 dB with $S_{11} < -7$ dB and $S_{22} < -15$ dB, a $P_{\rm 1dB}$ of 15.7 dBm at 2.4 GHz.

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