A high-performance, low-power ΣΔ ADC for digital audio applications

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Abstract: A high-performance low-power ΣΔ analog-to-digital converter (ADC) for digital audio applications is described. It consists of a 2-1 cascaded ΣΔ modulator and a decimation filter. Various design optimizations are implemented in the system design, circuit implementation and layout design, including a high-overload-level coefficient-optimized modulator architecture, a power-efficient class A/AB operational transconductance amplifier, as well as a multi-stage decimation filter conserving area and power consumption. The ADC is implemented in the SMIC 0.18-μm CMOS mixed-signal process. The experimental chip achieves a peak signal-to-noise-plus-distortion ratio of 90 dB and a dynamic range of 94 dB over 22.05-kHz audio band and occupies 2.1 mm^2, which dissipates only 2.1 mA quiescent current in the analog circuits.

Key words: ΣΔ modulator; decimation filter; low power; audio analog-to-digital converter
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1. Introduction

Professional audio systems require analog-to-digital converters (ADCs) with high resolution and linearity. ΣΔ modulation provides an efficient method of signal conversion to achieve high resolution without the need for high-accuracy analog building blocks[1,2]. By combining oversampling and feedback to shape the noise, and then using a digital filter to attenuate the noise that has been pushed out-of-band, it is possible to achieve a dynamic range of above 90 dB. Moreover, oversampling architectures transfer much of the signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage[3−6].

This paper presents a high-performance low-power ΣΔ ADC for high-end digital audio applications. It consists of a 2-1 cascaded ΣΔ modulator and a decimation filter. The performance and power consumption of the converter is optimized by taking care of system design issues and circuit implementation techniques, as well as layout arrangement.

2. Modulator design

2.1. Modulator architecture

To achieve an overall dynamic range of above 90 dB, a 3-order modulator with an oversampling ratio of 128 is adopted. A cascaded architecture is chosen primarily for two reasons. First, cascading first- and second-order modulators eliminate the stability problems associated with higher order single-loop modulators, thus a higher input overload level and a larger dynamic range are approached. Second, baseband spectral tones are largely suppressed in cascaded modulators, which is desirable in high-end audio applications. The 2-1 cascaded architecture is preferable to alternative cascaded third-order architectures because it is less sensitive to component mismatch[7,8]. Figure 1 shows a block diagram of the modulator.

Simulation and analytical modeling of the 2-1 cascaded architecture indicate that for different coefficients of b, β and λ, there is a tradeoff between quantization noise and the input level at which the modulator overloads. Another consideration in choosing the coefficients is to avoid the presence of spurious tones and signal dependence in the noise floor. Traditionally, the feedback coefficient b is chosen to be 2, but when $b = 2$, strong tones appear near the zero input level, where they can be especially objectionable since the signal power is low. A value of $b = 2.5$ can be used to reduce the spectral tones in the first stage of the modulator. Figure 2 shows that the modulator appears to be free of spectrum tones at low level inputs when $b = 2.5$. A high overload level of -1.3 dB is achieved when $\beta = 0.25$ and $\lambda = 1$, and the case of $\beta = 0.25$ and $\lambda = 1$ results in a quantization noise floor that is very nearly independent of signal power, as shown in Fig. 3. Therefore, the coefficient combination of $b = 2.5$, $\beta = 0.25$ and $\lambda = 1$ achieves both a high overload level and excellent spectral pu-

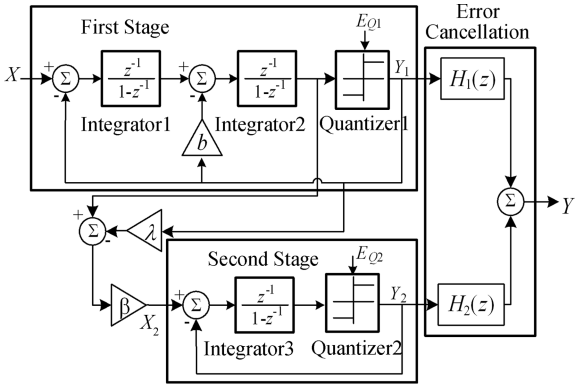

Fig. 1. Block diagram of a 2-1 cascaded modulator.

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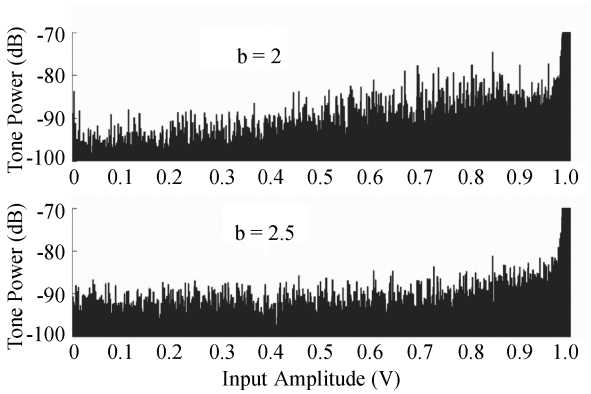

Fig. 2. Spectrum tones in the first stage.

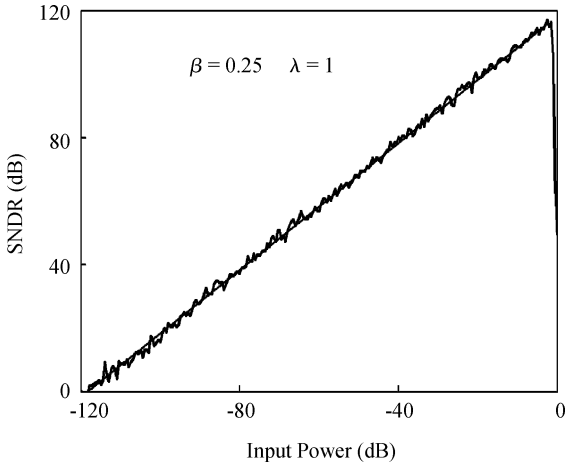

Fig. 3. SNDR versus input power.

rity. In addition, the signal swings throughout the modulator should be scaled to avoid saturating the integrators. Figure 4 shows the probability density functions of the integrator outputs for the modulator in this paper.

2.2. Circuit topology

The modulator is implemented with switched-capacitor (SC) circuits. Figure 5 shows the circuit topology for the first stage of the modulator, and all the building blocks are designed in a 0.18 μm CMOS mixed-signal process. Capacitors CB1 and CB2 ensure that the disturbances through lead frame, pins, and bond wires onto one of the two differential input lines appear on the other line as well and hence become a common-mode input to the modulator.

The switches are controlled by two-phase, non-overlapping clocks, p1 and p2, advanced falling edge clocks, p1a and p2a, and a complement of p2a, p2ab, in which p1a and p2a are designed to suppress the signal-dependent channel charge injection, and p2ab is used for the control clock of the comparator to avoid adverse effects due to signal delay. A bootstrapped switch[9, 10] is adopted in front of the modulator to considerably enhance the linearity of input sampling that directly limits the overall performance.

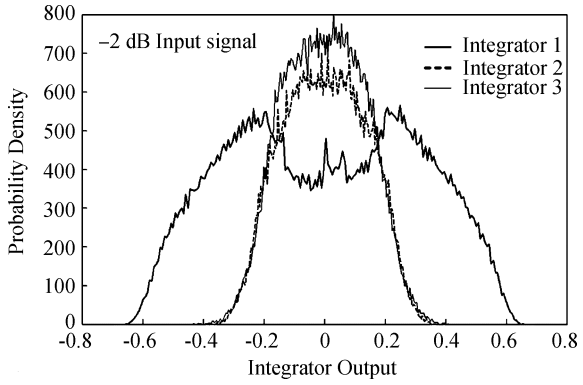

Fig. 4. Probability density functions of integrator outputs.

2.3. Modulator performance

To realize a high-performance modulator, the issues of implementation nonidealities, including capacitor mismatch, integrator leak and circuit noise, are explored.

Capacitor mismatch easily deteriorates the baseband quantization noise of a 2-1 cascaded modulator. For an ideal cascaded modulator, the quantization noise of the preceding stages is re-modulated in the succeeding stages, and lastly removed by digital error cancellation. The capacitor ratio error leads to the presence of mismatch between integrator coefficients and their digital counterparts in error cancellation. According to theoretical calculation, to limit the increase of quantization noise to less than 1 dB as compared to the perfectly matched situation, the maximum capacitor-mismatch error allowed is shown in Fig. 6.

With an oversampling ratio of 128, the proposed 2-1 cascaded modulator requires a mismatch error less than 4.2%. In the SMIC 0.18 μm CMOS mixed-signal process, the 3 σ fractional standard deviation for 0.1 pF metal-insulator-metal (MIM) capacitors is less than 1%. Therefore, the 0.1 pF MIM capacitor acts as the minimum unit cell in this design.

Integrator leak, which is a consequence of finite amplifier DC-gain, changes the transfer function of SC integrators, thereby limiting the extent to which low-frequency quantization noise is shaped in a modulator[11]. If a 2-1 cascaded architecture is adopted with an oversampling ratio of 128, in order to limit the loss of dynamic range due to integrator leak to less than 1dB beyond that obtained with ideal integrators, the required DC-gain of the OTA in the first stage is calculated to be above 60 dB, as shown in Fig. 6. The requirement of the OTA in the second stage is relaxed owing to the noise-shaping property of the modulator. The above conclusion is helpful for our OTA design.

Circuit noise, including thermal and flicker noise, is also an important nonideality in a well-designed modulator. Thermal noise is mainly from the OTA and sampling switches in the first integrator, and the amplifier and sampling noise powers are usually at the same order. To achieve the sampling noise power of less than 106 dB, the sampling capacitor value in the first integrator must be more than 2.6 pF. In this work, a 4.8 pF sampling capacitor is chosen in order to provide adequate suppression of sampling noise. In addition to thermal noise, flicker noise can result in a significant noise component when referred

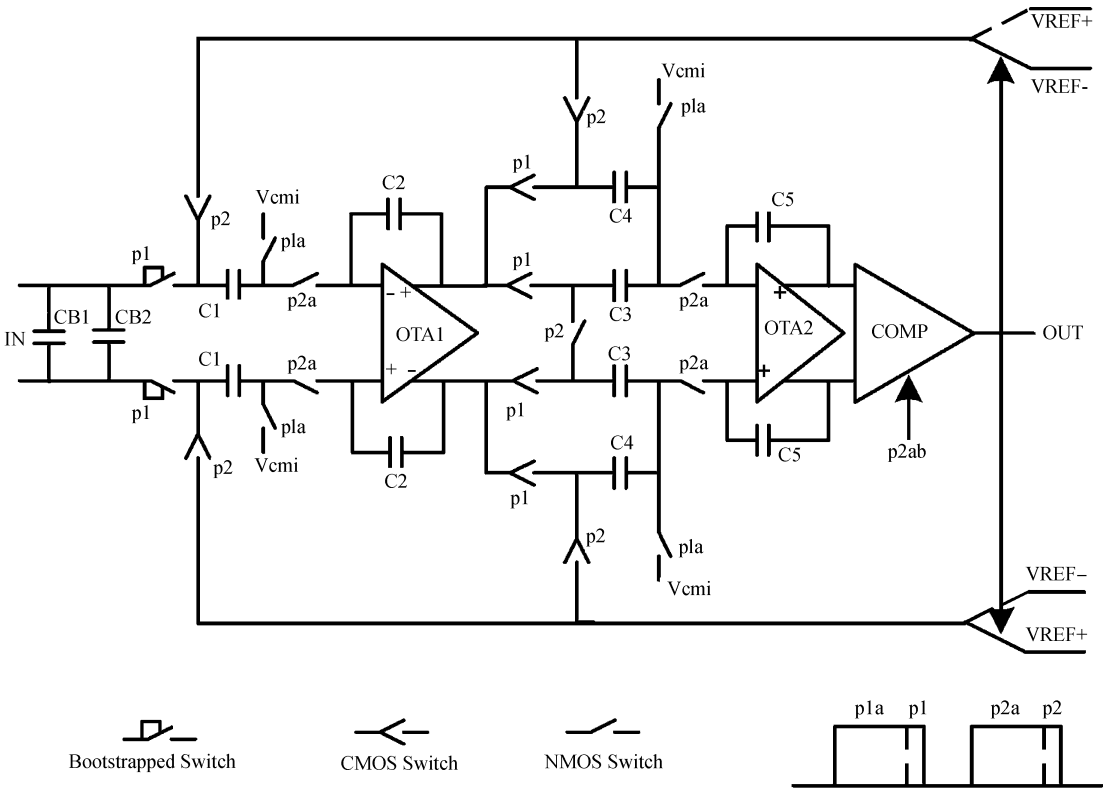

Fig. 5. First stage of the 2-1 cascaded modulator.

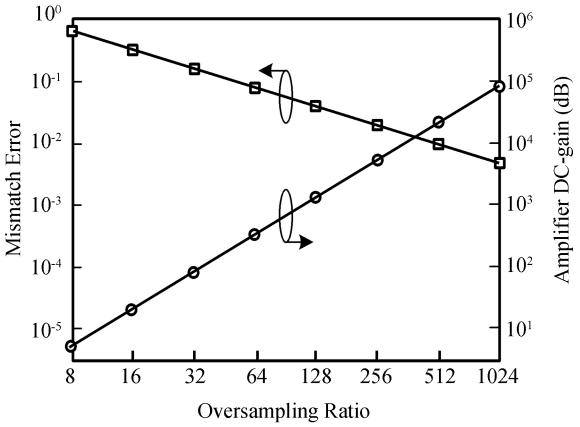

Fig. 6. Required mismatch error and amplifier DC-gain to yield a 1-dB reduction in dynamic range.

to the amplifier input in audio applications. Therefore, the size of transistors that contribute significantly to flicker noise is increased in our design without excessive degradation of the settling performance.

2.4. OTA

The OTA used in the integrators is the most critical building block with most of the power consumption, especially in cascaded modulators. Figure 6(a) shows the details of the designed two-stage class A/AB OTA. It includes a class A/AB output stage wherein push-pull operation is implemented through the use of current mirrors. Because of the push-pull operation, the slew rate of the proposed OTA is doubled as compared to a conventional folded-cascade OTA with the same tail current. As a result, the slew-rate requirement can be satisfied by the proposed OTA with a significantly reduced power consumption. A large current gain (n : 1) in the current mirrors also contributes to the enhancement of the slew rate, as well as direct-current (DC) gain, but the mirror pole is lowered, which will eventually degrade the phase margin of the circuit. A current gain of 1.6 ($n = 1.6$) is used in this design. With diode-connected NMOS devices M3 and M4, the first stage has an inherent common-mode-feedback (CMFB). A simple CMFB circuit is used for the second stage of the amplifier, as shown in Fig. 6(b).

Under the worst temperature and process corner conditions, the proposed OTA in the first integrator achieves 113-V/μs slew rate, 76.5-dB DC gain, 72.2-MHz bandwidth, 69.6° phase margin with 9.6-μV inband input-referred noise, consuming only 0.8 mA quiescent current. Total power dissipation is 2.6 mW from a 3.3 V supply. The OTAs in the second and third integrators are scaled versions of the first OTA. Due to the relaxed requirements of DC gain, bandwidth and capacitor load, the OTAs in the second and third integrators dissipate 1.5 and 0.8 mW, respectively.

3. Decimator design

Decimation is an important component of oversampled analog-to-digital conversion. It transforms the digitally modulated signal from short words occurring at a high sampling rate to longer words at the Nyquist rate while suppressing much of the high frequency quantization noise. In this design, a multi-

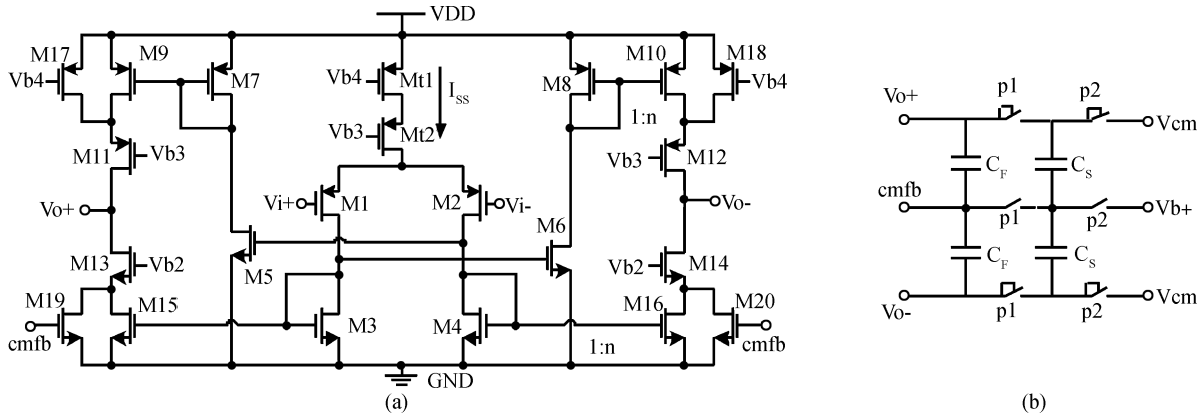

Fig. 7. (a) Two-stage class A/AB OTA. (b) CMFB circuit.

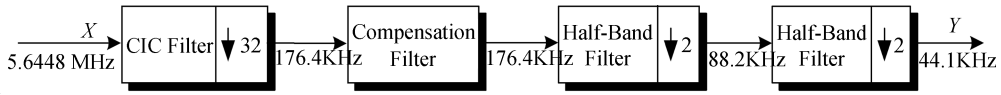

Fig. 8. Block diagram of decimation filter.

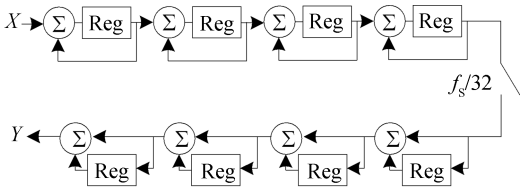

Fig. 9. CIC filter architecture.

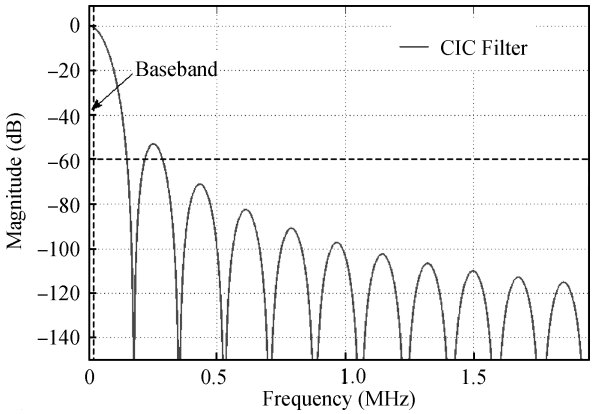

Fig. 10. CIC filter frequency response.

stage decimation filter[12] with a downsampling ratio of 128 is presented.

3.1. Decimation filter architecture

The decimate-by-128 filter is required to have greater than 90 dB stop-band attenuation and less than 0.01 dB passband ripple. The passband of the decimation filter lies between 0–0.453 f_w, and the stopband starts from 0.5 f_w, where f_w is the output word rate. The proposed decimation filter is composed of several stages: the first stage is a 4-order cascaded-integrated-comb (CIC) filter, followed by a finite impulse response (FIR) compensation filter, and the latter stages are several cascaded halfband filters. The multi-stage design offers significant savings in computation and storage requirements over a single-stage design, thus the area and power consumption are reduced. The block diagram of the proposed decimation filter is described in Fig. 8.

3.2. Decimation filter implementation

A front-end 4-order CIC filter with a downsampling ratio of 32 is depicted in Fig. 9. The CIC filter is implemented with four cascaded integrators, which operate at 5.6448 MHz, followed by resampling processing and four cascaded differentiators operating at 176.4 kHz. Such an architecture features both minimal data storage and straightforward decimation ratio programmability and avoids the need for multipliers. Moreover, because the differentiator unit is placed after the downsampling, the amount of hardware operating at the high sampling rate is kept to a minimum, thereby conserving power. The frequency response of the proposed CIC filter is shown as Fig. 10.

A 11-order FIR compensation filter, operating at the 176.4 kHz output rate, is used to compensate the droop at the passband edge introduced by the CIC filter. The droop-correction filter does not perform a sampling rate reduction and has non-zero odd coefficients. As shown in Fig. 11, the passband ripple of an original CIC filter is up to 0.86 dB, while the compensated CIC filter achieves only 0.00023 dB passband ripple.

Two cascaded halfband filters accomplish the remaining sampling rate reduction to the Nyquist output rate of 44.1 kHz, and filter out out-of-band noise efficiently. Halfband filters are a subset of symmetric FIR filters. All of their odd coefficients are equal to zero except for the center one, which is equal to 1/2[13], thereby reducing their computational complexity by nearly 50% as compared to general direct-form filter architecture. This results in fewer taps, less hardware, and lower power. The two halfband filters are both implemented using the polyphase structure, although more coefficients and delay

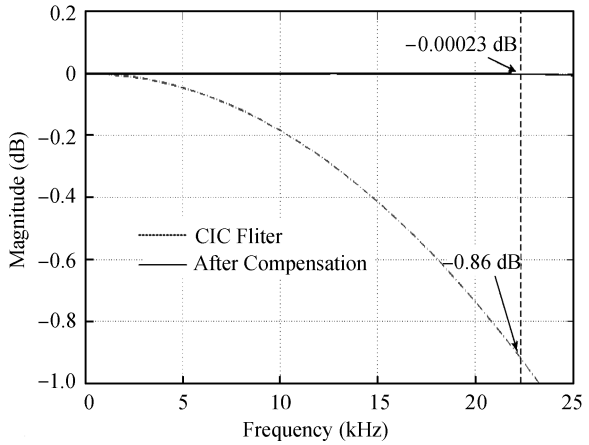

Fig. 11. Original, compensated CIC filter passband ripple.

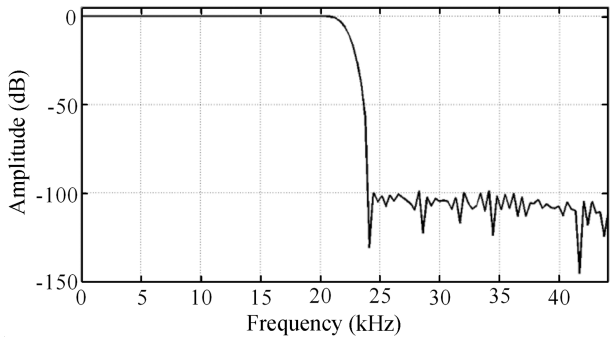

Fig. 12. Decimator frequency response.

terms are required in the second halfband filter. The coefficients of the halfband filters are implemented using the canonic signed digit (CSD) number system with shifters and adders. Based on the optimized CSD code, the realization cost and power consumption can be further reduced. The numbers of the two halfband filter taps are 22 and 130, respectively.

The frequency response of the overall decimator is shown in Fig. 12. The proposed decimate-by-128 filter achieves greater than 95 dB stop-band attenuation and less than 0.001 dB passband ripple.

4. Layout design

Figure 13 is a micrograph of the proposed ADC chip, which occupies an area of 2.1 mm^2 and integrates an analog $\Sigma\Delta$ modulator and a digital decimation filter. The analog circuitry uses a 3.3-V power supply, while the digital part operates at 1.8 V. For layout design, the crosstalk issue between the digital and analog signal should be fully considered. A physical distance of 100 μm is left between the digital filter and the analog modulator, and an independent-grounded P+ guard ring is added around the entire $\Sigma\Delta$ modulator. Inside the modulator, an independent power is supplied for noise-sensitive components, such as current reference and OTAs, so the noise, generated by clock circuits, switches and comparators, will not be coupled to the noise-sensitive part directly through power line. In addition, the clock signals are routed along the edge of the analog modulator to minimize their interference effects in internal

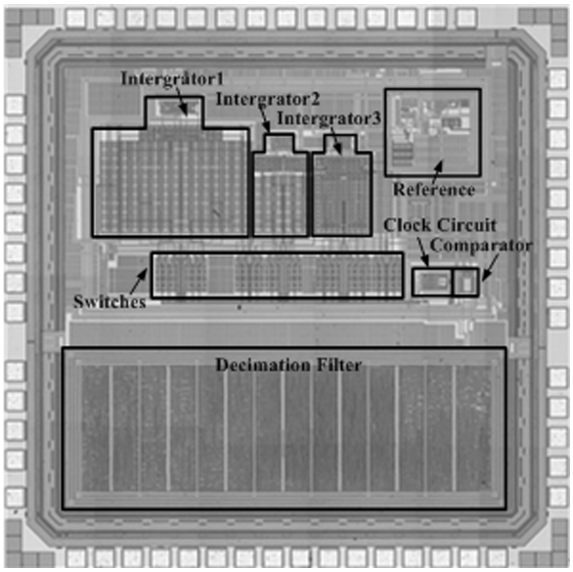

Fig. 13. Micrograph of the ADC.

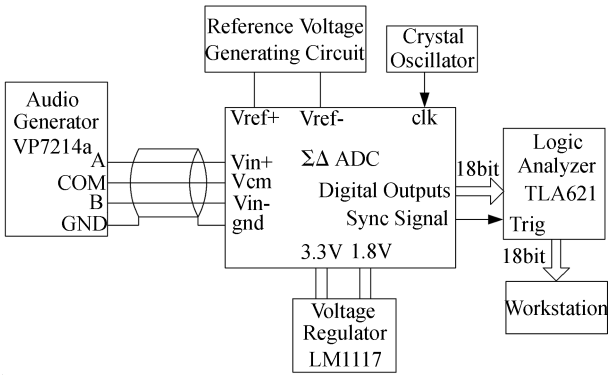

Fig. 14. Experimental test setup.

analog modules.

5. Experimental results

The $\Sigma\Delta$ ADC described is fabricated in a 0.18 μm CMOS mixed-signal process. Figure 14 depicts the test setup used in this work.

The input to the experimental ADC chip is provided by a low-distortion audio signal generator VP7214a. The output of the sinewave generator is firstly driven by voltage buffers, and then connected with a one-pole low pass anti-aliasing filter. This filter also attenuates charge kickback from the sampling switches in the ADC chip to the source. A 6 MHz crystal oscillator is adopted for the clock signal, and the power supplies are generated by high efficiency linear regulators LM1117. Because the noise introduced by the reference voltage will be superimposed on the input signal directly, the positive and negative phase reference voltage $V_{\text{ref+}}$ and $V_{\text{ref–}}$ are set by a low-noise voltage regulator LM723 (providing 6 V) and two 2-kΩ potentiometers. In order to further filter out the noise in different frequency bands, the output reference voltages are bypassed with a parallel combination of 10-μF, 1-μF, 0.1-μF and 0.01-μF capacitors. A logic analyzer TLA621 acquires the

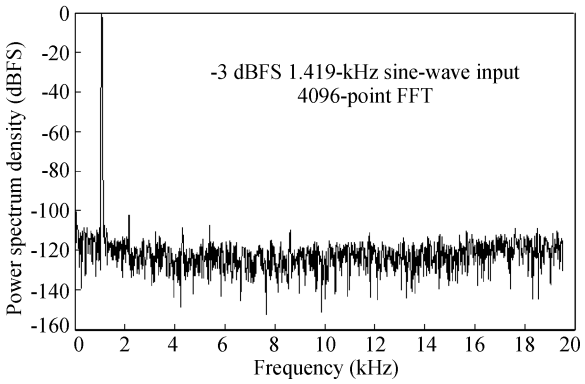

Fig. 15. Output spectrum of the ADC.

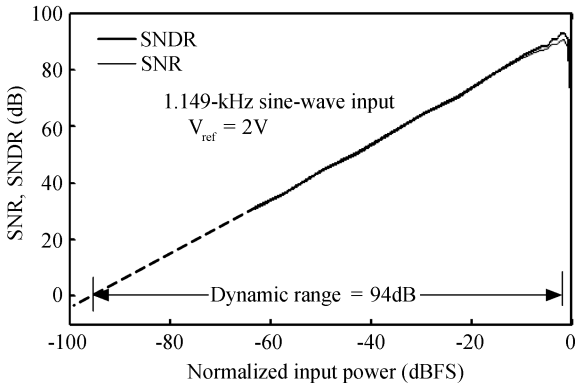

Fig. 16. Measured SNR and SNDR versus input signal power.

multi-bit digital output of the ADC chip, then transfers the data to a workstation for off-chip processing using MATLAB[2].

A 4096-point FFT of the output spectrum for a −3 dBFS, 1.419-kHz sinusoidal input is shown in Fig. 14. The spectrum demonstrates a very flat noise floor free of spectrum tones, which implies that the performance of the ADC is thermal noise limited. The measured SNR and SNDR versus the relative input amplitude are shown in Fig. 15. An input level of 0 dBFS corresponds to a sinusoidal input whose peak-to-peak differential voltage is 4 V.

Because of the limitation of the signal generator VP7214a, the SNDR is obtained through curve extension when the input power is lower than −63 dBFS. A 90-dB peak-SNDR and 93-dB peak-SNR are achieved when the amplitude of the input signal is −1.8 dBFS. The overload level is −1.1 dBFS and hence the dynamic range of the ADC is 94 dB. The total power consumption of the ADC is 15.9 mW, in which the analog $\Sigma\Delta$ modulator only draws 2.1 mA current from a 3.3 V supply.

Over a temperature range of 0–90 °C, the peak-SNDR specification of the experimental ADC changes less than 1.5 dB, which displays a strong robustness, as shown in Fig. 17.

The measured performance of the ADC is summarized in Table 1.

As reported domestic counterparts[14−16] are mostly modulators, a comparison of modulator performance is listed in Table 2. The proposed modulator achieves a much higher SNDR and more competitive figure-of-merit (FOM, $\mathrm{FOM} = \frac{\mathrm{Power}}{2^{(\mathrm{SNDR}-1.76)/6.02} \times 2 \times \mathrm{BW}}$) compared with other published modulators.

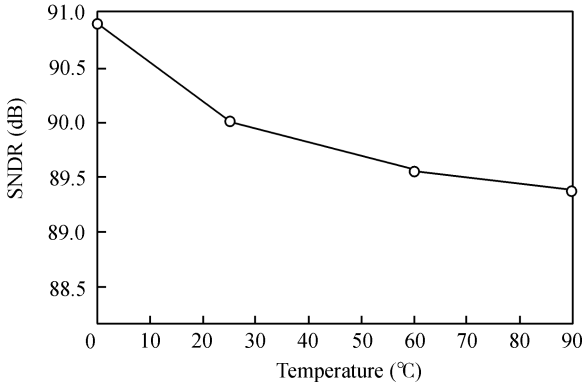

Fig. 17. Peak-SNDR versus temperature.

Table 1. ADC performance summary.

Specification	Value
Power supply	Analog: 3.3 V, Digital: 1.8 V
Oversampling ratio	128
Bandwidth	22.05 kHz
Sampling rate	5.6446 MHz
Power dissipation	Analog: 6.9 mW, Digital: 9 mW
Peak SNDR	90 dB
Peak SNR	93 dB
Dynamic range	94d B
Area	2.1 mm^2
Technology	0.18-μm CMOS

Table 2. Modulator performance comparison.

	Ref. [14]	Ref. [15]	Ref. [16]	This work
Technology (μm)	0.5	0.6	0.18	0.18
Supply (V) / Power (mW)	5 /–	5 / 15	1.8 / 16.7	3.3 / 6.9
Bandwidth (kHz)	21.8	200	250	22.05
SNDR (dB)	80	72	73	91
FOM (pJ/step)	–	11.5	9.1	5.4

6. Conclusion

The implementation of a high performance, low-power $\Sigma\Delta$ ADC has been described. The converter, fabricated in SMIC 0.18 μm CMOS technology, integrates an analog modulator and a digital decimator in a single chip. Top-down design optimizations, from system level to layout level, are implemented to extend the dynamic range, suppress quantization noise and harmonic distortion and reduce power dissipation. The audio ADC prototype achieves 90-dB peak-SNDR and 94-dB DR with a power consumption of 15.9 mW, which is suitable for high-end digital audio applications.

Acknowledgement

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