Design and implementation of a high precision and wide range adjustable LED drive controller*

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Abstract: This paper presents a novel high precision and wide range adjustable LED constant-current drive controller design. Compared with the traditional technique, the conventional mirror resistance is substituted by a MOSFET with fixed drain voltage, and a negative feedback amplifier is used to keep all mirror device voltages equal, so that the output current is precise and not affected by the load supply voltage. In addition, the electric property of the mirror MOSFET is optimized by a current subsection mirror (CSM) mechanism, thus ensuring a wide range of output current with high accuracy. A three-channel LED driver chip based on this project is designed and fabricated in the TSMC 0.6 μm BCD process with a die area of 1.1×0.7 mm^2. Experimental results show that the proposed LED drive controller works well, and, as expected, the output current can be maintained from 5 to 60 mA. A relative current accuracy error of less than 1% and a maximal relative current matching error of 1.5% are successfully achieved.

Key words: CSM mechanism; BCD process; LED drive controller
DOI: 10.1088/1674-4926/31/2/025010 **EEACC:** 2570A

1. Introduction

LEDs have wide applications in display, LCD backlighting, and automotive lighting because of their small size, low power consumption, superior longevity and improved luminance[1]. As a result of LED power level restriction, drive controller circuits are required to light multiple LEDs for enough power, and can be divided into constant-current drive controllers and constant-voltage drive controllers[2]. Any change in LED forward voltage creates a large change in LED current which is directly related to brightness, so the constant-current drive controller becomes the preferred method of driving the LED rather than the constant-voltage drive controller, to eliminate changes in current due to variations in forward voltage. Currently, two control technologies are widely used for the constant-current drive controller: linear regulated control technology[3] and switch-mode control technology[4]. The linear regulated control has low cost, low noise, a fast transient response to load and can be realized simply, but has low efficiency and low power levels. The switch-mode control has high power levels and high efficiency (i.e., the PWM control can reach more than 90%), but has a slow response to load and produces high level of EMI. So we can choose one of them for the constant-current drive controller to meet different demands. However, constant-current drive controllers with the above technologies both have the same drawbacks in applications. On the one hand, most constant-current drive controllers are not very accurate, which would produce errors in the brightness between different modules. The human eye can distinguish a brightness difference of more than 6%, and at low screen brightnesses can even distinguish a 1% difference in brightness. For example, when multi-channel LED drivers provide the backlight for the LCD, the current differences would lead to uneven backlight, and the LCD screen brightness is intertwined[5]. On the other hand, more and more applications require LED-driven current that can be adjusted to a certain extent; the wider the current range, the better. In fact, these two properties always restrict each other so that the wider current range will be due to the lower accuracy. Therefore, improving the current precision at the same time as realizing a wide range of current regulation has become one of the most important topics in LED-driven design.

In this paper, the basic principles of a traditional LED constant-current drive controller and the causes of imprecision are analyzed. Then a new high precision drive technology based on linear and negative feedback theories is presented to minimize current accuracy error. Additionally, a novel image mechanism called a current subsection mirror (CSM) is proposed which can broaden the output current range with high accuracy. Finally, a three-channel LED driver IC is designed whose range is 5–60 mA, which can be adjusted accurately through an external resistor.

2. Traditional LED constant-current drive controller

The traditional LED constant-current drive controller is shown in Fig. 1. Amp op_1 and FET M0 constitute a feedback loop; V_1 will be equal to V_{ref} so long as the gain of amp op_1 is large enough. We have:

$$I_1 = \frac{V_1}{R_{\mathrm{e}}} = \frac{V_{\mathrm{ref}}}{R_{\mathrm{e}}}, \tag{1}$$

where V_{ref} is a bandgap voltage[6], and R_{e} is an external resistor.

* Project supported by the National Ministry Pre-Research Foundation of China (No. 9140A08010208DZ0123) and the Applied Materials Innovation Foundation of Xi'an, China (No. XA-AM-200817).
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Received 17 July 2009, revised manuscript received 21 October 2009

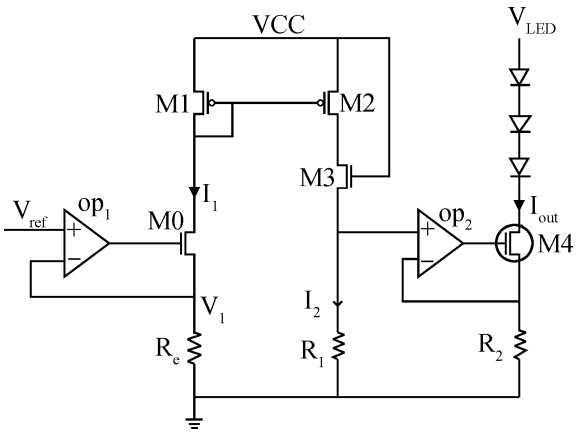


Fig. 1. Traditional LED constant-current drive controller.

Since M1 and M2 have equal gate–source voltages and operate in saturation, we can write:

$$I_1 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 , \tag{2}$$

$$I_2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 . \tag{3}$$

Obtaining:

$$I_2 = \frac{(W/L)_{M2}}{(W/L)_{M1}} I_1, \tag{4}$$

where μ_p is the charge carrier mobility and C_{ox} is the gate oxide capacitance per unit area.

In the same way, amp op_2 makes the voltage of R_1 and R_2 be equal:

$$I_{out} R_2 = I_2 R_1. \tag{5}$$

Therefore, the initial current I_1 on the R_e is mirrored for I_2 through M1, M2, and then mirrored by the resistor R_1, R_2, and we finally get the output current. This can be calculated as:

$$I_{out} = \frac{V_{ref}}{R_e}\frac{(W/L)_{M2}}{(W/L)_{M1}}\frac{R_1}{R_2}. \tag{6}$$

It is easy to see that the output current and the external resistor are inversely proportional in Eq. (6). By changing the value of R_e we can adjust the output current. Once the external resistor is fixed, we can guarantee a constant output current for the LED.

The above analysis ignores the effect of channel-length modulation. Actually, V_{DS} of the mirror FETs are not equal, so the output current will have a considerable error. In saturation:

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}), \tag{7}$$

where λ is the channel-length modulation coefficient and V_{DS} is the drain–source voltage of a FET.

Since R_1 and R_2 are not external resistors, under standard MOS technique conditions, there are big tolerances in resistances (over 10%), so it is difficult to achieve an accurate current mirror image. In addition, the amp op offset and mismatches in the MOS transistors will also cause errors in the output current. Considering the above reasons, the actual current can therefore be written as:

$$I_{out} = \frac{V_{ref} - V_{os}}{R_e + \Delta R_e}\frac{(W/L + \Delta W/\Delta L)_{M2}}{(W/L + \Delta W/\Delta L)_{M1}}$$

$$\times \frac{(V_{GS2} - V_{TH} + \Delta V_{TH})^2}{(V_{GS1} - V_{TH})^2}\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\frac{R_1 + \Delta R_1}{R_2 + \Delta R_2}, \tag{8}$$

where V_{os} is the offset voltage of amp op_1, V_{DS1} (V_{DS2}) is the drain–source voltage of FET M1(M2), $\Delta V_{TH} = V_{TH1} - V_{TH2}$, ΔR_e, ΔR_1, ΔR_2, ΔW, ΔL are the warps of each variables.

The relative error of the output current can be calculated as:

$$\varepsilon_c = |I_{out1} - I_{out}| / I_{out}. \tag{9}$$

The relative current matching error can be calculated as:

$$\sigma = 2 \times |I_{out2} - I_{out1}| / (I_{out1} + I_{out2}), \tag{10}$$

where I_{out} is the designed target value. I_{out1} and I_{out2} are the output currents of different channels in the LED driver.

Because of the mature technology for low offset operational amplifiers, the offset voltage of the amplifier can easily be designed less than 1 mV (when the voltage offset of op_1 is 1 mV and the relative current accuracy error of I_{out1} is only 0.1%)[7–9], and R_e is an external resistor whose value can be made exact by choosing a high precise resistor outside the chip. Therefore, the relative output current error approximates the relative total current magnification error (I_{out}/I_1), which is decided by the resistances of R_1, R_2, the channel length modulation effect, the mismatch of V_{TH} and the width to length ratio between the mirror FETs.

3. Proposed LED constant-current drive controller

3.1. High precision design

Figure 2 shows the high precision LED constant-current drive controller with the CSM mechanism. To solve the problem of inaccurate current caused by the large errors of R_1 and R_2, we could adopt a MOSFET which works in the deep linear region to substitute resistance. However, when we regulate the output current I_{out} by regulating the value of the external resistance R_e, there are larger swings in the gate voltage V_g of MOS tubes M5 and M6, so it is difficult for them to work in the deep linear region all the time, resulting in large changes in their resistance value. This method is not feasible. However, a MOSFET operating in the linear region can provide a linear characteristic of I_D/V_{GS} when the drain–source voltage is constant, that is:

$$I_D = (1/2)\mu C_{OX}(W/L)[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]. \tag{11}$$

The proposed project is just based on the operating characteristics of the MOSFET. We use a MOSFET with fixed drain–source voltage to replace the traditional mirror image resistance, as is shown in Fig. 2. Amp op_2 and op_4 make the drain voltage of M5 (V_3) and M6 (V_4) be equal to a low value (300 mV), to ensure that M5, M6 can always work in the linear region.

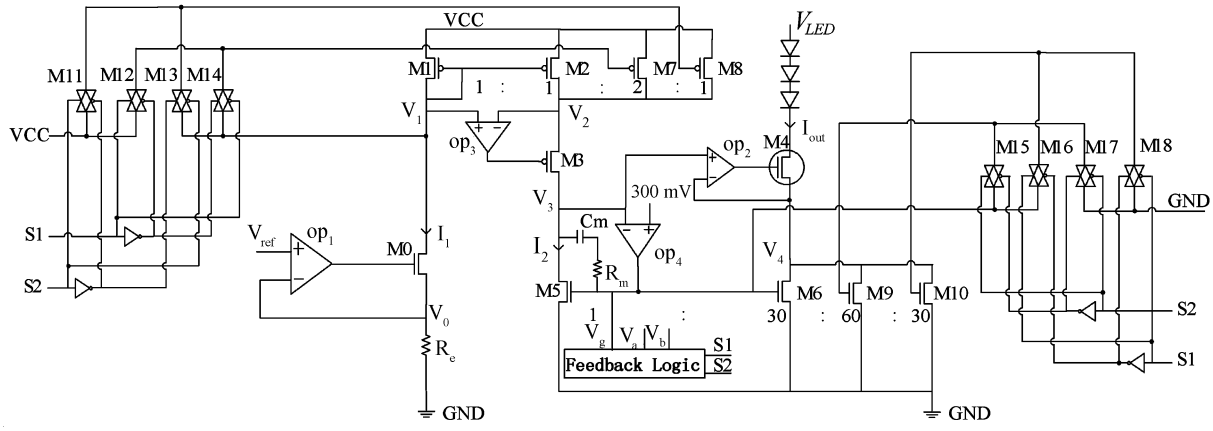


Fig. 2. LED constant-current drive controller proposed in this paper.

In addition, the increase of amp op_3, in combination with op_2 and op_4, ensures that all mirror tubes have the same drain voltage. Thereby we can effectively eliminate the current image error caused by the channel length modulation effect.

Compared with the saturation region, a MOSFET operating in the linear region has less current image error caused by the mismatch of V_{TH}. If the two mirror FETs are M1, M2, $V_{GS1} = V_{GS2}$, $V_{DS1} = V_{DS2}$, $\Delta V_{TH} = V_{TH1} - V_{TH2}$, $\beta = \mu C_{OX}(W/L)$, when they operate in the saturation region, we have:

$$\frac{I_{DS2}}{I_{DS1}} = \frac{\beta_2}{\beta_1}\left(\frac{V_{GS2} - V_{TH2}}{V_{GS1} - V_{TH1}}\right)^2 = \frac{\beta_2}{\beta_1}\left(1 + \frac{2\Delta V_{TH}}{V_{GS1} - V_{TH1}} + \frac{\Delta V_{TH}^2}{V_{GS1} - V_{TH1}}\right). \quad (12)$$

Considering $\Delta V_{TH} \ll V_{GS1} - V_{TH1}$, we can write:

$$\frac{I_{DS2}}{I_{DS1}} = \frac{\beta_2}{\beta_1}\left(1 + \frac{2\Delta V_{TH}}{V_{GS1} - V_{TH1}}\right). \quad (13)$$

When they operate in the linear region, we have:

$$\frac{I_{DS2}}{I_{DS1}} = \frac{\beta_2\left[2\left(V_{GS2} - V_{TH2}\right)V_{DS2} - V_{DS2}^2\right]}{\beta_1\left[2\left(V_{GS1} - V_{TH1}\right)V_{DS1} - V_{DS1}^2\right]} \cong \frac{\beta_2}{\beta_1}\left(1 + \frac{\Delta V_{TH}}{V_{GS1} - V_{TH1}}\right). \quad (14)$$

Now the output current inaccuracy is mainly caused by the mismatch properties of the MOS transistors, which are mainly due to the mask and photolithography, as well as diffusion. To reduce these errors, the layout must be rational[10−12]. More details will be given in the following.

3.2. Accurate expansion of the output current range by the CSM mechanism

The output current range is restricted by the gate voltage V_g of M5 and M6. If V_g is too high or too low, we cannot guarantee that M5 and M6 work in the linear region, which leads to an imprecise output current. A novel CSM mechanism is adopted to optimize the electric property of the mirror FETs. In this mechanism, three types of mirror image modes are designed and can be switched in different working regions automatically by a feedback logic circuit. As shown in Fig. 2, M7–M10 are controlled by the switch signal S1, S2 for different magnifications. We choose the total current magnification to be 120 in this design; if the first magnification is α, the second magnification is β, and the working conditions of three types of modes are shown in Table 1.

Table 1. Current mirror image conditions in different modes.

	S1	S2	α	β	$\alpha\beta$
Mode 1	0	0	4	30	120
Mode 2	1	0	2	60	120
Mode 3	1	1	1	120	120

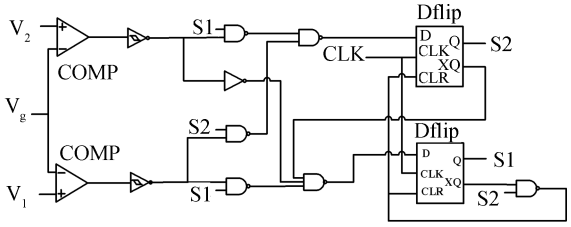


Fig. 3. Inner circuit of feedback logic.

Figure 3 shows the feedback logic circuit which can switch the mirror image modes according to the value of V_g momentarily, where V_1, V_2 are pre-set referenced voltages; it works as follows: If $V_1 < V_g < V_2$, S1, S2 will not change, that is to say, when the value of V_g is between V_1 and V_2, the circuit does not change modes. If $V_g < V_1$, S1, S2 will change in the order 11→10→00. In this case, the circuit will switch in the order mode 3→mode 2→mode 1 to increase V_g. If $V_g > V_2$, S1, S2 will change in the order 00→10→11. In this case, the circuit will switch in the order mode 1→mode 2→mode 3 to decrease V_g.

From what has been discussed above, we can draw a conclusion that the electric property of the mirror FETs is optimized by the negative feedback design. V_g is always between V_1 and V_2 when the output current changes over a wide range. Thus, we can achieve accurate expansion of the output current range in the same total magnification. The I–V curve of M6 is shown in Fig. 4; when the circuit works in mode 1, we choose V_1 to V_2 where output current is 5 mA to 15 mA. Then we get

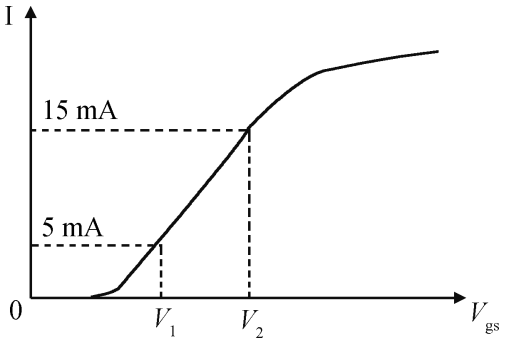


Fig. 4. I–V curve of M6.

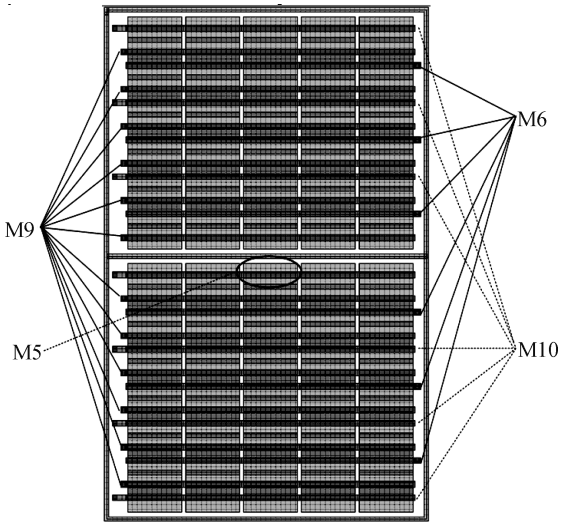


Fig. 5. Layout of the mirror FETs.

three different modes corresponding to different current output ranges respectively: mode 1 is 5–15 mA, mode 2 is 10–30 mA, and mode 3 is 20–60 mA. These three modes can switch automatically in accordance with V_g to ensure that the mirror FETs have a good linearity I–V curve in the whole range of 5–60 mA. Eventually, we can get:

$$I_{out} = \alpha\beta\frac{V_{ref}}{R_e} = 120I_1. \tag{15}$$

Although the whole range we designed is 5–60 mA, we can achieve different ranges (such as 10–120 mA, 20–240 mA, 40–480 mA) to meet more applications by increasing the number of M4, M6, M9 and M10.

3.3. Layout design

The layout design is very important to the chip's performance. In order to match the mirror image transistors accurately, the output transistors are designed as cross-fingered, as shown in Fig. 5. Also, we should choose the device size to be as large as possible in the design, so that the mirror image current error caused by the W/L error can be minimized. In order to reduce the matching error between the current channels, several LED current channels should be put together as much as possible, and be kept apart from other parts. At the same time, attention should be paid that the metal wire length between each channel to the previous cell and the output pin is equal to ensure that each wire has the same voltage drop. Of course, measures that the isolation ring is among the modules are also necessary. The layout of the three-channel constant-current drive controller is shown in Fig. 6.

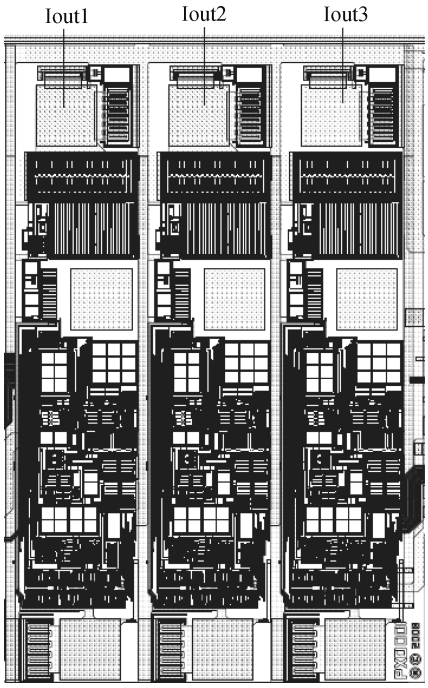


Fig. 6. Layout of the three-channel constant-current drive controller.

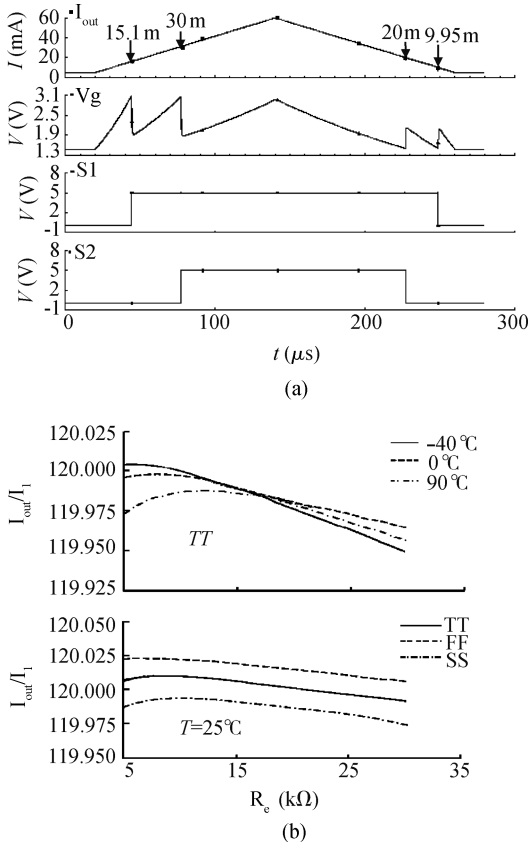


Fig. 7. (a) Simulated waveform of automatically switching between three mirror image modes. (b) I_{out}/I_1 versus R_e under different conditions.

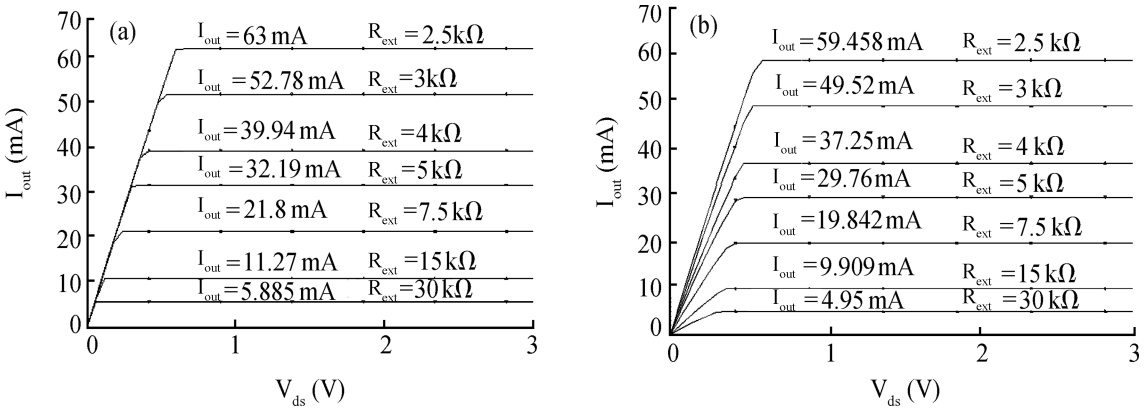


Fig. 8. (a) Simulation result of traditional controller. (b) Simulation result of proposed controller.

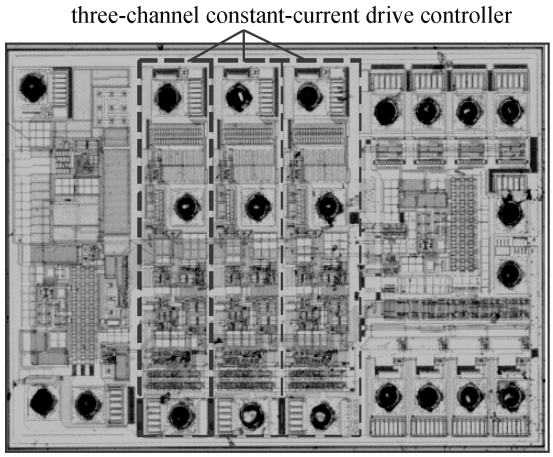
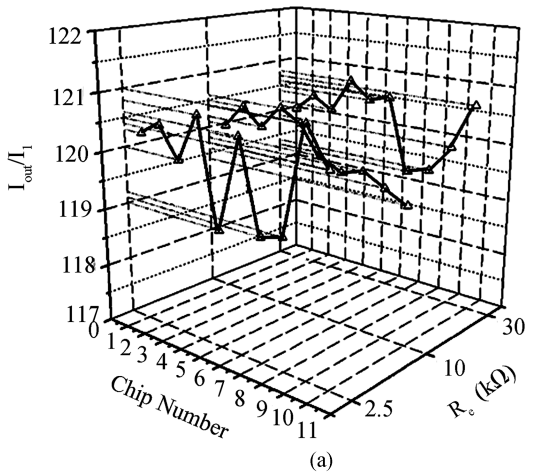


Fig. 9. A micro-photograph of the chip.



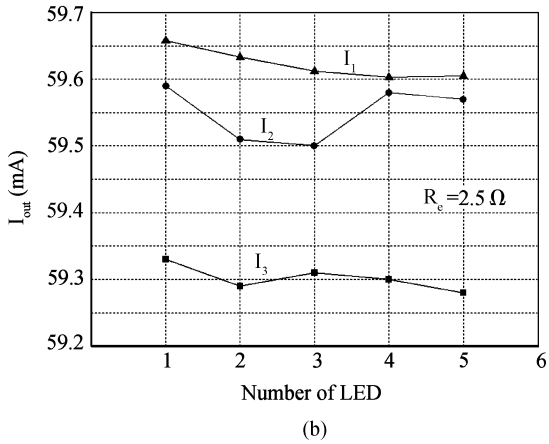


Fig. 10. (a) Test result of 10 chips for I_{out}/I_1. (b) Each channel's current versus the number of LEDs.

4. Experimental results

This article is based on the TSMC 0.6 μm BCD model and gives a simulation and verification of the designed circuit with the Spectre simulator.

Figure 7(a) is the simulation waveform of the circuit during automatic switching between three mirror image modes by the current. We can see that the gate voltage of the mirror FET can always be maintained from 1.5 V to 3 V when the output current changes in the whole range of 5–60 mA. Figure 7(b) is the simulation result of the relationship between the total current magnification (I_{out}/I_1) and the external regulating resistance (R_e) under different conditions. We can see that the maximal relative error of the total current magnification is only 0.045%.

A traditional LED constant-current drive controller is also designed for comparison. We make $V_{ref} = 1.24$ V, VCC = 5 V, $R_1 = 150\ \Omega$, $R_2 = 5\ \Omega$, $(W/L)_{M2}/(W/L)_{M1} = 4$, so we will have the same total magnification and the lowest workable load terminal voltage. Figure 8 shows the two simulation results of the relationship between the output current with different external regulating resistances and the load terminal voltage. We can see that the output current can be set up when the load terminal voltage reaches 0.6 V, and is not affected by the load supply voltage, which is the advantage of the constant-current drive controller compared with the constant-voltage drive controller. For the traditional circuit, using Eq. (9), we can calculate that the relative current error is over 10% when the external regulating resistance reaches 15 kΩ. For the proposed drive controller, the simulation value of the relative error of the output current is only less than 0.2% when the external regulating resistance varies in the range of 2.5–30 kΩ.

Based on the project designed in the article, a three-channel LED driver IC has been taped out successfully, and a micro-photograph of the chip is shown in Figure 9. The chip area is 1.1×0.7 mm^2, and the power dissipation is only 4 mW. Figure 10(a) shows the total current magnification (I_{out}/I_1) of 10

Table 2. Electrical characteristic comparison between the designed chip and MBI60x (T = 25 °C).

Characteristic	Condition	Designed chip			MBI60x			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	—	6.0	—	18	6.0	—	12	V
Inside supply voltage	V_{DD} = 12 V		4.8	5.3	6.04.8	5.3	6.0	V
Voltage at R_e	V_{DD} = 6.0–18 V	1.238	1.240	1.242	1.20	1.24	1.30	V
Output current 1	V_{ds} = 0.6 V, R_e =2.5 kΩ	59.43	60.0	60.29	58.6	60.0	63.6	mA
Relative current error 1	V_{ds} = 0.6 V, R_e =2.5 kΩ	—	—	0.93	—	—	6	%
Output current 2	V_{ds} = 0.6 V, R_e =30 kΩ	4.93	4.97	5.01	4.75	5.0	5.2	mA
Relative current error 2	V_{ds} = 0.6 V, R_e = 30 kΩ	—	—	0.84	—	—	5	%
Relative current matching error	V_{ds} = 0.6 V, R_e =2.5 kΩ	—	—	1.5	—	—	3	%
Current skew at various load voltages	The LED cluster number is 1–5	—	—	0.15	—	—	0.2	%

chips whose three channels severally connect an external resistor of 2.5 kΩ, 10 kΩ, 30 kΩ; we can see that I_{out}/I_1 varies from 119 to 121, and its relative error is less than 0.84%. Figure 10(b) shows each channel's output current when connecting the same value of external resistor (2.5 kΩ) but where the LED cluster number is different; we can calculate that the relative current error is less than 1%, the relative current matching error is not more than 1.5% and the maximal current skew at various load voltages is 0.15%. Table 2 shows an electrical characteristic comparison between the designed chip and MBI60x, which is an LED constant-current driver produced by Macroblock in 2007. We can see that the maximal relative current error of MBI60x is 6%, its maximal relative current matching error is 3% and its maximal current skew at various load voltages is 0.2%, which are all much higher than the electrical characteristics of the chip designed in this paper.

5. Conclusion

In this paper, we studied a new constant-current LED drive controller based on the TSMC 0.6 μm BCD. To get a high precision output current, it uses a MOSFET with fixed drain voltage instead of the conventional mirror resistance, and a negative feedback amplifier to keep all the mirror device voltages equal. To expand the precision current range, the electric properties of the mirror FETs are optimized by a CSM mechanism, which can select the current mirror image modes automatically according the different output currents. Layout design and verification were completed with Cadence Spectre using TSMC 0.6 μm BCD technology. The tape-out results of the three-channel LED driver show that the output current range is 5–60 mA, the relative error of the output current is less than 1%, and the maximal relative current matching error among the three channels is 1.5%; this is due to the good design of the LED drive controller.

References

[1] Komine T, Nakagawa M. Fundamental analysis for visible-light communication system using LED lights. IEEE Trans Consum Electron, 2004, 50(1): 100

[2] Hu Y, Jovanovic M M. A novel LED driver with adaptive drive voltage. Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008: 565

[3] Liu Lianxi, Yang Yintang, Zhu Zhangming. The design research on the constant current LDO driver of the white light LED. Journal of Xidian University, 2007, 34(2): 265 (in Chinese)

[4] Xu Xiaoru, Wu Xiaobo, Zhao Menglian, et al. Design and implementation of a high dimming ration LED driver controller. Journal of Semiconductors, 2009, 30(2): 025010

[5] Chen C C, Wu C Y, Chen Y M, et al. Sequential color LED backlight driving system for LCD panels. IEEE Trans Power Electron, 2007, 22(3): 919

[6] Wang Hongyi, Lai Xinquan, Li Yushan. A piecewise-linear compensated bandgap reference. Chinese Journal of Semiconductors, 2004, 25(7): 771 (in Chinese)

[7] Enz C C, Temes G C. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stablilization. Proc IEEE, 1996, 84(11): 1584

[8] Chan P K, Siek L, Tay H C, et al. A low-offset class-AB CMOS operational amplifier. IEEE International Symposium on Circuits and Systems, 2000: 455

[9] Han Shuguang, Chi Baoyong, Wang Zhihua. A novel offset cancellation technique for low voltage CMOS differential amplifiers. Chinese Journal of Semiconductors, 2006, 27(5): 778 (in Chinese)

[10] Christopher M J, Ismail M. Statistical modeling of device mismatch for analog MOS integrated circuits. IEEE J Solid-State Circuits, 1992, 27(2): 254

[11] Lakshmikumar K R, Hadaway R A, Copeland M A. Characterization and modeling of mismatches in MOS transistors for precision analog design. IEEE J Solid-State Circuits, 1986, 21(6): 1057

[12] Pelgrom M J M, Duinmaiger A C J, Welbers A P G. Matching properties of MOS transistors. IEEE J Solid-State Circuits, 1989, 24(5): 1433