An undersampling 14-bit cyclic ADC with over 100-dB SFDR*

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Abstract: A high linearity, undersampling 14-bit 357 kSps cyclic analog-to-digital convert (ADC) is designed for a radio frequency identification transceiver system. The passive capacitor error-average (PCEA) technique is adopted for high accuracy. An improved PCEA sampling network, capable of eliminating the crosstalk path of two pipelined stages, is employed. Opamp sharing and the removal of the front-end sample and hold amplifier are utilized for low power dissipation and small chip area. An additional digital calibration block is added to compensate for the error due to defective layout design. The presented ADC is fabricated in a 180 nm CMOS process, occupying 0.65×1.6 mm^2. The input of the undersampling ADC achieves 15.5 MHz with more than 90 dB spurious free dynamic range (SFDR), and the peak SFDR is as high as 106.4 dB with 2.431 MHz input.

Key words: cyclic ADC; high linearity; undersampling; improved passive capacitor error-average sampling network; opamp sharing

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1. Introduction

Radio frequency identification (RFID) is a wireless communication technology that lets a processing device (reader) read the identity of electronic tags from a distance, without requiring a battery in the tags[1]. With developments in microelectronics and low-power semiconductor technologies, RFID tags and readers can be reused and the cost of tags is reduced to a few pennies per tag. The RFID system has been employed in purchasing and inventory management, and new applications will be developed, such as transportation, airlines, healthcare, and mobile phones[1].

Figure 1 shows the simplified RFID transceiver architecture. The filtered RF signal is amplified by a low noise amplifier (LNA). The signal is bridged from the radio frequency to the baseband by quadrature mixing, and then limited and passed through an anti-aliasing filter. The baseband signal is amplified by variable gain amplifier and converted to a digital signal by an analog-to-digital convert (ADC). The digital baseband processing block performs advanced signal processing. The ADC connects the analog and digital parts of the system, which is critical for an RFID transceiver. The ADC is embedded in this RFID transceiver system SOC. The resolution of the ADC is required to be 14 bit and the sampling frequency to be above 300 kHz. The power must be low and the chip area must be small.

Among different ADC architectures, successive approximation (SAR) ADCs and cyclic ADCs perform analog to digital conversion with small chip area and low power dissipation at moderate frequencies. However, the performance of SAR ADCs[2] is limited by the deficiency of comparator designs and the nonlinearity of capacitors, and SAR architecture suffers from increased area for high-resolution requirements due to the passive elements used.

In this paper, a high linearity, undersampling 14-bit 375 kSps cyclic is proposed to meet the requirement of the RFID transceiver system. The passive capacitor error-averaging (PCEA) technique is adopted. PCEA is an analog calibration scheme to compensate for the capacitor mismatch[3]. An improved PCEA sampling network is proposed to eliminate the crosstalk path between the two pipelined stages. The opamp is shared and the dedicated front-end sample and hold amplifier (SHA) is removed to reduce power dissipation and save chip area. Based on the initial measurement results, an additional digital calibration algorithm is proposed to compensate for the error arising from defective layout design.

This paper describes the architecture of the 14-bit cyclic ADC, highlights the key techniques and the circuit implementations, and also describes the measurement and improvement for high linearity.

2. Proposed ADC architecture

The proposed undersampling 14-bit cyclic ADC is shown in Fig. 2. It consists of pipelined passive capacitor error-average (PCEA) stage 1 and PCEA stage 2, a clock generator, a counter, a bandgap and on-chip I/V reference. The 2-stage pipelined cyclic structure is employed to compromise the conversion rate and chip area. Each PCEA stage gives 1.5 effective bits. The cyclic ADC supplies serial output. Every 7 clock cycles, a full single 14-bit binary code is produced and a sync signal is generated.

In order to improve the accuracy of the ADC, the PCEA

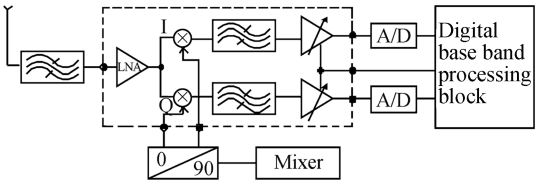

Fig. 1. Simplified RFID transceiver architecture.

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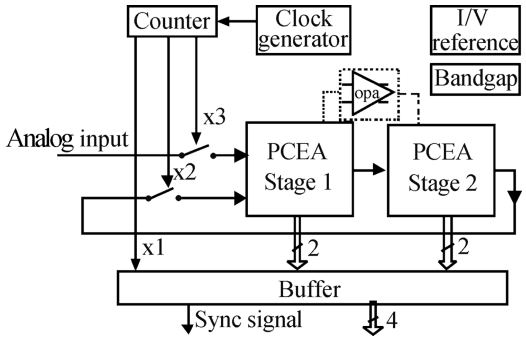

Fig. 2. 14-bit cyclic ADC architecture.

technique is adopted in the two stages. In a cyclic ADC, capacitor mismatch introduces an interstage amplifier gain error, which results in missing decision levels or missing codes[4]. PCEA is an analog calibration technique to treat capacitor mismatch error[3]. The improved PCEA sampling network can improve the accuracy and reduce the power dissipation at the same time.

The opamp is shared between PCEA stage 1 and PCEA stage 2. A conventional stage is operated in a two-phase nonoverlapping clock, a sampling phase and an amplification phase. Since the opamp is not required in the sampling phase, it can be used in another stage for amplification. The disadvantage of opamp sharing is the memory effect[5]. In this design, a telescopic gain boosting opamp is used to supply high DC gain to reduce the memory effect.

The dedicated front-end SHA is removed as shown in Fig. 2 for low power. The front-end SHA introduces extra power dissipation and adds noise and distortion to the input signal[6]. However, the removal of the SHA results in aperture error. In this work, sampling switches are modified to reduce the aperture error.

3. Circuit implementation

3.1. Improved PCEA sampling network

The PCEA stage is operated in a four-phase nonoverlapping clock. Figure 3 shows PCEA stage 1 in the amplification phase and stage 2 in the sampling phase. They share one opamp. In the subsequent T_1 and T_2 phases, C1 and C2 merge charge sampled in T_3 and T_4 phases. Therefore the two residue voltages with complementary error are averaged to reduce the capacitor mismatch error. With PCEA used, the first-order gain error can be removed and a high accuracy can be obtained[7].

An improved PCEA sampling network is proposed in the work to maintain the charge fidelity at the summing node ip in Fig. 3(a), which is critical for the opamp sharing technique. At the falling edge of T_3, capacitor C3 finishes sampling and the sampling switch is off, which introduces a signal-dependent charge injection. The charge injection couples through CP, which results in an opamp output error. The improved PCEA sampling network is shown in Fig. 4. The bottom of C2A is tied to AC ground in the whole sampling phase, so that the coupling only introduces a fixed offset. In sampling phases T_3 and T_4, only switch T_{3a} or T_{4a} is on respectively. The load of the opamp

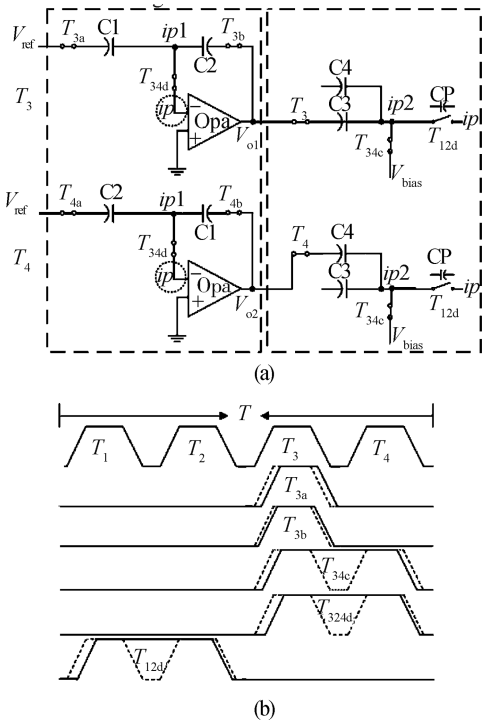

Fig. 3. Passive capacitor error-averaging technique. (a) Stage 1 and 2 in T_3 and T_4 phases. (b) Timing diagram.

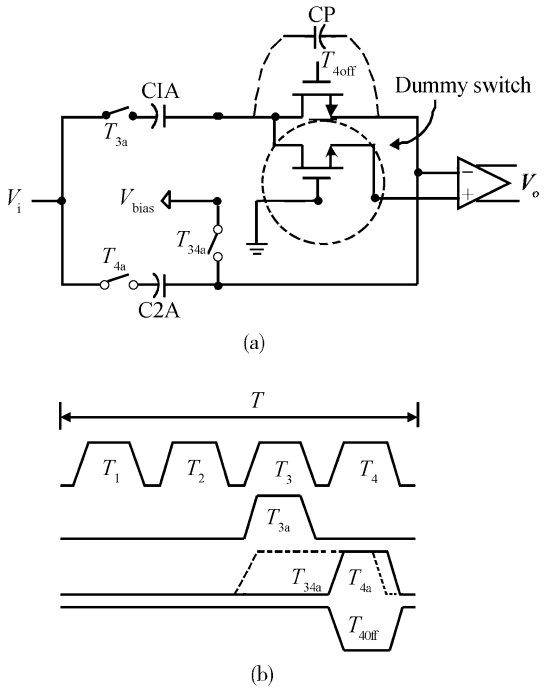

Fig. 4. Improved sampling network and timing.

in the previous stage is equal in T_3 and T_4. Compared with the sampling network adopted in Ref. [3], which has the problem of unbalanced load, the load of the opamp in this work is reduced and the power dissipation is decreased.

With this analog calibration technique, the capacitor matching requirement in the PCEA stage is relaxed. Within the limit of KT/C noise, the capacitor size is scaled down to save power dissipation and chip size.

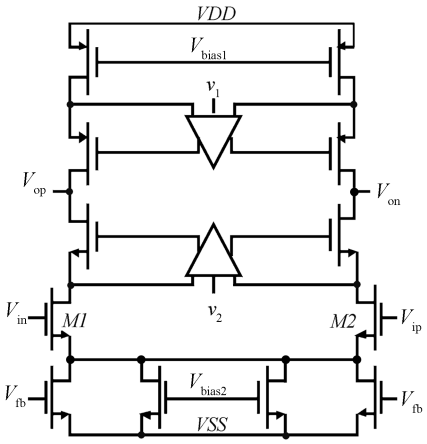

Fig. 5. Schematic of opamp.

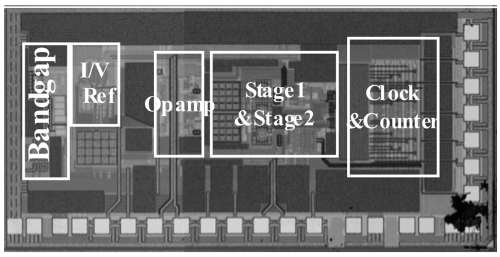

Fig. 6. Die micrograph.

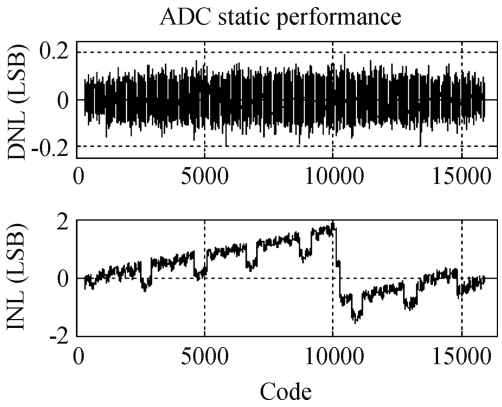

Fig. 7. Measured DNL and INL.

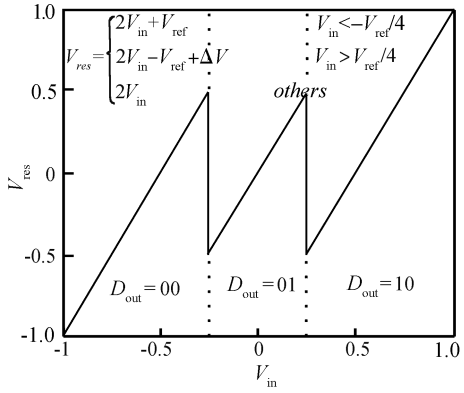

Fig. 8. Ideal transfer curve of the 1.5-b stage ($\Delta V = 0$, $V_{\rm ref} = 1$).

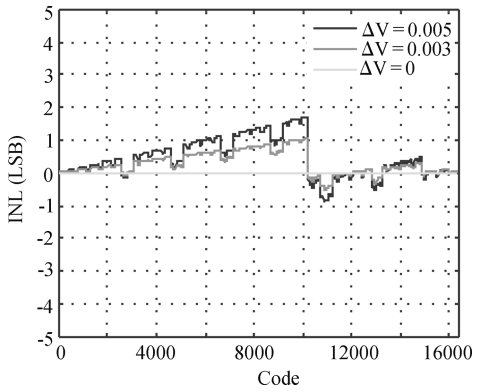

Fig. 9. Simulated INL with different error terms.

3.2. Opamp

For a high accuracy and low power cyclic ADC, high DC gain and a low power dissipation opamp is required. Compared with a folded cascode opamp, a telescopic cascode opamp can provide higher speed with lower power dissipation. The telescopic cascode opamp shown in Fig. 5 is employed in this design. The length of the input NMOS devices is designed to be very small, such that the parasitic capacitor is decreased and the speed of the opamp is improved. Gain-boosting stages are added to satisfy the gain requirements of a 14-bit ADC. The opamp achieves a DC gain of 106 dB, and the output differential swing range is 3.08 V. The high DC gain and small parasitic capacitance of the input node reduce the memory effect introduced by opamp sharing.

4. Measurement and improvement

The 14-bit undersampling cyclic 357 kSPs ADC is fabricated in 180 nm CMOS mixed-signal technology. It occupies a die area of 0.65×1.6 mm^2, which includes PCEA stage 1, stage 2, bandgap, clock generator, counter and on-chip I/V references. The die micrograph is shown in Fig. 6. The measurements are performed with a 3 V supply at room temperature (27 ℃), including static performance and FFT measurement. A 2.431 MHz full-scale sinusoidal signal is selected to measure the static performance. The measured integral nonlinearity (INL) errors and differential nonlinearity (DNL) errors are shown in Fig. 7, and they are less than 0.2 LSB and 2 LSB respectively. With −0.0864 dBFS 2.431 MHz, 5.03 MHz and 15.59 MHz input signal, the measured FFT plots are shown in Figs. 11(a), 12(a) and 13(a), respectively.

As shown in Fig. 7, the measured INL errors are nonlinear and there is a jump at the codes around 10000. Based on the transfer curve of the 1.5-b stage in Fig. 8, the jump in the measured INL occurs where the reference voltage of the first PCEA stage changes from 0 to $-V_{\rm ref}$, which supplies important calibration information. Due to defective layout design, an inaccurate residue calculation exists in the first stage of the cyclic ADC. The error is independent of the input signal and is only introduced when the reference voltage is $-V_{\rm ref}$, which is also verified by the simulation results in Fig. 9. Error term ΔV is added to the residue voltage described by the formula in Fig. 8. As an example, ΔV is set to 0, 0.0003 and 0.0005 for the simulation, respectively. With the error term ΔV added, the simulated INL errors in Fig. 9 are similar to the measured

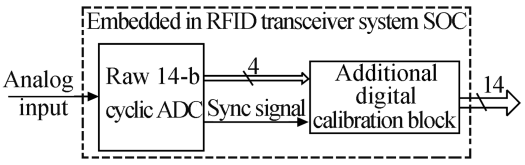

Fig. 10. The undersampling 14-b cyclic ADC with additional digital calibration block.

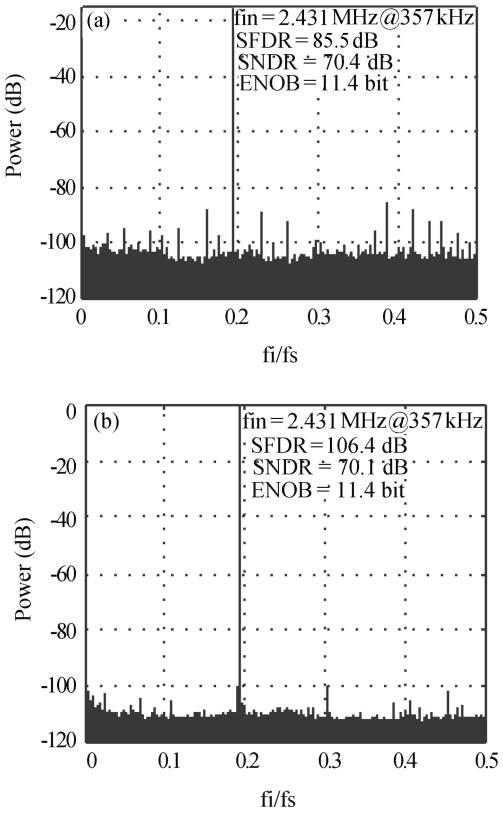

Fig. 11. Measured FFT plot. (a) Before additional digital calibration. (b) After additional digital calibration.

results in Fig. 7.

The inaccurate residue calculation results in the weight of the 14-bit code deviating from the ideal one. In order to improve the performance of the cyclic ADC, an additional digital calibration block is added as shown in Fig. 10. A calibration term α is introduced to compensate for the error term V. The corrected output of the 14-bit cyclic ADC is described by

$$D_{\text{outc}} = (D_{\text{M}} \times 2 + D_{\text{L}}) \times 2^{12}(1-\alpha) + (D'_{\text{M}} \times 2 + D'_{\text{L}}) \times 2^{11} + (D_{\text{M}} \times 2 + D_{\text{L}}) \times 2^{10}(1-\alpha) + (D'_{\text{M}} \times 2 + D'_{\text{L}}) \times 2^{9} + \cdots + (D_{\text{M}} \times 2 + D_{\text{L}}) \times 2^{2}(1-\alpha) + (D'_{\text{M}} \times 2 + D'_{\text{L}}) \times 2^{1} + (D_{\text{M}} \times 2 + D_{\text{L}}) \times (1-\alpha) + D'_{\text{M}}, \quad (1)$$

where D_{M}, D_{L} and D'_{M}, D'_{M} are the 2-b outputs of PCEA stage 1 and stage 2, respectively. The evaluation of the calibration parameter α is based on the SFDR of the cyclic ADC.

A comparison of the dynamic performance before and after the additional −0.0864 dBFS 2.431 MHz sinusoidal signal. The peak SFDR improves from 85.5 dB to 106.4 dB. With 5.03 MHz input, the measured SFDR improves by 14 dB to 100.9

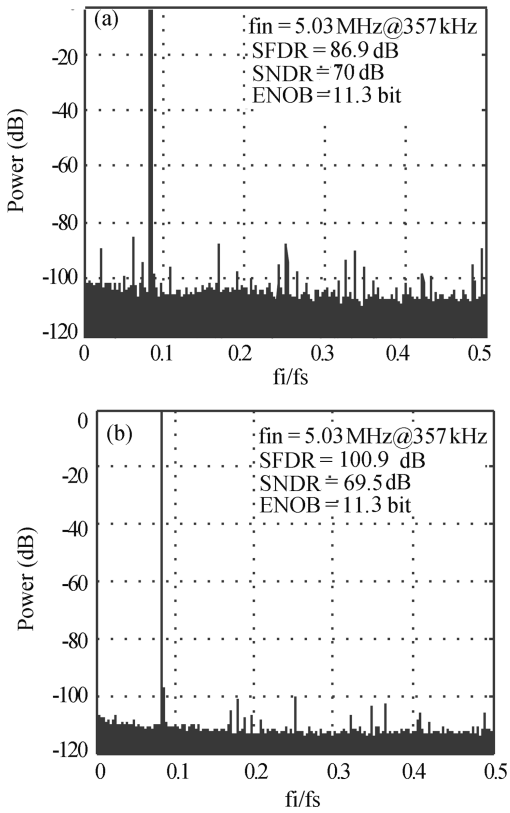

Fig. 12. Measured FFT plot. (a) Before additional digital calibration. (b) After additional digital calibration.

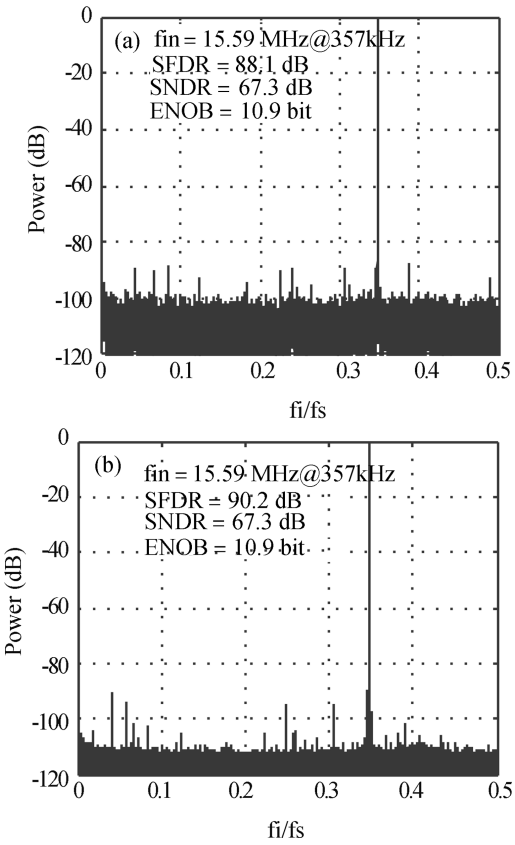

Fig. 13. Measured FFT plot. (a) Before additional digital calibration. (b) After additional digital calibration.

Table 1. Performance summary.

Parameter	Value
Technology	180 nm CMOS
Resolution	14 bit
Conversion rate	357 kSps
Supply voltage	3 V
Input range	2 V
DNL, INL	0.2 LSB, 2 LSB
SNDR	70.1 dB @ $f_{in} = 2.431$ MHz 69.5 dB @ $f_{in} = 5.03$ MHz
SFDR	67.1 dB @ $f_{in} = 15.59$ MHz 85.5 dB @ $f_{in} = 2.431$ MHz 86.9 dB @ $f_{in} = 5.03$ MHz 88.1 dB @ $f_{in} = 15.59$ MHz 106.4 dB (after calibration) @ $f_{in} = 2.431$ MHz 100.9 dB (after calibration) @ $f_{in} = 5.03$ MHz 90.2 dB (after calibration) @ $f_{in} = 15.59$ MHz
Power consumption	4.2 mW
FOM	4.3 pJ/step
Area (ADC core)	0.65×1.6 mm^2

Table 2. Comparison with some previous work.

Parameter	Ref. [2]	Ref. [8]	Ref. [9]	Ref. [10]	This work
Resolution (bit)	10	12	12	10	14
Sampling rate (MSps)	> 1	0.143	2	2.3	0.357
SNDR/SFDR (dB)	56/NA	NA/NA	70.9/81.7 @ $f_{in} = 100$ kHz	NA/74.95 @ $f_{in} = 100$ kHz	70.1/106.4 @ $f_{in} = 2.431$ MHz
Power (mW)	< 100	3.94	3.6	NA	4.2

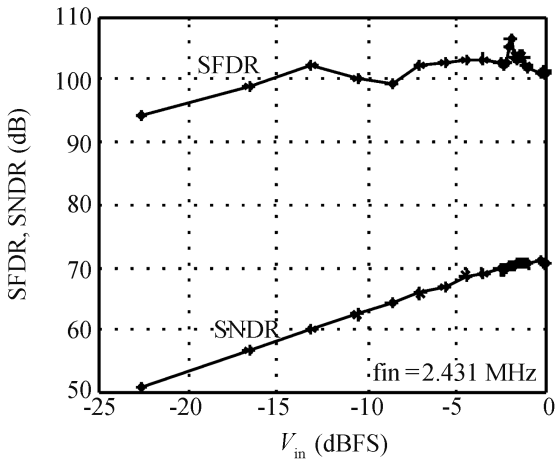

Fig. 14. Measured SFDR and SNDR versus input amplitude.

dB shown in Fig. 12. The input frequency of the undersampling cyclic ADC can increase to 15.59 MHz, and the measured SFDR is 90.2 dB after additional calibration shown in Fig. 13. Figure 14 describes the dynamic performance with different input amplitudes. The measurement confirms that the additional digital calibration eliminates the errors arising from defective layout design, and significantly improves the linearity of the ADC.

With 3 V supply, the cyclic ADC consumes 4.2 mW. The common figure of merit (FOM) is 4.3 pJ/step according to

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \times f_s}, \tag{2}$$

where P is the power dissipation and f_s is the sampling rate. A common figure of merit (FOM)[11] is also used to evaluate the undersampling ADC performance as

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \times 2 \times f_{\mathrm{ERBW}}}, \tag{3}$$

where f_{ERBW} is the effective resolution bandwidth (ERBW). ERBW is the input frequency where the SNDR has dropped by 3 dB. Only the 2.431, 5.03 and 15.59 MHz signals are selected as inputs due to the limitation of the bandpass filters. Based on the test results, it is concluded that 5.03 MHz $< f_{\mathrm{ERBW}} <$ 15.59 MHz. The FOM is smaller than 0.166 pJ/step and larger than 0.07 pJ/step.

A summary of the measurement results of the cyclic ADC is provided in Table 1. A comparison between this work and several previous cyclic ADCs is described in Table 2. Compared with other cyclic ADCs, the resolution of this cyclic ADC is higher and the dynamic performance is much better at the same input frequency.

5. Conclusion

A high linearity, undersampling 14-bit 357 kSps cyclic ADC is presented. The PCEA technique is adopted for high accuracy, and an improved PCEA sampling network is proposed. Opamp sharing and the removal of the front-end SHA are utilized for low power dissipation and small chip area. An additional digital calibration block is added for high linearity. With 2.431 MHz, 5.03 MHz and 15.59 MHz input, the ADC achieves 106.4 dB, 100.9 dB and 90.2 dB SFDR, respectively. With a 3 V supply, it consumes 4.2 mW. The ADC satisfies the requirements of the radio frequency identification (RFID) transceiver system.

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