Design and realization of an ultra-low-power low-phase-noise CMOS LC-VCO*

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Abstract: A fully integrated cross-coupled LC tank voltage-controlled oscillator (LC-VCO) using transformer feedback is proposed to achieve a low phase noise and ultra-low-power design even at a supply below the threshold voltage. The ultra-low-power VCO is implemented in the mixed-signal and RF 1P6M 0.18-μm CMOS technology of SMIC. The measured phase noise is –125.3 dBc/Hz at an offset frequency of 1 MHz from a carrier of 2.433 GHz, while the VCO core circuit draws only 640 μW from a 0.4-V supply. The designed VCO can cover a frequency range from 2.28 to 2.48 GHz. The tuning range of the circuit is 200 MHz (8.7%) and the FOM is –195.7 dB, which is suitable for an IEEE 802.11b receiver.

Key words: low phase noise; low-power transformer; voltage-controlled oscillator; feedback
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1. Introduction

For wireless receivers, VCOs are widely used as sinusoidal signal generating blocks in phase locked loop (PLL) based frequency synthesizers, and greatly affect the performance of the whole system. The design goals of a VCO are low-power consumption, low phase noise and wide tuning range. The development of wireless communication demands low-cost low-power solutions in battery operated mobile systems to increase the battery lifetime and to improve the portability[1]. There is usually a trade-off between VCO phase noise and its DC power consumption. Existing techniques for low-voltage low-power VCO design employ either nonstandard processes or external tank components with a high quality factor[2]. Those solutions, however, are not fully compatible with standard CMOS processes and makes system-on-chip integration impossible.

CMOS has become a competitive technology for radio transceivers due to aggressively scaled-down gate lengths, high integration level, and low cost. In this study, a novel transformer feedback voltage-controlled oscillator with high performance, even at a supply lower than the devices' threshold voltages, is presented and implemented in the SMIC (Shanghai, China) 0.18-μm mixed-signal and RF 1P6M CMOS process. The proposed circuit topology of the LC tank VCO is described in detail. The measured results of the implemented VCO are included.

2. Circuit design and analysis

2.1. Proposed low-power VCO

This circuit presented in this paper is based on the negative transconductance LC oscillator[3,4]. As shown in Fig. 1(a), the proposed VCO consists of an integrated transformer and a negative conductance cross-coupled differential pair. The transformer is in the place of the inductor in the conventional VCOs and the transformer feedback can provide extra voltage swings and improve the loaded quality factor to enhance the VCO performance[5]. The transformer's primary coil with self-inductance $L_{\rm d}$ is connected to the drain of the cross-coupled differential pair, forming an LC tank with corresponding capacitive elements. The secondary coil with self-inductance $L_{\rm s}$ is connected at the source of the differential pair. Both the primary coil $L_{\rm d}$ and the secondary coil $L_{\rm s}$ are magnetically coupled to each other with a coupling factor. The LC tank contains accumulation mode varactors allowing continuous frequency tuning. The output inverter buffers were used for measurement with the spectrum analyzer and oscillograph[6–8]. The single-ended oscillating waveform is given in Fig. 1(b) under 0.4-V supply.

Due to the loading inductor, the output signal swings with a maximum peak-to-peak amplitude of about two times the supply voltage. This enables a large oscillating amplitude at a low supply voltage and consequently low-power consumption at a given bias current compared to the conventional topology. Furthermore, the source voltage could swing below the ground potential with the transformer feedback. The oscillating amplitude is enhanced, and consequently, the supply voltage can be reduced for the same phase noise with lower power consumption or for better phase noise with the same power consumption. Most importantly, as shown in Fig. 1(b), the drain and source signals oscillate in phase. When the gate voltage is increased, the drain and source voltages are decreased at the same time; the effective gate–source overdriving is also enlarged, so the supply voltage can be further reduced to ensure that the circuit oscillates normally.

The semi-empirical model proposed in Ref. [9], also known as the Leeson–Cutler phase noise model, is based on an LTI assumption for tuned tank oscillators. It predicts the following behavior for $L(\Delta f)$:

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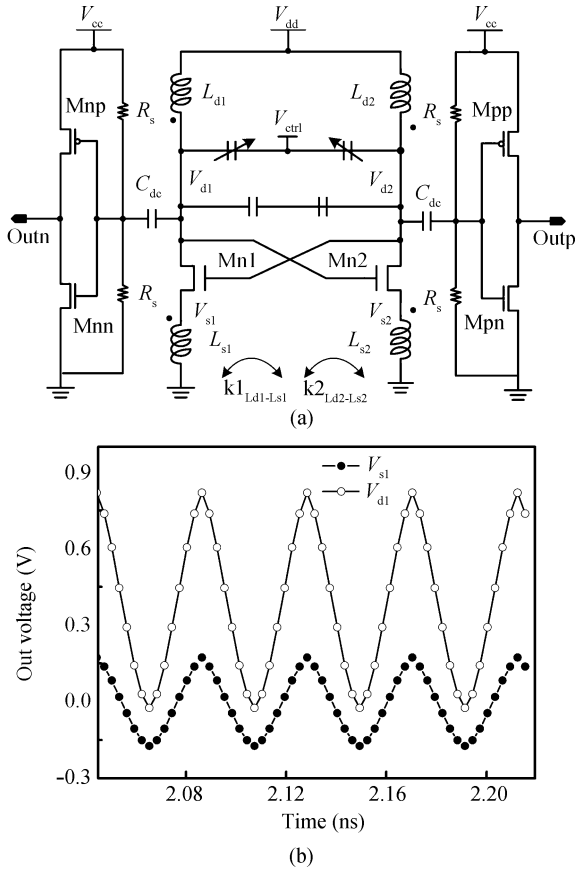

Fig. 1. (a) Schematic of the proposed VCO. (b) Simulated single-ended output voltage waveforms of the proposed VCO.

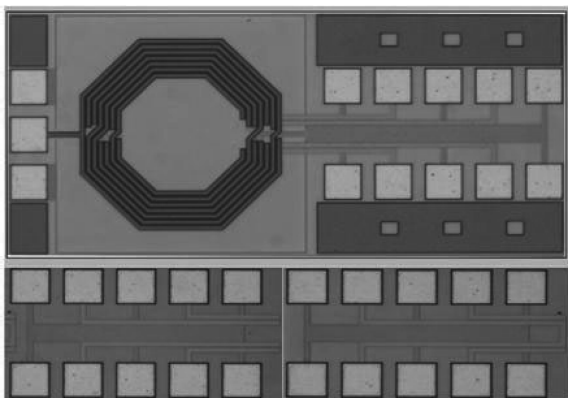

Fig. 2. Micrograph of the implemented transformer.

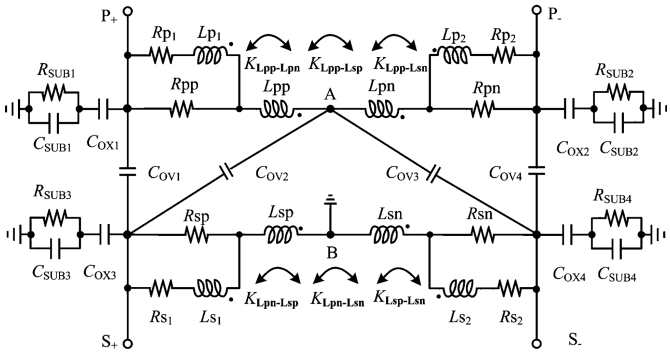

Fig. 3. Proposed equivalent circuit model of the transformer.

$$L(\Delta f) = 10\lg\left\{\frac{2FkT}{P_{\rm s}}\left[1+\left(\frac{f_0}{2Q_{\rm L}\Delta f}\right)^2\right]\times\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right\}, \quad (1)$$

where F is an empirical parameter, k is Boltzmann's constant, T is the absolute temperature, $P_{\rm s}$ is the average power dissipated in the resistive part of the tank, f_0 is the oscillation frequency, $Q_{\rm L}$ is the effective quality factor of the tank with all the loadings in place, Δf is the frequency offset from the carrier, and $\Delta f_{1/f^3}$ is the frequency of the corner between the $1/f^3$and $1/f^2$ regions in the sideband spectrum of the phase noise of the VCO. From the equation, the phase noise is inversely proportional to the square of $Q_{\rm L}$ and to the signal power. The oscillation amplitude and signal power could be maximized at the resonant frequency given bias condition. As a result, to realize VCOs with low-power and low-phase-noise, small series loss and a large L/C ratio of the LC tank are desirable[10]. The series resistive loss could be minimized by an optimum transformer layout. So the design and optimization of the transformer is the key step to achieve low power and low phase noise VCOs.

2.2. Transformer design and test

The layout of the transformer is parameterized based upon several geometrical attributes: outer/inner diameter, line width, line spacing and turn-ratio. The performances of the transformer, such as the insertion loss, the mutual coupling coefficient, and the bandwidth, are dependent on the geometrical attribution[11]. Figure 2 shows a microphotograph of the implemented transformer which is laid out as two interwound octagon spirals using the top metal layer with five turns for the primary and two turns for the secondary. The transformer has an outer diameter of 400 μm, an inner diameter of 236 μm, a metal width of 10 μm, and a spacing of 2 μm. The standard pads arranged as GSGSG were designed to perform an on-wafer measurement for the differential structure. The influences caused by the pad parasitic had been removed by means of the de-embedding technique. The proposed equivalent circuit for a four-port transformer is shown in Fig. 3 based on the 0.18-μm mixed-signal 1P6M salicide 1.8 V/3.3 V RF differential inductor Spice models[12]. The definitions of the parameters in the model can be found in the RF Spice models too. The most important aspect for modeling an on-chip transformer is the extraction or fitting of model parameters. The model parameters of side AB shown in Fig. 3 are equal to each other because of the symmetry of the transformer. The main extracted equivalent circuit parameters of the transformer are listed in Table 1. To verify the performances of the on-chip transformer and examine the validity of the proposed lumped element equivalent circuit model, the transformer is fabricated in the SMIC CMOS process too. The on-wafer measurement was performed with an Agilent E5071B VNA. Figure 4 gives a comparison of the modeled and measured differential-mode S-parameters for the frequency range from 500 MHz to 5 GHz.

Table 1. Extracted equivalent circuit parameters of the transformer.

Parameter	Value	Parameter	Value
L_{pp}	2.35 nH	C_{sub1}	37 fF
L_{sp}	0.85 nH	C_{sub3}	18 fF
R_{pp}	5.97 Ω	C_{ox1}	53 fF
R_{sp}	2.80 Ω	C_{ox3}	23 fF
L_{p1}	1.02 nH	C_{ov1}	35 fF
L_{s1}	0.36 nH	C_{ov2}	22 fF
R_{p1}	3.16 Ω	K_{Lpp_Lpn}	0.78
R_{s1}	1.45 Ω	K_{Lsp_Lsn}	0.75
R_{sub1}	922 Ω	K_{Lpp_Lsp}	0.72
R_{sub3}	706 Ω	K_{Lpp_Lsp}	0.74

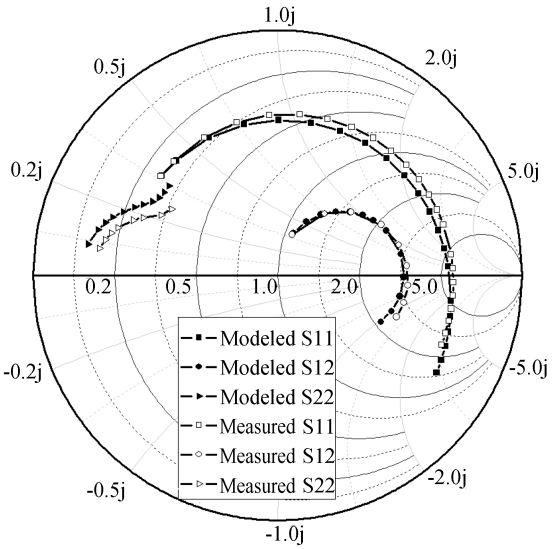

Fig. 4. Differential-mode S-parameters of the transformer.

It can be found that the modeled S-parameters show a high agreement with the measured ones. The coupling coefficient K_{Lpp_Lpn} of the implemented transformer at 2.4 GHz is 0.74 according to the measured S-parameters, and the K_{Lsp_Lsn} is 0.72[13].

3. Measurement results

For demonstration, the presented VCO circuit has been fabricated in SMIC's 0.18-μm CMOS process. The process has six metal layers with a thick top metal of 2.17 μm. The threshold voltages of the NMOS and PMOS devices are about 0.45 V and –0.55 V, respectively. A microphotograph of the chip is shown in Fig. 5. According to the impulse sensitivity function (ISF) theory[14], the phase noise can be significantly reduced if certain symmetry properties exist in the waveform of the oscillation. So any asymmetry in the coupling circuits or the individual oscillators will result in a steady-state operation of the unilaterally coupled oscillators that differs from the ideal. Then the design of the VCO layout must be focused on the full symmetry. The size of the chip including the pads is 675 × 690 μm^2. The output buffer was used for measurement with an Agilent E4440A spectrum analyzer. Figure 6 shows the tuning range of the VCO as a function of control voltage. The tuning range is 200 MHz, from 2.28 to 2.48 GHz, with a control voltage from 0.2 to 1.5 V. Figure 7 shows a plot of the measured phase noise versus offset frequency, and Figure 8 shows the measured output spectrum at an oscillation frequency of 2.433 GHz with a buffered output power of about 0 dBm. The phase noise at l MHz offset is –125.3 dBc/Hz while dissipating only 0.16 mA for the VCO core circuit by a 0.4-V supply.

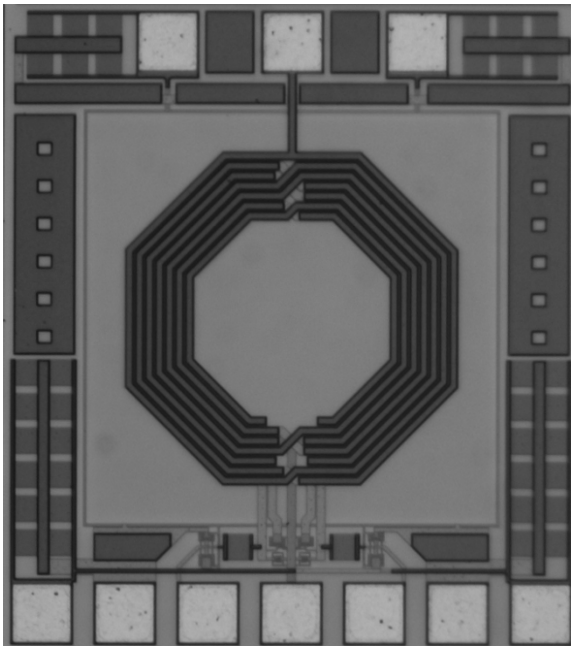

Fig. 5. Microphotograph of the VCO.

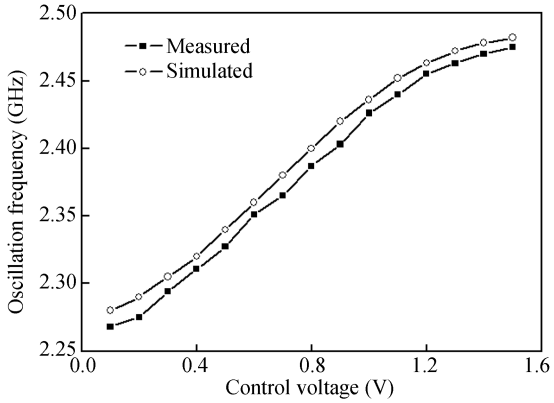

Fig. 6. Tuning range of the VCO.

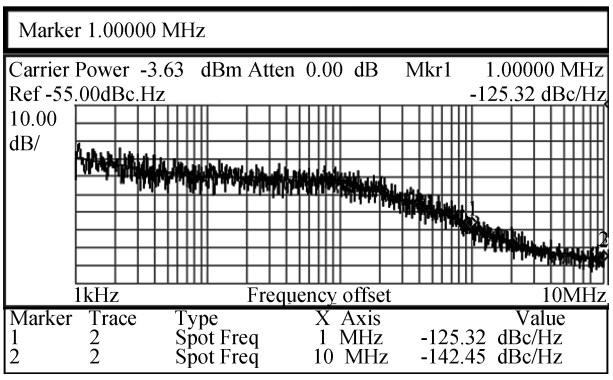

Fig. 7. Measured phase noise.

Table 2. Comparison of the most recent state-of-the-art low-power VCOs.

Parameter	Ref. [1]	Ref. [3]	Ref. [4]	This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Supply voltage (V)	0.9	0.45	0.5	0.4
Power (μW)	500	630	660	640
Oscillation frequency (GHz)	1.87	2.645	2.56	2.433
Tuning range (%)	7.8	8	18	8.7
Phase noise (dBc/Hz)	–111 @ 1 MHz	–106.4 @ 400 kHz	–120 @ 1 MHz	–125.3 @ 1 MHz
FOM (dB)	–180	–184.8	–192	–195

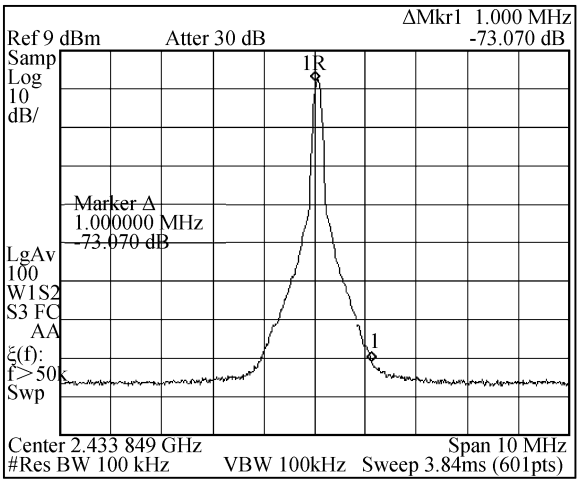

Fig. 8. Measured output spectrum of the VCO.

A figure of merit (FOM) has been defined to compare the VCO performances.

$$\mathrm{FOM} = L(f_0, \Delta f) + 10\lg\left\{\left(\frac{\Delta f}{f_0}\right)^2 \frac{P_{\mathrm{VCO}}}{[\mathrm{mW}]}\right\}, \quad (2)$$

where $L(f_0, \Delta f)$ is the single side band phase noise at the offset frequency Δf from the carrier frequency f_0. P_{VCO} denotes the total power consumption of the VCO. This results in an FOM of –195 dB for this design. Table 1 summarizes the performance of the most recent state-of-the-art low-power VCOs. It is obvious that the proposed VCO has the best FOM value and low phase noise compared to the published results in Refs. [1, 4] with about the same power consumption.

4. Conclusion

A 2.4-GHz ultra-low-power and low-phase-noise oscillator with transformer feedback is presented. The LC oscillator has been implemented in SMIC's 0.18-μm CMOS process. The measured results show the proposed oscillator can achieve a phase noise of –125.3 dBc/Hz at 1-MHz offset from a 2.433-GHz carrier with a power consumption of 640 μW under a 0.4-V supply. Such a VCO is potentially useful for WLAN 802.11b wireless applications.

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