A snap-shot mode cryogenic readout circuit for QWIP IR FPAs

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Abstract: The design and measurement of a snap-shot mode cryogenic readout circuit (ROIC) for GaAs/AlGaAs QWIP FPAs was reported. CTIA input circuits with pixel level built-in electronic injection transistors were proposed to test the chip before assembly with a detector array. Design optimization techniques for cryogenic and low power are analyzed. An experimental ROIC chip of a 128 × 128 array was fabricated in 0.35 μm CMOS technology. Measurements showed that the ROIC could operate at 77 K with low power dissipation of 35 mW. The chip has a pixel charge capacity of 2.57×10^6 electrons and transimpedance of 1.4×10^7 Ω. Measurements showed that the transimpedance non-uniformity was less than 5% with a 10 MHz readout speed and a 3.3 V supply voltage.

Key words: QWIP; ROIC; CTIA; cryogenic; transimpedance non-uniformity
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1. Introduction

Focal plane arrays (FPAs)[1] based on GaAs/AlGaAs quantum-well infrared photo-detectors (QWIP)[2] have become a promising choice for the development of high-resolution infrared imaging systems, due to their superior uniformity, yield, and radiation hardness. The high resolution requires the FPA to have a larger array format and smaller pixel size. As a result, the associated readout circuit should be realized in snap-shot mode which can ensure the frame rate in a large array. Moreover, the operation temperature of QWIP is usually 77 K (liquid nitrogen temperature, LNT) to suppress the dark current. So a cryogenic ROIC is required.

Readout integrated circuits (ROIC), typically realized in silicon CMOS, integrate the photocurrent generated by the detectors and multiplex all individual detector outputs in voltage modes. The ROIC is basically composed of four major components: pixel-level input circuits integrating the photocurrent into voltage, column-shared correlated double sample (CDS) circuits which sample the integrated voltage, an analog multiplexer to switch the sampled voltage to the output stage, and a high speed output buffer amplifier which provides high speed and high driving capability to output voltage. These components are illustrated in Fig. 1 which describes the signal flow in ROIC.

Usually, the ROIC should be tested before assembly to ensure that the non-uniformity of the transimpedance will meet the FPA requirements. One of the test methods is based on optical injection which utilizes the Si photodiodes within the ROIC as a current source. However, the detectivity of the Si photodiode is less than a QWIP, and thus this method is not convenient for testing the ROIC before assembly. Another method is using external electronic injection[3]. The injection current is generated from an external current source. However, this method is only available to the ROIC for line arrays or small FPAs. A new pre-assembly test method based on built-in electronic injection is introduced in this paper. Using the built-in electronic injection transistors in each pixel of the ROIC, the output voltage corresponding to certain injection currents can be obtained. Then the non-uniformity of the transimpedance will be mea-

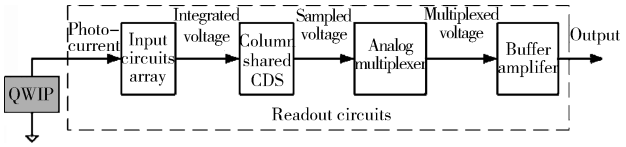

Fig. 1. Signal flow diagram of ROIC.

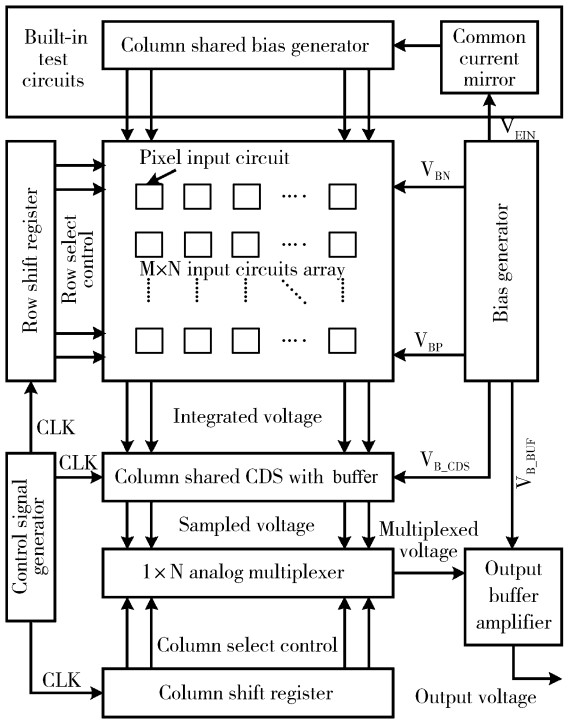

Fig. 2. Block diagram of snap-shot readout structure.

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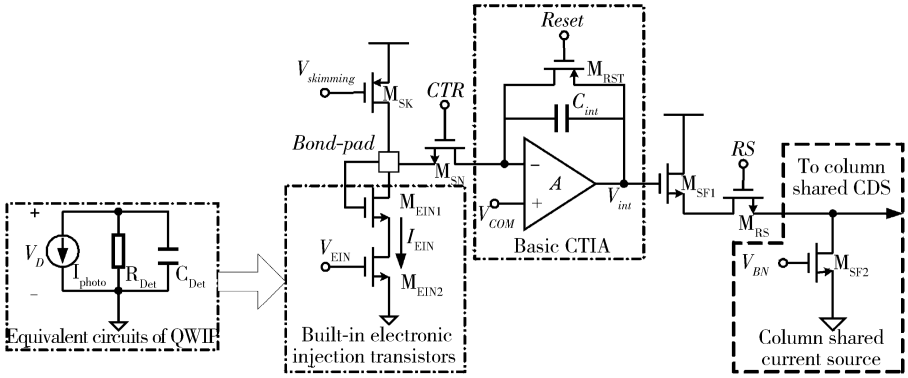

Fig. 3. Schematic of CTIA input circuit with built-in electronic injection transistors and QWIP model.

sured.

As mentioned above, the design and measurement of a snap-shot mode cryogenic readout circuit for QWIP FPAs are discussed in this paper. The circuit structure, readout strategy, and the design of each building block are described. The technique for cryogenic and low power optimization is also discussed. Measurements of the prototype chip are presented and analyzed. Finally, a conclusion is given.

2. Snap-shot mode ROIC for QWIP

Figure 2 shows a block diagram of the snap-shot mode readout structure with built-in test circuits. The input circuits, which are bonded to the detector using flip-bonding technology, skim the dark current and integrate the photocurrent at the capacitor in each pixel. After an integrating interval, the integrated voltages at the capacitors are switched one row at one time by row shift registers to a column-shared CDS, in which the integrated voltage is sampled. The sampled voltages are then multiplexed by the $1 \times N$ analog multiplexer, which is controlled by column shift registers, and are output serially to the common high speed output buffer amplifier. Built-in test circuits are employed to provide electronic injection current for the pre-assembly test of the ROIC. The detailed readout circuit structure and the operational principle of each element are described in this section.

2.1. Snap-shot mode input circuit array

For snap-shot readout circuits for QWIP FPA, to achieve high readout performance, the input circuits should have two basic functions, eliminating the dark current and integrating the photocurrent, which means the skimming[4] transistors and integrating capacitor should be in pixel input circuits. In addition, the input circuits also provide a stable bias voltage to the detector, especially for QWIP.

Many kinds of input scheme, such as direct injection (DI), buffered direct injection (BDI), source follower per detector (SFD), and capacitive trans-impedance amplifier (CTIA[5]), have become commonly used structures in IR FPA readout chips. However, due to the requirement of stable bias voltage on QWIP, CTIA is a better choice of input circuit than the others. Moreover, the Miller effect of the amplifier provides a higher equivalent capacitor value, which can improve the dynamic range and noise performance. Figure 3 shows the detailed schematic of CTIA with an equivalent QWIP circuit (for operation mode) and a built-in electronic injection transistor (for test mode).

The QWIP can be equivalent to the circuits illustrated in Fig. 3, where photocurrent is equivalent to current source $I_{\rm photo}$, and dark current $I_{\rm dark}$ can be expressed as

$$I_{\rm ph} = I_{\rm photo}, \tag{1}$$

$$I_{\rm dark} = V_{\rm D}/R_{\rm Det}, \tag{2}$$

where $R_{\rm Det}$ is the parasitic resistance of QWIP, and $V_{\rm D}$ is the detector bias voltage provided by the input circuits. The bond-pad is the interface between the detectors and the input circuits. The photocurrent and dark current, through the bond-pad, are injected into the input circuits where the dark current is skimmed by transistor MSN and photocurrent is integrated in capacitor $C_{\rm int}$. At time 0, the reset pulse Reset is low, the PMOS MRST is ON, the capacitor $C_{\rm int}$ is reset, and the voltage of the integrated node is reset to $V_{\rm com}$. When Reset and CTR are high, the device MRST is OFF and the photocurrent begins to integrate in $C_{\rm int}$. After a period of integration time $T_{\rm int}$, the voltage of the integrating node is increased to

$$V_{\rm int}(T_{\rm int}) = V_{\rm com} + (I_{\rm photo}T_{\rm int})/C_{\rm int}. \tag{3}$$

The voltage $V_{\rm int}(T_{\rm int})$ is then buffered by a source follower, which is composed of transistors MSF1 and MSF2, and is switched to the column-shared CDS through the MOS switch MRS controlled by a row select pulse RS.

When the ROIC is working in the test mode, the built-in electronic injection transistors implemented by MEIN1 and MEIN2 can generate current with the same magnitude as that of the photocurrent by setting MEIN2 operating in the subthreshold region[6]. The injection current $I_{\rm EIN}$ is proportional to the aspect ratio W/L and is exponential to bias voltage $V_{\rm EIN}$ and can be expressed as:

$$I_{\rm EIN} = \frac{W}{L} I_{\rm D0} {\rm e}^{(V_{\rm EIN}-V_{\rm T})/nV_{\rm t}}, \tag{4}$$

where $V_{\rm T}$ is the threshold voltage, $V_{\rm t} = KT/q$ is the thermal voltage and n is the subthreshold slope factor. The parameter $I_{\rm D0}$ is related to the transconductance and process parameters. The input circuit with built-in electronic injection was fabricated in 0.35 μm CMOS technology and was measured with different bias voltages $V_{\rm EIN}$ provided by the external voltage source. The injection current can be changed from 1 to 35 nA

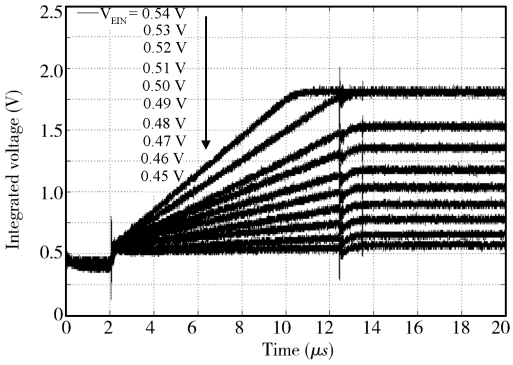

Fig. 4. Integrated voltage of CTIA with different V_{EIN} at 300 K.

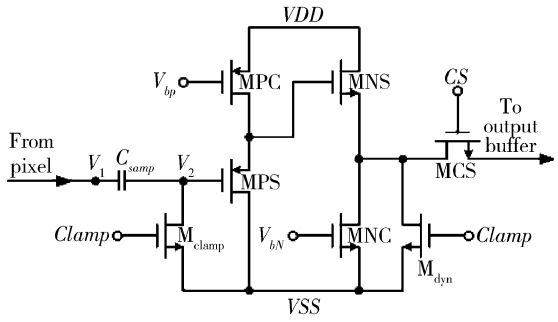

Fig. 5. Schematic of clamping CDS with dynamic discharging.

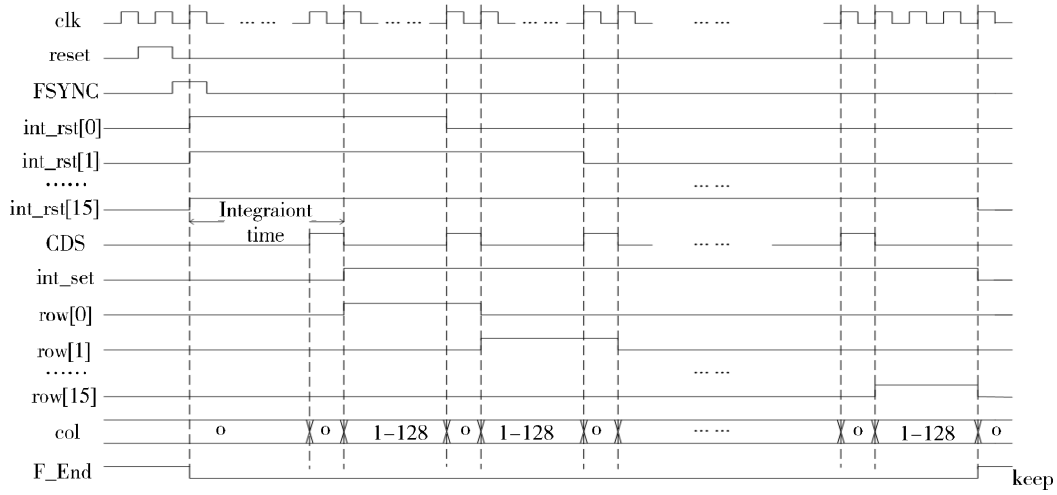

Fig. 6. Timing diagram of the ROIC.

by adjusting V_{EIN} from 450 to 540 mV. Figure 4 shows the measured integrated voltage curves on a 125 fF integrating capacitor with different bias voltages VEIN during 10 μs integrating time.

2.2. Column-shared CDS with buffer amplifier

The clamping CDS[7], shown in Fig. 5, is employed as the column-shared CDS of ROIC. The correlated double sampling function is realized by the sample capacitor C_{samp} and clamp transistor Mclamp. The kTC noise is less than that of common CDS circuits due to there being only one capacitor employed. The P type source follower and N type source follower form a complementary cascade source follower stage which can obtain a nearly zero dc offset by compensating their gate-source threshold voltage.

The sampled voltage from CDS is multiplexed, by the $1\times N$ analog multiplexer controlled by column shift registers, to the high bandwidth output buffer amplifier. To obtain a high output rate, the output buffer amplifier is designed to a 100 MHz gain bandwidth product and 85dB DC gain. The detector common voltage V_{com} is given by the off-chip regulator, and other dc bias voltage is given by the on-chip bias generator.

2.3. Operation of ROIC

Figure 6 shows the timing diagram of the main digital signals, the system clock CLK, system reset signal RESET, frame synchronization signal FSYNC, integrated capacitor reset signal INT_RST[0:127] for 128 rows, CDS sample clock CLAMP, row select signal ROW[0:127], column switch bus col[0:127], and frame readout end signal F_END. When FSYNC is high, the photocurrent begins to integrate on the capacitors in each pixel. After a period of integration time T_{int}, by switching the photocurrent off, the integrated voltage is kept on the capacitor and then multiplexed to CDS by switching on the first row select signal ROW[0]. When the integrated voltage is sampled, the integrating capacitor is reset immediately by switching the INT_RST to low, and the sampled voltage is multiplexed to the output buffer by switching the column select bus. When all pixels in the first row are read out, the second row select signal ROW[1] is high and then the integrated voltage of the second row is read out. After the 128th row is read out, the end-of-frame signal F_END is high which indicates that the first frame readout is complete.

3. Design optimization

Usually the QWIP FPA operates at liquid nitrogen temperature (77 K) to suppress the dark current. As a result, the ROIC should also operate in a cryogenic environment. Furthermore, the power dissipation of the ROIC should be small enough so as to minimize the background noise arising from heat generation. In this section, both design tricks for cryogenic ROIC and

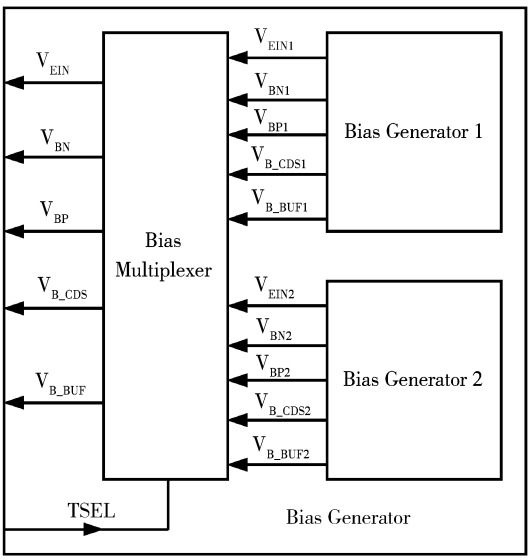

Fig. 7. Bias generation for a cryogenic ROIC compatible with RT.

low power optimization are discussed.

3.1. Design for cryogenic operation

Carrier mobility and threshold voltage are both temperature dependent; as the temperature is decreased from 300 to 77 K, the carrier mobility increases by a factor of 4–6 and the threshold voltage is increased about 0.2–0.4 V[8]. Another effect known as impurity freeze out begins to appear and limit performance at temperature below 100 K. At 77 K weak freeze out occurs which leads to the increase of parasitic resistance of LDD regions in MOS devices[9]. As temperature decreases from 300 to 77 K, the variations of the carrier mobility, threshold voltage V_{TH} and parasitic resistance (R_{LDD}) of LDD regions cannot be predicted by using the BSIM3 model due to the carriers being frozen out. These unpredictable variations make the design of the ROIC more complicated at liquid nitrogen temperature (LNT) than at room temperature (RT).

When operating at LNT, the performances of digital components in ROIC are improved due to faster switching speed and lower leakage. However, for the analog part, the traditional design method[10], such as 0.2 V overdrive voltage for MOS, is no longer suitable for cryogenic circuit design due to the increase of both V_{TH} and R_{LDD} at LNT. The bias voltages should be large enough to provide sufficient overdrive at 77 K. As a result, the output swing is decreased. Considering the worst case, the bias voltages of NMOS at LNT should be 0.4 V more than those at RT; however, the bias voltages of PMOS at LNT should be 0.4 V less than those at RT.

As illustrated in Fig. 7, the bias generator is composed of 3 blocks, two bias generators and a bias multiplexer. One set of bias voltages is provided by two bias generators, bias generator 1 for RT and bias generator 2 for LNT. The bias voltages for NMOS (or PMOS) from bias generator 2 are 0.4 V more (or less) than that of bias generator 1. The voltages from the two generators are multiplexed to the ROIC controlled by the temperature switch TSEL for RT and LNT separately.

By using this method, the input circuit with electronic injection was tested at LNT. Figure 8 shows the integrated voltages of CTIA with different V_{EIN} increasing from 0.7 to 0.75 V by 5 mV step. The integration time is 10 μs. Due to the increase of V_{TH} at LNT, the higher gate voltage should be put on V_{EIN} to produce the same magnitude of injection current at the RT. Compared with the integrated voltage at the RT shown in Fig. 4, the integrated voltage swing at LNT is 1.1 V which is 0.1 V less than that at RT because of higher V_{TH} and R_{LDD}. The smaller step means that the transconductance is increased at LNT due to higher carrier mobility.

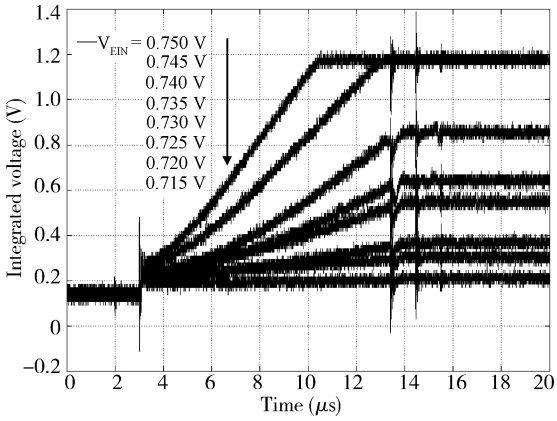

Fig. 8. Integrated voltage of CTIA with different V_{EIN} at 77 K.

The measurements verified the estimation of the integrating activity of CTIA at LNT. The multiplexed bias generator method has been proved to be applicable to a cryogenic ROIC.

3.2. Power optimization

Power dissipation is another important parameter of the ROIC. More power dissipation will generate more heat, and then produce more background current to the QWIP. It is significant for an ROIC to operate at low power dissipation in order to suppress background noise.

As the main component of an ROIC, the input circuit array consumes more than 90% of the total power. In the pixel level input circuit, more than 95% of the total power is consumed by the TIA. The optimization of the TIA for low power is the most efficient method of ROIC power optimization. Other than adopting the low power TIA discussed in section 2, another optimization method is power management.

Commonly, the ROIC operates in integrate-then-readout mode. Integrate-then-readout mode means that there are two operation stages for CTIA: integrate stage and readout stage. At the integrate stage, all 128 × 128 input circuits integrate the photocurrent. At the same time, the column-shared CDS with buffer amplifier and output buffer amplifier "take a break". At the readout stage, the integrated voltages of the array are read out to the column-shared CDS with the buffer amplifier row by row, and then to the output buffer amplifier column by column. When accomplishing the readout of one row, the input circuits on this row "take a break". The power management will shut down the power of the "idle" sub-circuits when they "take a break".

Table 1 shows the power distribution of the ROIC before and after power optimization. After optimization, the power dissipation of the ROIC is reduced to almost 57% of the power dissipation before optimization.

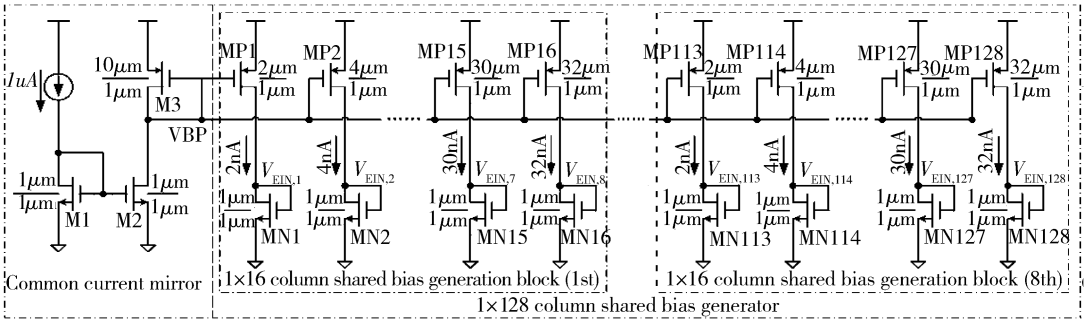

Fig. 9. Bias generator for 128 × 128 ROIC.

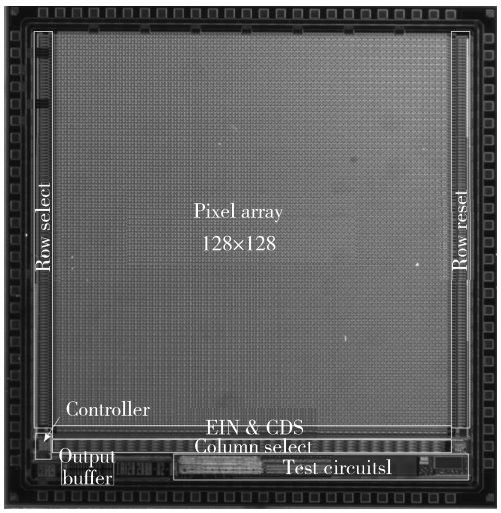

Fig. 10. Chip photograph of 128 × 128 ROIC.

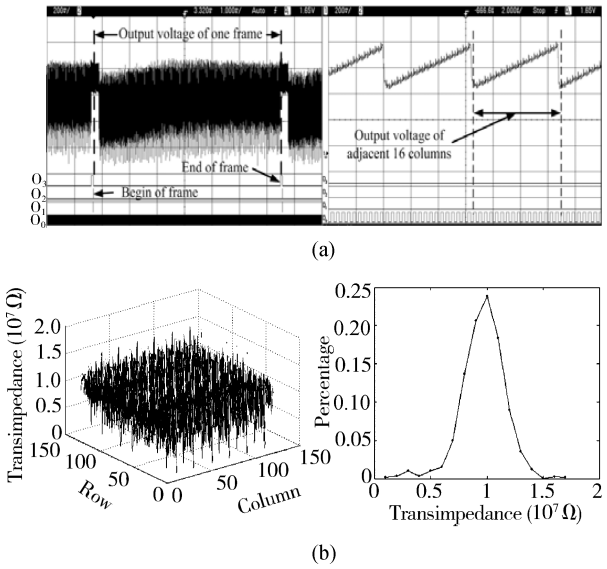

Fig. 11. Measurement and analysis of the experimental ROIC. (a) Output voltage in one frame (left) and in 16 column (right) (the voltage per division is 200 mV); (b) Transimpedance distribution in 2D (left) and statistically (right).

Table 1. Power distribution before and after power optimization. The unit is mW.

Sub-circuits	Before opt.	After opt.
Input circuit array	54.1	27.5
Column-share CDS with buffer amplifier	4.22	4.17
Output buffer amplifier	3.3	3270
Digital part	0.2	0.2
Full chip	61.82	35.14

4. Measurement

4.1. Biult-in test strategy for ROIC

In order to measure the transimpedance non-uniformity the bias voltage $V_{\rm EIN}$ should be generated in the ROIC. A 1 μA current reference and a 1 × 128 current mirror array were designed to provide bias voltages for electronic injection devices. Figure 9 shows the bias generator for a 128 × 128 ROIC. The current reference provides 1 μA current to M1 which operates in the subthreshold region because of its large width to length ratio, W/L. The common current mirror which is composed of M1–M3 transfers the current into 10 nA by setting the proper device ratio. The gate voltage $V_{\rm BP}$ of the self-biased M3 makes all PMOS be in the 1 × 128 column-shared bias generator working in the subthreshold region. The various test patterns can be generated by setting various widths of PMOS in the column-shared bias generator. To simplify the design, as illustrated in Fig. 9, the 1 × 128 bias generator can be constructed by combining eight similar 1 × 16 bias generation blocks. In each block, the drain current of PMOS increases from 2 to 32 nA from the first column to the 16$^{\rm th}$ column in steps of 2 nA. The self-biased NMOSs (MN1–MN128) provide bias voltage ($V_{\rm EIN1} - V_{\rm EIN128}$) to the electronic injection transistors (MEIN2 in Fig. 2) in the same column.

4.2. Measurement and analysis

A 128 × 128 experimental chip with built-in electronic injection has been fabricated in 0.35 μm CMOS technology. A chip photograph is shown in Fig. 10. The chip was tested at 3.3 V supply voltage and 10 MHz clock frequency. The measured output voltage curves of one frame and of 16 adjacent columns are illustrated in Fig. 11(a). The incremental output voltage of the adjacent 16 columns corresponding to the bias generation block shown in Fig. 9 is also shown in Fig. 11(a). The transimpedance non-uniformity can be tested by processing the sampled output voltage. Figure 11(b) shows the transimpedance distribution of the experimental chip in 2D and in a statistical way. Because of process variation and device mis-

Table 2. Summary of the test chip.

Parameter	Value
Array size	128 × 128
Chip area	4.9 × 4.9 mm^2
Pixel pitch	30 × 30 μm^2
Power dissipation	35.2 mW @ 50 fps and 3.3 V Vdd
Charge capacity	2.57 × 10^6 e$^-$ @ 125 fF integration capacitor
Transimpedance	1.4 × 10^7 Ω
Output voltage swing	1.1 V (0.1–1.2 V) @ 77 K
Integration time	10 μs

match, the transimpedance values of individual pixels are different from each other. The maximum transimpedance of 1.7 × 10^7 Ω occurs at the location where the row exchange happens. The typical value is 1.1 × 10^7 Ω, which is lower than the simulated result of 1.5 × 10^7 Ω because of the output voltage attenuation. As shown in Fig. 11(b), the transimpedance non-uniformity of the experimental chip is lower than 5%.

The chip performance is shown in Table 2. The chip area is 4.9 × 4.9 mm^2. The pixel size is 30 × 30 μm^2 and has a charge capacity of 2.57 × 10^6 electrons and a transimpedance of 1.4 × 10^7 Ω. The measurements show that the readout speed is 10 Mbps; the maximum frame rate is 640 frame/s for 128 × 128 FPAs under a 3.3 V supply voltage.

5. Conclusion

This paper reports the implementation of a snap-shot mode 128 × 128 cryogenic readout circuit for GaAs/AlGaAs QWIP FPAs. The ROIC fabricated in 0.35 μm CMOS technology has a 1.1 V output swing and 35.3 mW power dissipation at 77 K. The prototype chip is measured by using built-in electronic injection transistors. The measurements show that the transimpedance non-uniformity is less than 5%.

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