Design of an LDO with capacitor multiplier

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Abstract: This paper presents a low quiescent current, highly stable low-drop out (LDO) regulator. In order to reduce capacitor value and control frequency response peak, capacitor multipliers are adopted in the compensation circuit with mathematic calculations. The phase margin is adequate when the load current is 0.1 or 150 mA. Fabricated in an XFAB 0.6 μm CMOS process, the LDO produces 12.2 mV (0.7%) overshoot voltage while the current changes at 770 mA/100 μs with a capacitor load of 10 μF.

Key words: LDO; frequency compensation; capacitor multiplier; dynamic bias; buffer
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1. Introduction

As one of the most important power management modules, LDO can provide regulated low-noise and precision supply voltage for noise sensitive blocks. With the widespread proliferation modern portable devices, more stringent performance requirements of the LDO are proposed. First, fast load transient response with little output voltage variation, including overshoot and undershoot upon load switching, is critical to prevent an accidental turn off or resetting of the portable device. Secondly, low no-load quiescent current is required to reduce standby power. Finally, in order to save die size, a small compensation capacitor is also needed. The adoption of the external device is a common method for compensation. However, there are several difficulties. When load current increases, the dominant pole at the output of LDO moves to a higher frequency, which may cause stable problems. On the other hand, the variation of the ESR of the external capacitor can also make the phase margin (PM) worse. Another way is with internal compensation. Miller compensation is widely used here. Compared with the external compensation above, internal compensation is much more feasible. Due to the Miller splitting, a dominant pole and a non-dominant pole are created related to UGB. To get higher PM, the position of secondary non-dominant pole should be properly controlled. Because a lager load capacitor is used to inhibit overshoot and undershoot, the lager capacitor is implemented on a chip to make pole-splitting available. To get a better stability with a small compensation capacitor on chip, the capacitor multiplier is introduced in this paper to ensure the PM is always above 60° throughout the loading range. In addition, a dynamic bias buffer is used to enhance the transient response and reduce standby current.

2. Capacitor multiplier

Compared to the traditional voltage-mode Miller compensation, Figures 1 (a) and 1(b) illustrate the principle behind the current-mode counterpart of the multiplier.

The key of the concept is to sense the current flowing through the capacitor, multiply it by a factor greater than one ($K_x > 1$), and reapply it back to the same node by means of a current-controlled current source. The factor K_x can be achieved by current mirrors. The current through the capacitor C_c is $I_c = sV_{n1}C_c$ and the equivalent capacitance C_{eq} seen at node n1 is,

$$C_{eq} = \frac{I_{eq}}{sV_{n1}} = \frac{I_c + K_x I_c}{sV_{n1}} = (1 + K_x)C_c. \tag{1}$$

Figure 1 (c) shows a practical circuit of the current-mode capacitor multiplier described in Figs. 1(a) and 1(b), where factor y is the W/L of transistor Mn1. Transistor Mp1 is added to illustrate how the circuit is worked within the context of a gain stage. The current through capacitor C_c is sensed by transistor Mn1. Transistor Mn2 pulls an amplified version of the current from node n1. In a steady-state condition, Mn2 sinks the current required to bias Mp1 (DC current is equal to $K_x I_b$). During a transient condition, however, the current flowing through capacitor C_c is summed with current I_b and, therefore, sensed and ultimately multiplied by K_x. Transistor Mn1, while sensing the current, loads capacitor C_c with a diode-connected NMOS transistor and can be effectively treated as a series resistor $1/g_{Mn1}$. Due to the correlativity with the capacitor current and the dependence on frequency as well, the multiplier K_x is a factor affecting the frequency response of the equivalent capacitance. The dependence between K_x and frequency can be ascertained by deriving the relation for current I_c and substituting it back in the last equation derived for equivalent capacitance C_{eq}.

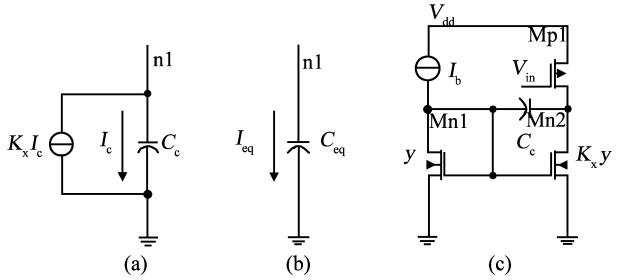

Fig. 1. Current-mode capacitor multiplier.

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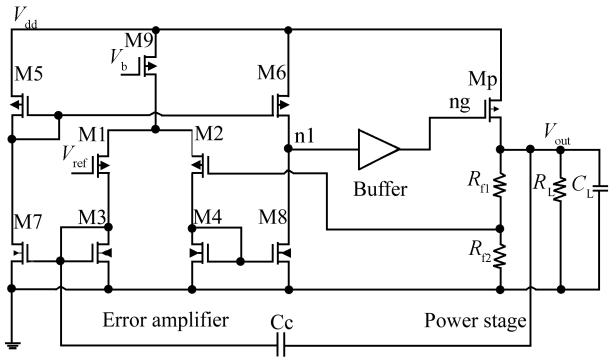

Fig. 2. LDO structure.

$$C_{eq} = \frac{I_c(1+K_x)}{sV_{n1}} = \frac{(V_{n1}-V_y)sC_c(1+K_x)}{sV_{n1}} = \frac{C_c(1+K_x)}{\frac{sC_c}{g_{Mn1}}+1}. \quad (2)$$

where V_y is the voltage at the gates of Mn1 and Mn2.

As it can be observed, the attenuating pole of the multiplication factor introduces an LHP (left half plane) zero in the overall response[1]. This zero lies at relatively high frequencies; however, it can be used to optimize frequency compensation.

3. Circuit design

An LDO circuit is applied in Fig. 2 with a capacitor multiplier.

The error amplifier (EA) is realized by M1–M9. The output stage consists of the power MOS 'Mp' and feedback resister R_{f1}–R_{f2}. A current buffer is inserted between EA and power stage. In EA, the W/L of M7–M8 is K_x times of that of M3–M4. Because of the capacitor multiplier, the capacitor between node n1 and V_{out} is Miller multiplied by K_x so as to compensate the LDO much easier to get a higher stability. The LDO can be compensated by this equivalent capacitor to get a higher stability.

3.1. Stability analysis

The equivalent small signal circuit is shown in Fig. 3. Device G1 is the EA, whose trans-conductor is g_{M1}; the device named 1x is buffer stage; the device G2 is the power stage, whose trans-conductor is g_{Mp}. The device Gc is the feedback stage, whose trans-conductor is g_{Mc}. The parasitic resister and capacitor at node n1 is r_{o1} and C_1. The resister and capacitor at V_{out} is R_L and C_L. In this circuit, Mp3 is connected as a diode to sample the feedback current, the $R_c = 1/g_{M3}$. Mp7 works as an amplifier to amplify the sampled signal. So $g_{Mc} = g_{M7}$.

The loop-gain transfer function can be derived from the following considerations.

(1) C_L, C_c are much larger than C_1;

(2) Trans-conductance g_{Mp} and output resistance R_L provide the gain of the pass device $A_{vp} = g_{Mp}R_L$, A_{vp} varies with the load current, particularly, is inversely proportional to I_L.

(3) $g_{Mc} = g_{M7} = K_x g_{M3}$.

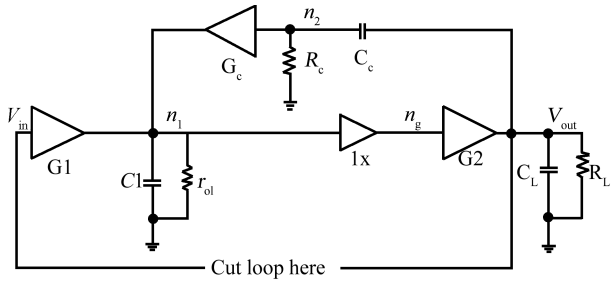

Fig. 3. Small signal circuit.

Apply KCL at node n1, V_{out}, n2:

$$\text{n1: } g_{M1}V_{in} + g_{Mc}V_{n2} = \frac{V_{n1}(1+sr_{o1}C_1)}{r_{o1}}, \quad (3)$$

$$V_{out}: -g_{Mp}V_{n1} = \frac{V_{out}(1+sR_LC_L)}{R_L} + \frac{V_{out}-V_{n2}}{\frac{1}{sC_c}}, \quad (4)$$

$$\text{n2: } \frac{V_{out}-V_{n2}}{\frac{1}{sC_c}} = \frac{V_{n2}}{R_C}. \quad (5)$$

The transfer function is:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{M1}r_{o1}g_{Mp}R_L(1+C_cs/g_{M3})}{1+as+bs^2+cs^3}, \quad (6)$$

where $a = R_L(C_L + K_x g_{Mp} r_{o1} C_c)$, $b = R_L C_L r_{o1} C_1$, $c = C_1 C_c C_L r_{o1} R_L / g_{M3}$.

The loop gain transfer function should be studied under different current load.

When $I_L = 0$, g_{Mp} is at its minimum and R_L is at its maximum. As a result, $R_L C_L \gg K_x g_{Mp} r_{o1} C_c R_L$, the transfer function can be approximated to

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{M1}r_{o1}g_{Mp}R_L(1+C_cs/g_{M3})}{1+(C_LR_L)s+(R_LC_Lr_{o1}C_1)s^2+(C_1C_cC_Lr_{o1}R_L/g_{M3})s^3} = \frac{1}{(1+R_LC_Ls)(1+r_{o1}C_{o1}s)}. \quad (7)$$

The pole-zero cancellation occurs here. So, there are two poles left. One is within UGB which is the dominant pole at node V_{out}; the other is outside of UGB.

When $I_L \gg 0$, g_{Mp} increases with I_L quickly, $K_x g_{Mp} r_{o1} C_c \gg C_L$. The transfer function can be approximated to

$$T(s) = \frac{V_{out}}{V_{in}} = -g_{M1}r_{o1}g_{Mp}R_L(1+C_cs/g_{M3}) \times \left[1+(K_xg_{Mp}C_LR_L)s+(R_LC_Lr_{o1}C_1)s^2 + (C_1C_cC_Lr_{o1}R_L/g_{M3})s^3\right]^{-1}. \quad (8)$$

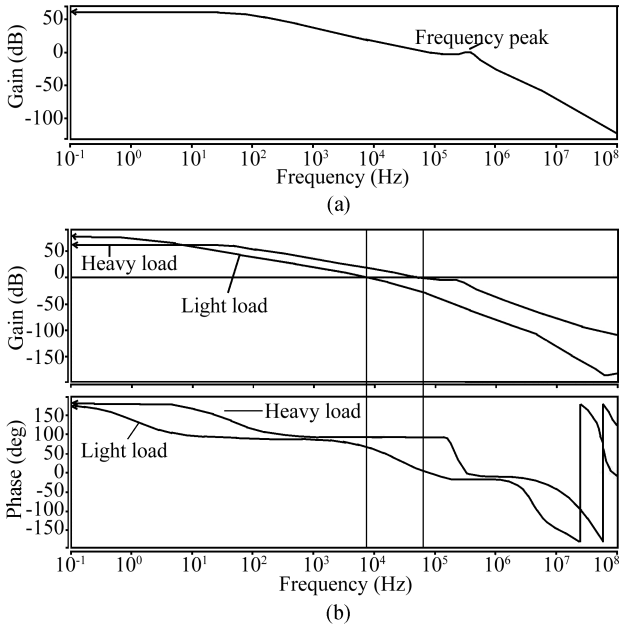

Fig. 4. (a) Frequency response with small damping factor. (b) Frequency response with different load currents.

There are one low-frequency pole and tow mid-frequency poles here in this function. So, the denominator can be displayed as

$$\left(1-\frac{s}{p_1}\right)(1+ds+es^2)=1-\frac{1}{p_1}s-\frac{d}{p_1}s-\frac{e}{p_1}s^3. \quad (9)$$

The transfer function (8) can be approximated to

$$T(s)=\frac{V_{\text{out}}}{V_{\text{in}}}=-g_{\text{M1}}r_{\text{o1}}g_{\text{Mp}}R_{\text{L}}\left(1+\frac{C_{\text{c}}}{g_{\text{M3}}}s\right)\times\left[\left(1+K_{\text{x}}g_{\text{Mp}}r_{\text{o1}}C_{\text{L}}R_{\text{L}}s\right)\times\left(1+\frac{C_{\text{L}}C_1}{K_{\text{x}}g_{\text{Mp}}C_{\text{c}}}s+\frac{C_1C_{\text{c}}C_{\text{L}}}{K_{\text{x}}g_{\text{Mp}}g_{\text{M3}}}s^2\right)\right]^{-1}. \quad (10)$$

As can be seen from above, the dominant pole is decreased to $1/K_{\text{x}}$ of that in the traditional Miller compensation. This pole can be set to a very low frequency easily to ensure the loop is stable. However, there are two other poles in this loop. The existence of the other two poles in this loop causes stable problems. One of the resolving ways is splitting them into two real poles with the system UGB decreases. The other way is to make these two poles as dual conjugate complex poles.

The damping factor of $1+ds+es^2$ in denominator is

$$\zeta=\sqrt{\frac{g_{\text{M3}}C_1C_{\text{L}}}{4K_{\text{x}}g_{\text{Mp}}C_{\text{c}}^2}}. \quad (11)$$

Because of the large g_{Mp} and K_{x} at heavy load $I_{\text{L}}\gg 0$, the damping factor is always small. The small damping factor will lead to a frequency peak on bode, which is shown in Fig. 4(a). The gain margin may be larger than –12 dB. As a result, the loop is not stable.

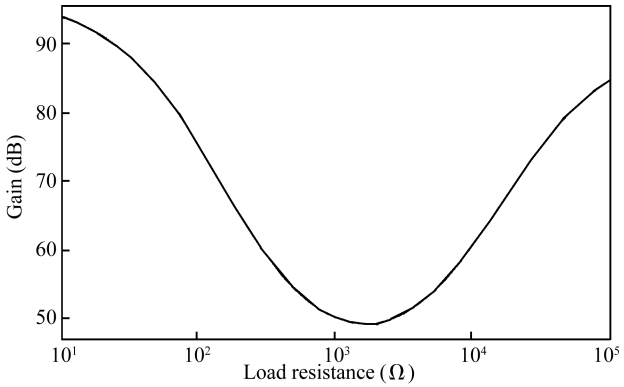

Fig. 5. Phase margin varies with load current.

Connect a compensation capacitor C_{c2} between node n1 and the gate of M8, so as to increase the equivalent capacitor C_1 at node n1 by capacitor multiplier. Accordingly, the damping factor is increased to eliminate the frequency peak. However, lager damping factor may slit these two complex poles into real poles and limit the UGB of LDO. For this, the damping factor can be set to $\zeta=1/\sqrt{2}$, and,

$$C_{\text{c}}=\sqrt{\frac{g_{\text{M3}}C_1C_{\text{L}}}{2K_{\text{x}}g_{\text{Mp}}}}. \quad (12)$$

C_1 is approximated to 10^{-1} pF dimension, and C_{L} is set to 10 μF to get small overshoot and undershoot. As a result, according to Eq. (12), C_{c} is around 20 pF. Comparing to nested Miller compensation, the compensation capacitor is decreased from 99 to 20 pF[4].

Run the open loop frequency feature simulation with $I_{\text{out}}=150$ mA and $I_{\text{out}}=0.1$ mA. The gain and phrase are shown in Fig. 4(b).

Seen from Fig. 4(b), when $I_{\text{out}}=150$ mA (heavy load), the open loop gain is 62.3 dB, PM is 93.2°, and gain margin (GM) is –14.5 dB. While $I_{\text{out}}=0.1$ mA (light load), the open loop gain is 77.1 dB, PM is 67.8°, GM is –32.5 dB.

In addition, Figure 5 shows the simulated PM of the loop-gain transfer function under different load currents. The minimum phase margin is always larger than 45° for the entire range of the load current.

This simulation result verifies that this structure is sufficient to ensure unconditionally stability under the full range of the load current. Especially, the PM and GM at typical using condition 0.1 mA and 150 mA both are better.

3.2. Circuit design

The whole LDO is shown in Fig. 6. The M1–M2 are the input gain stage of EA. The M3–M4 are used as load of M1–M2. M5–M8 translate differential signal into one port output. M10–M15 are used as current buffer. M10 is connected as source follow which can drive the gate of Mp efficiently. The dynamic feedback is implied by M11–M15.

The M13 is used as negative feedback MOS to reduce the resister at node ng. The voltage at the node is maintained by M13 when the current is changing with the load current at node ng.

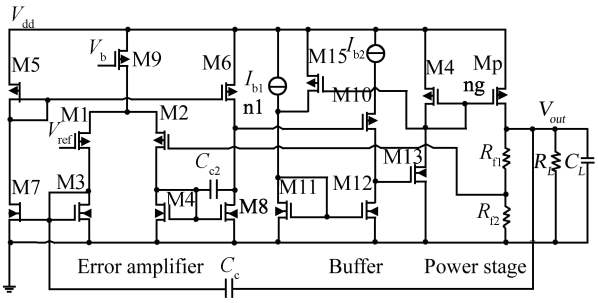

Fig. 6. LDO circuit.

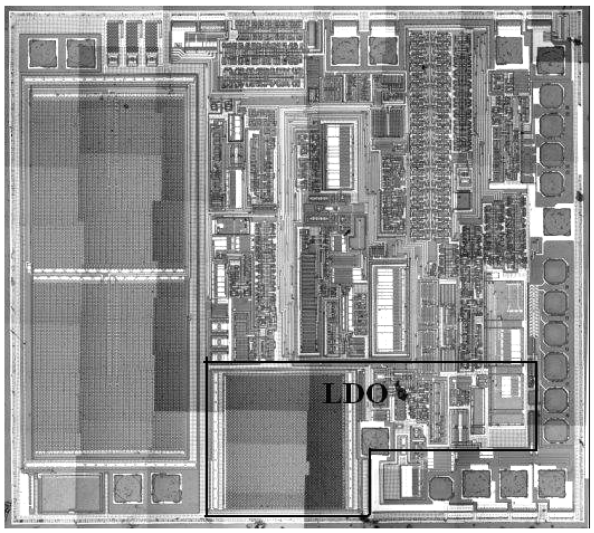

Fig. 7. Die photo of the chip.

Accordingly,the equivalent resistor of the source follow is lower by this feedback[3]. That is to say, the pole at node ng is pushed to a high frequency. However, the feedback bias current is low when the output current is low. So, the quiescent current can be set to 16 μA.

4. Results and discussions

In order to verify the proposed capacitor multiplier technique, the LDO shown in Fig. 6 was fabricated in the XFAB 0.6 μm CMOS process. Figure 7 shows the die micrograph of the proposed LDO, which was fabricated as part of an integrated power IC.

The LDO is used for converting power supplying voltage 3.3 to 1.8 V. And $V_{\rm ref} = 1.2$ V is used as a reference voltage. The output capacitor is $C_{\rm L} = 10$ μF. When $V_{\rm out} = 1.8$ V, the LDO can deliver 800 mA current. The transient response is shown in Fig. 8 when the load current is changing at 770 mA / 100 μs.

As shown above, the overshoot of the LDO is 12.2 mV (0.7%) when the load changing. The power reset curves are shown in Fig. 9.

5. Conclusions

The paper presents an LDO available on 3.3 V to compensation and dynamic current feedback buffer is adopted. After

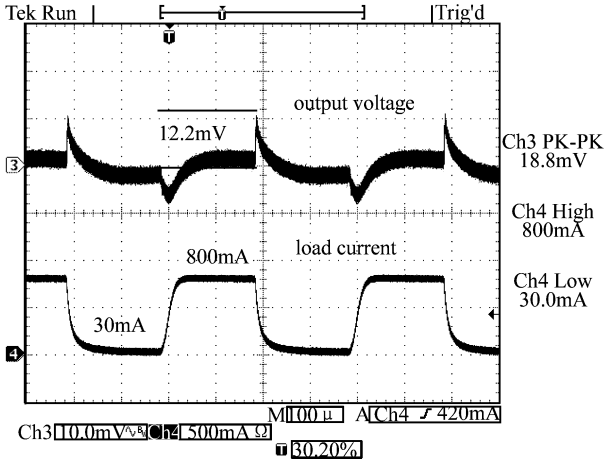

Fig. 8. Transient response.

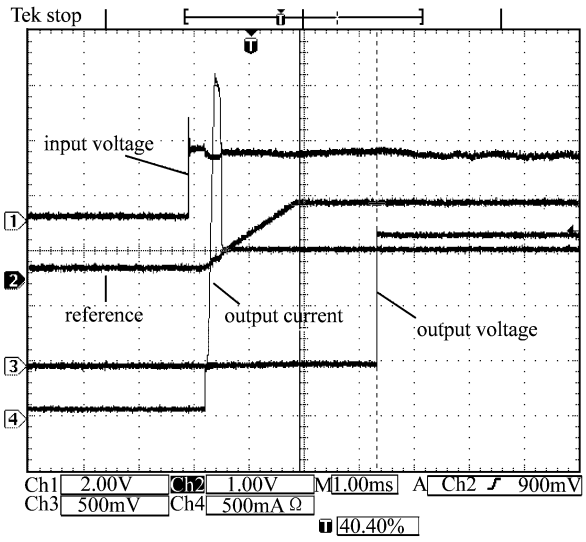

Fig. 9. Power reset.

introducing the principle of the capacitor multiplier, the loop stability of the compensated LDO is anglicized here with mathematic methods. The PM of the LDO is 67.8° with a light load and 93.2° with a heavy load after being compensated. The quiescent current is limited to 17 μA. And the max output current is up to 150 mA. The max overshoot is 12.2 mA (0.7%) when the load current is changing at 770 mA / 100 μs. The LDO can be used as a proper power supply.

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