A novel charge pump drive circuit for power MOSFETs*

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Abstract: Novel improved power metal oxide semiconductor field effect transistor (MOSFET) drive circuits are introduced. An anti-deadlock block is used in the P-channel power MOSFET drive circuit to avoid deadlocks and improve the transient response. An additional charging path is added to the N-channel power MOSFET drive circuit to enhance its drive capability and improve the transient response. The entire circuit is designed in a 0.6 μm BCD process and simulated with Cadence Spectre. Compared with traditional power MOSFET drive circuits, the simulation results show that improved P-channel power MOSFET drive circuit makes the rise time reduced from 60 to 14 ns, the fall time reduced from 240 to 30 ns, and its power dissipation reduced from 2 to 1 mW, while the improved N-channel power MOSFET drive circuit makes the rise time reduced from 360 to 27 ns and its power dissipation reduced from 1.1 to 0.8 mW.

Key words: charge pump; drive circuit; power MOSFET; transient response
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1. Introduction

For low cost, simple topology and no electromagnetic interference, charge pumps[1−4] can be found in wide applications of digital products. The design of the drive circuit has a significant influence on the performance of the charge pump. The transient response and drive capability are two important factors for power MOSFET drive circuits.

To meet the stringent transient response requirement, the switching frequency of the power converter should increase. At high-frequency applications, the effect of the gate drive circuit of the MOSFET on the overall performance of the converter becomes quite significant. As the switching frequency increases, the gate drive loss of the power MOSFET, which is proportional to the switching frequency, increases as well. So good transient response speed and drive capability are required for power MOSFET drive circuits. To this aim, much work has been done in the past[5, 6]. Resonant gate drive circuits that feature efficient energy recovery at both charging and discharging transitions are presented. Several driving circuits allowing the optimal feeding of the base of a cascade device are discussed. Some gate drive circuits[7−11] are proposed which not only save the gate drive loss but also reduce the switching loss.

However, these circuits are complicated or have intrinsic drawbacks. In this paper, novel power MOSFET drive circuits with simple structure are proposed and the operation principle is illustrated in detail. The new drive circuit can greatly improve the transient response and enhance the drive capability.

2. Principle of drive circuit

Figure 1 shows the charge pump topology. The DT block generates dead time, EA is the error amplifier, the V–I block converts the voltage signal into a current signal, and P_DRIVE and N_DRIVE are the P-channel power MOSFET drive circuit and N-channel power MOSFET drive circuit respectively. M1 is the P-channel power MOSFET, and M2 is the N-channel power MOSFET. For weak drive capabilities, the output signal of the EA cannot be used directly to drive a power MOSFET, and the signal needs to be modified first. The V–I block converts the output voltage of the EA into a current signal, then the current signal is turned into a voltage signal by P_DRIVE or N_DRIVE to drive the power MOSFET. The function of the drive circuit is to transfer signal and enhance drive capability.

3. Drive circuits of the charge pump

3.1. Traditional and improved drive circuits for a P-channel power MOSFET

Figure 2 shows a traditional P-channel power MOSFET drive circuit, where V_{DD} is the supply voltage, CLK is the clock

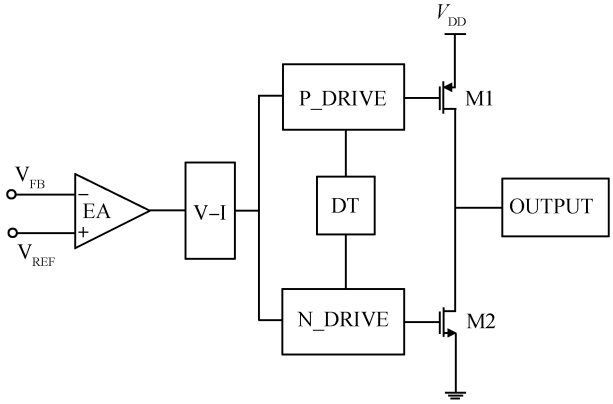

Fig. 1. Charge pump topology.

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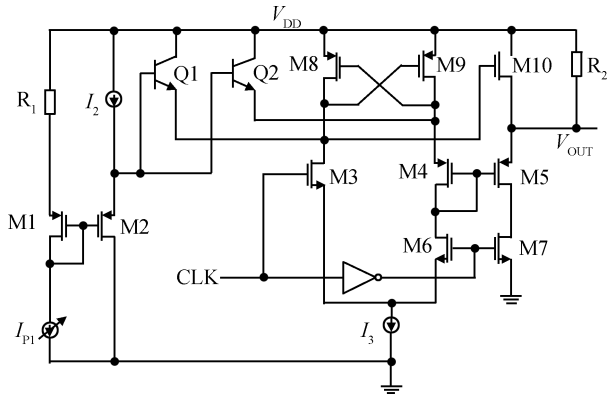

Fig. 2. Traditional drive circuit for a P-channel power MOSFET.

signal, V_{OUT} is the output of the drive circuit, and I_{P1} is the error current signal varying with the output of the EA.

$$V_{SM1} = V_{DD} - I_{P1}R_1, \tag{1}$$

where V_{SM1} is the source voltage of M1. Keep $V_{SGM1} \approx V_{SGM2}$, then:

$$V_{SM2} = V_{SM1} - V_{SGM1} + V_{SGM2} \approx V_{SM1}, \tag{2}$$

where V_{SGM1} and V_{SGM2} are the source–gate voltages of M1 and M2 respectively.

When CLK is high, M3 is conducting and M4–M7 are off. The drain voltage of M3 is pulled low, then M9, M10 and Q1 are turned on, and M8 is turned off. The P-channel power MOSFET M1 shown in Fig. 1 is turned off for the conduction of M10. Taking Eq. (2) into account, V_{DM3} can be calculated as:

$$V_{DM3} = V_{SM2} - V_{BEQ1} \approx V_{SM1} - V_{BEQ1}. \tag{3}$$

When CLK is low, M3 is off and M4–M7 are conducting, the source voltage of M4 will be pulled low, turning M8 and Q2 on. Then M9 and M10 are off. From Eq. (2), we can get:

$$V_{SM4} = V_{SM2} - V_{BEQ2} \approx V_{SM1} - V_{BEQ2}. \tag{4}$$

Provided $V_{SGM4} \approx V_{SGM5}$, then from Eqs. (1) and (4), V_{OUT} can be drawn as:

$$\begin{aligned} V_{OUT} &= V_{SM4} - V_{SGM4} + V_{SGM5} \\ &\approx V_{DD} - I_{P1}R_1 - V_{BEQ2}. \end{aligned} \tag{5}$$

Equation (5) indicates that V_{OUT} is linearly related to the error current signal I_{P1} when the P-channel power MOSFET is conducting.

As shown in Fig. 2, M8 and M9 are cross-couple connected, which can provide a positive feedback to accelerate the switching between the two operations described above. Besides, Q1 and Q2 are used for level shift and clamp.

However, the circuit shown in Fig. 2 has two disadvantages. The first is that a suitable frequency is difficult to choose, a large output ripple comes with a low frequency and deadlock comes with a high frequency. The second is that I_3 is hard to set. When I_3 increases, more power dissipation will be consumed. Besides, the base currents of Q1 and Q2 also depend on the variation of I_3. Once the sum of the base current is over I_2, there will no current injected to M2, then M2 is off and the circuit is out of operation. Generally, a small value of I_3 will be taken. However, the deadlock often comes out when the value of I_3 is small.

When CLK is low, if the discharge current across the path of M4, M6 is much smaller, the gate voltage of M8 cannot be pulled low rapidly and remains high, and the gate voltage of M9 remains low. M10 is conducting and V_{OUT} stays at a high level. When CLK turns high, V_{OUT} still stays at a high level, so the P-channel power MOSFET is off over the whole cycle, resulting in deadlock and abnormal operation.

To avoid the deadlock caused by high frequency or a small tail current I_3, an anti-deadlock block is added in Fig. 3. On the rising edge of CLK, no current flows through M11 and M13, but a large pulse current injects to M16 and M18. M16 and M17 constitute a current mirror, as well as M19 and M20. Thus the discharging current of M3 increases immediately, and the gate voltage of M9 decreases immediately. At same time, M10 is turned on rapidly, and the P-channel power MOSFET is turned off fast. Similarly, on the falling edge of CLK, M10 is turned off rapidly, and the P-channel power MOSFET is turned on immediately. The transient response speed of the output is accelerated, and the drive capability is enhanced. At the same transient response speed, the value of I_3 in the improved P-channel power MOSFET drive circuit can be set smaller, which reduces static power dissipation. Besides, the anti-deadlock block operates only on the rising or falling edge, so it has very low static power dissipation.

3.2. Traditional and improved drive circuits for an N-channel power MOSFET

A traditional drive circuit for an N-channel power MOSFET is shown in Fig. 4. V_{DD} is the supply voltage, I_{N1} is the error current signal, I_2 and I_3 are the constant current sources, CLK1 and CLK2 is a pair of reversed-phase clocks, and V_{OUT} is the output of the drive circuit.

It can be easily seen that:

$$V_{BQ1} = I_{N1}R_1. \tag{6}$$

When CLK2 is high and CLK1 is low, M1, M3 and M4 are all off. The N-channel power MOSFET M2 shown in Fig. 1 is turned off for the conduction of M5.

When CLK1 is on the rising edge and CLK2 is on the falling edge, M5 is turned off and M1–M4 are turned on. While V_{OUT} is low, Q2 is off. The current across M3 charges the gate capacitance of the N-channel power MOSFET, the gate voltage increases. When it attains a threshold, Q2 conducts. Provided $V_{BEQ1} \approx V_{BEQ2}$, from Eq. (6), V_{OUT} can be calculated as:

$$V_{OUT} = V_{BQ2} + V_{BEQ2} \approx V_{BQ1} = I_{N1}R_1. \tag{7}$$

From Eq. (7), it can be easily seen that V_{OUT} varies linearly with I_{N1}. So the gate voltage of the N-channel power MOSFET could be controlled effectively by the error current signal I_{N1}.

The circuit shown in Fig. 4 has a disadvantage. When V_{OUT} is changed from low to high, the gate capacitance is charged through the path of M2, M3. If the current in this path is small, it will increase the rise time. So an improved N-channel power MOSFET drive circuit is shown in Fig. 5. Another charging path is added for increasing the charging current and reducing the rise time.

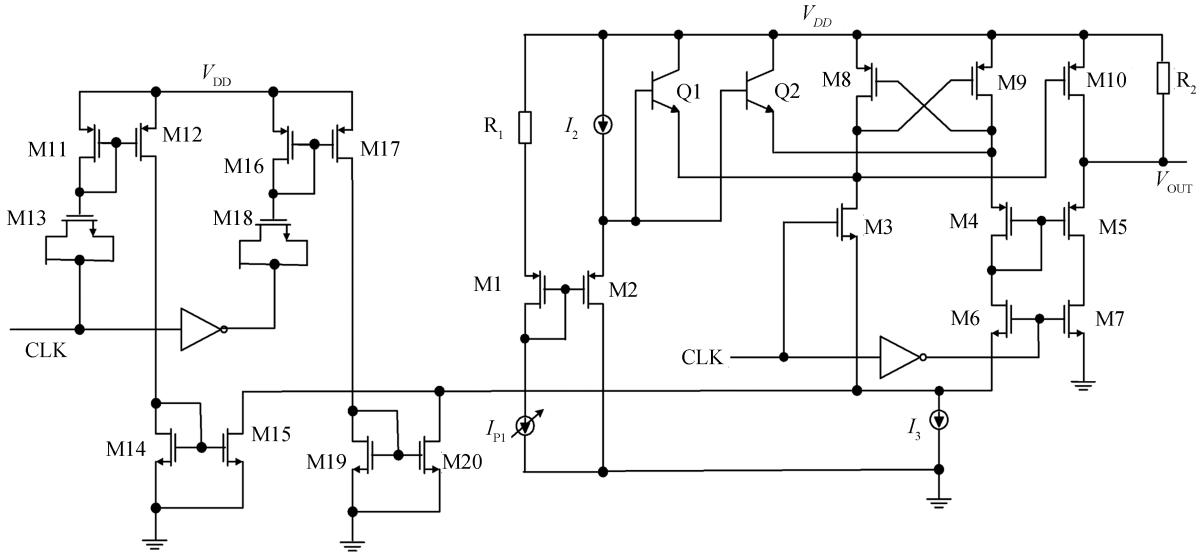

Fig. 3. Improved drive circuit for a P-channel power MOSFET.

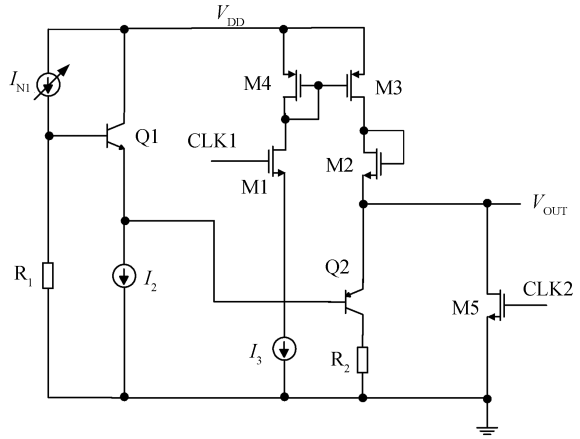

Fig. 4. Traditional drive circuit for an N-channel power MOSFET.

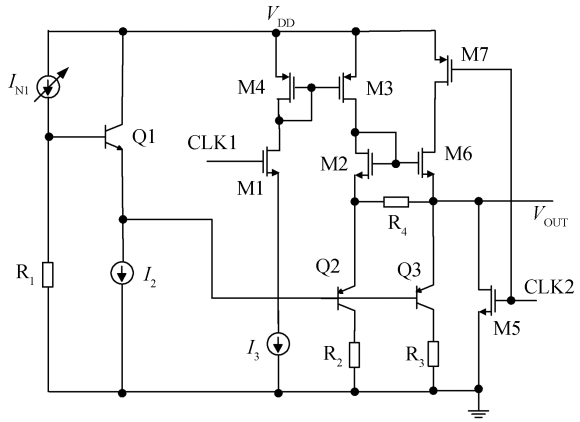

Fig. 5. Improved drive circuit for an N-channel power MOSFET.

When CLK1 is on the rising edge and CLK2 is on the falling edge, while V_{OUT} is low, Q2, Q3 are turned off. The gate capacitance is charged by the current I_{M2} across M2. For

$$V_{GSM6} = V_{GSM2} + I_{M2}R_4, \tag{8}$$

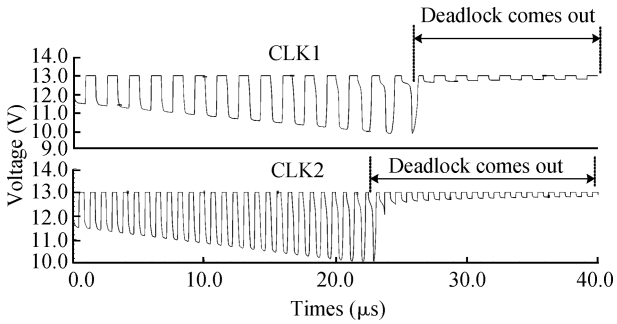

Fig. 6. Variation of deadlock with frequency for a P-channel power MOSFET.

it can be induced that $I_{M6} > I_{M2}$ (M7 operates in the deep triode region). I_{M6} will also charge the gate capacitance, so the drive capability will be enhanced. At the same transient response speed, the value of I_3 in the improved N-channel power MOSFET drive circuit can be set smaller than that in a traditional N-channel power MOSFET drive circuit, which can reduce the static power dissipation. When V_{OUT} attains a threshold, Q3 conducts and Q2 conducts later, then I_{M2} and I_{M6} flow through Q2 and Q3 respectively. V_{OUT} will be clamped when Q2 and Q3 are turned on. Provided $V_{BEQ1} \approx V_{BEQ3}$, V_{OUT} can be calculated as:

$$\begin{aligned} V_{OUT} &= V_{BQ3} + V_{BEQ3} = V_{BQ1} - V_{BEQ1} + V_{BEQ3} \\ &\approx V_{BQ1} = I_{N1}R_1. \end{aligned} \tag{9}$$

4. Experimental results

4.1. Simulation Results

The entire circuit is designed in a 0.6 μm BCD process and simulated with Cadence Spectre. The simulation results are varied with I_{P1} or I_{N1} which increase linearly with time.

In Fig. 6, $f_{CLK2} = 2f_{CLK1}$. It can be seen that the output can not be controlled effectively by I_{P1} when it gets to a thresh-

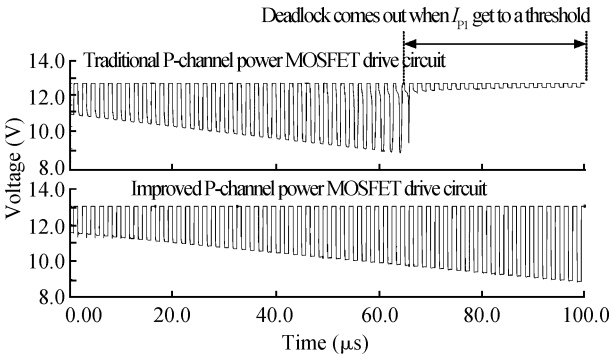

Fig. 7. Variation of output for a P-channel power MOSFET.

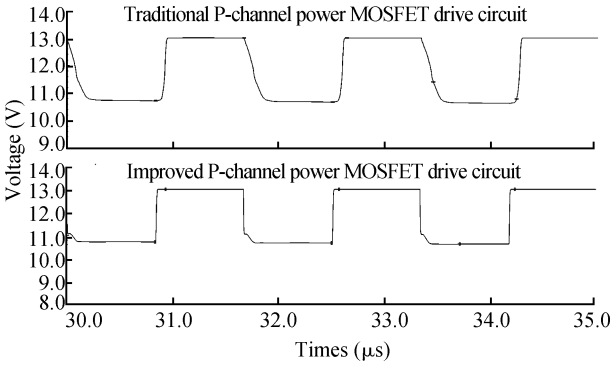

Fig. 8. Transient response of drive circuit for a P-channel power MOSFET.

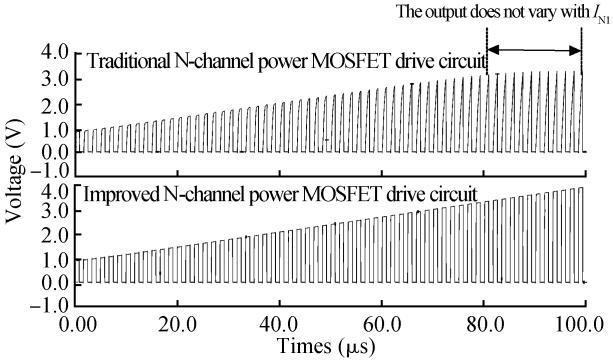

Fig. 9. Variation of output for an N-channel power MOSFET.

old, and the deadlock comes out. A deadlock is more likely to appear at a higher frequency.

Figure 7 shows the outputs of traditional and improved P-channel power MOSFET drive circuits. It can be observed that the improved drive circuit not only avoids deadlocks but also enhances the drive capability.

Figure 8 shows the transient response of the traditional and improved P-channel power MOSFET drive circuits. It can be seen that the improved drive circuit has a better transient response.

Figure 9 shows the outputs of traditional and improved N-channel power MOSFET drive circuits. It can be obtained that the improved drive circuit has a better drive capability.

Figure 10 shows the transient response of traditional and improved N-channel power MOSFET drive circuits. It can be seen that the improved drive circuit has a better transient response.

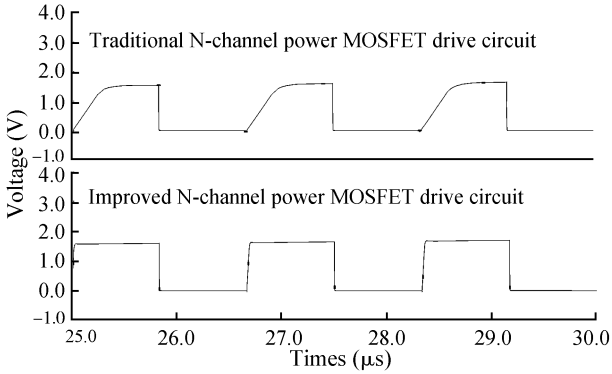

Fig. 10. Transient response of drive circuit for an N-channel power MOSFET.

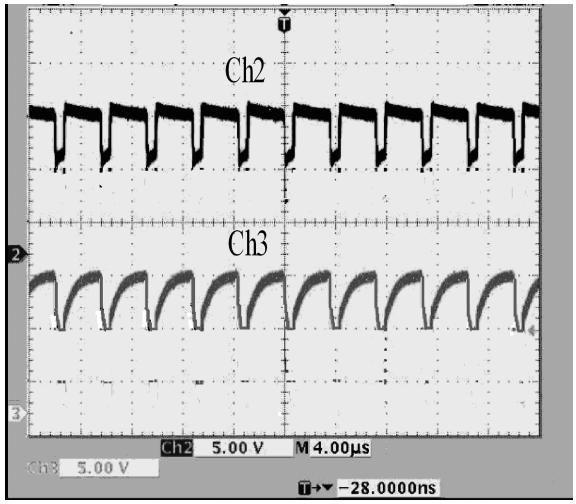

Fig. 11. Test result of traditional and improved drive circuit for a P-channel power MOSFET.

4.2. Test results

To verify the simulation, traditional and improved drive circuits are tested, and the results are shown in Figs. 11 and 12. They are tested in $V_{DD} = 13$ V, $T_A = 25$ °C, $I_{LOAD} = 60$ mA. Ch2 is the output of the improved drive circuit and Ch3 is the output of the traditional drive circuit. The test results are given in Table 1, showing that the improved drive circuits have better performance.

As shown in Fig. 11, it can be seen that the rise time in Ch2 is less than that in Ch3, so Ch2 has better transient characteristics than Ch3. The transient characteristics can be improved by increasing the tail current I_3, but the static power dissipation increases as the tail current I_3. Transient characteristics can be also improved by increasing $\frac{W_{20}/L_{20}}{W_{19}/L_{19}}$ or $\frac{W_{17}/L_{17}}{W_{16}/L_{16}}$, as well as $\frac{W_{15}/L_{15}}{W_{14}/L_{14}}$ or $\frac{W_{12}/L_{12}}{W_{11}/L_{11}}$. This method is often chosen. The anti-deadlock block operates only on the rising or falling edge, so it has very low static power dissipation.

It can be seen that Ch2 has better transient characteristics than Ch3 in Fig. 12. The transient response can be improved by increasing R_3, but it does not change significantly when R_3 increases to a certain value.

Additionally, the transient characteristics are affected by

Table 1. Characteristics of power MOSFET drive circuits.

Power MOSFET drive circuits		Rise time (ns)	Fall time (ns)	Power dissipation (mW)
P-channel	Traditional	60	240	2
	Improved	14	30	1
N-channel	Traditional	360	5	1.1
	Improved	27	5	0.8

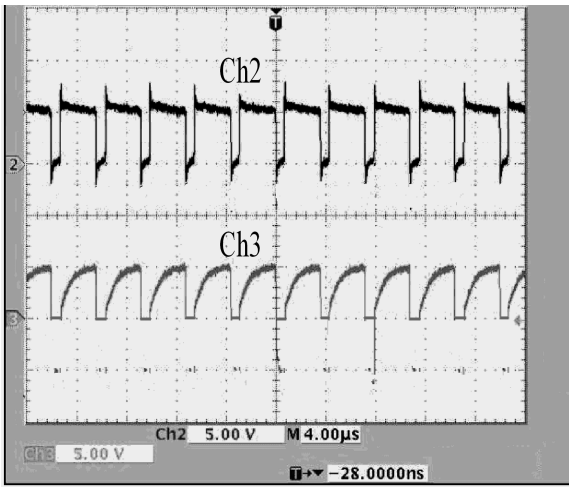

Fig. 12. Test result of traditional and improved drive circuit for an N-channel power MOSFET.

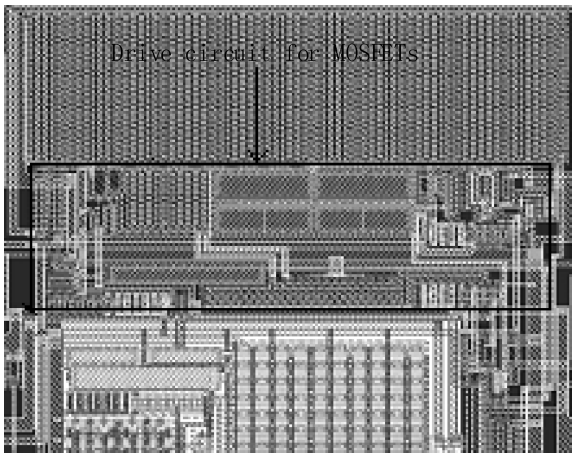

Fig. 13. Layout design of the proposed power MOSFET drive circuit.

the error current in P-channel and N-channel power MOSFET drive circuits. Greater the error current is, better the transient characteristic is. But the static power dissipation increases as the error current.

Characteristics of power MOSFET drive circuits are shown in Table 1. For the drive capability is improved, it has better transient response and less power dissipation.

The proposed power MOSFET drive circuit is fabricated in a 0.6 μm BCD process. The layout of the circuit is shown in Fig. 13. The drive circuit area is 300×100 μm^2.

5. Conclusion

Analyzing traditional power MOSFET drive circuits and their disadvantages, a novel P-channel power MOSFET drive circuit and a novel N-channel power MOSFET drive circuit are proposed. The entire circuits are designed in a 0.6 μm BCD process and simulated with Cadence Spectre.

Simulation results demonstrate that the improved P-channel power MOSFET drive circuit can not only enhance the transient response but also avoid deadlocks. The improved N-channel power MOSFET drive circuit enhances the drive capability and improves the transient response. Compared with the traditional power MOSFET drive circuits, the improved P-channel power MOSFET drive circuit makes the rise time reduced from 60 to 14 ns, the fall time reduced from 240 to 30 ns, and its power dissipation reduced from 2 to 1 mW. The improved N-channel power MOSFET drive circuit makes the rise time reduced from 360 to 27 ns and its power dissipation reduced from 1.1 to 0.8 mW. For its good characteristics, the drive circuit proposed in this paper can be widely used in charge pump and other voltage converters.

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