A 0.18 μm CMOS 3–5 GHz broadband flat gain low noise amplifier*

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Abstract: A 3–5 GHz broadband flat gain differential low noise amplifier (LNA) is designed for the impulse radio ultra-wideband (IR-UWB) system. The gain-flatten technique is adopted in this UWB LNA. Serial and shunt peaking techniques are used to achieve broadband input matching and large gain-bandwidth product (GBW). Feedback networks are introduced to further extend the bandwidth and diminish the gain fluctuations. The prototype is fabricated in the SMIC 0.18 μm RF CMOS process. Measurement results show a 3-dB gain bandwidth of 2.4–5.5 GHz with a maximum power gain of 13.2 dB. The excellent gain flatness is achieved with $\pm$0.45 dB gain fluctuations across 3–5 GHz and the minimum noise figure (NF) is 3.2 dB over 2.5–5 GHz. This circuit also shows an excellent input matching characteristic with the measured S_{11} below –13 dB over 2.9–5.4 GHz. The input-referred 1-dB compression point (IP1dB) is –11.7 dBm at 5 GHz. The differential circuit consumes 9.6 mA current from a supply of 1.8 V.

Key words: LNA; differential; UWB; flat gain; feedback
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1. Introduction

Ultra-wide band (UWB) technology is considered as a means of short distance wireless communication for high speed data transmission[1]. Recently, UWB communications have become the primary topic of interest for the research and industry communities, because of their potential to offer high data rates, low-power transmission and low power dissipation. This UWB LNA is designed for the IR-UWB zero-IF receiver system shown in Fig. 1.

After optional band pass filtering and amplification, the received 3–5 GHz signal is fed to two I/Q mixers. The local oscillator frequency 4 GHz is equal to the received center frequency and, consequently, the received signal is directly converted to baseband.

Design of the UWB LNA over 3–5 GHz is critical to the UWB receiver, as it should achieve high gain, good gain flatness, low noise figure, low return loss and good linearity over a bandwidth of as much as 2 GHz. There are several existing approaches for this ultra-wideband low noise amplifier. Distributed amplifiers can bring the GBW to a value close to the device f_T, but consume large power and area. Resistive shunt feedback amplifiers[2] provide good wideband matching and flat gain, but tend to suffer from a poor noise figure (NF) and large power dissipation. A multi-section LC ladder matching network has been proposed to achieve wideband matching, low noise figure, and low power consumption simultaneously[4]. However, the adoption of LC of the filter at the input mandates a number of reactive elements, which could lead to a larger chip area and NF degradation.

In the designs of ultra-wideband amplifiers, all of the known approaches give the gain flatness top priority over other performance aspects, and this severely limits the design flexibility, resulting in suppressed trade-off space for the gain, noise and power consumption requirements. In this work, the method of realizing flat gain is discussed in detail. By using serial and shunt peaking techniques in an RC-negative feedback topology, wideband input impedance matching and large GBW are achieved. This paper gives a detailed report on the design and analysis of this flat gain UWB LNA.

2. UWB LNA architecture

The proposed UWB LNA is shown in Fig. 2, and all components in the figure are integrated on-chip. Transistors M1 and M2 are placed in the deep N-well (DNW) region, so the source and bulk terminals can be connected together to eliminate the noise currents generated from the body effect. Devices in DNW also show a better isolation from substrate noise coupling. The inductor L_g, capacitors C_1, C_{pad}, C_{gs} of M1 and the Miller effect of R_f at the gate of M1 form input serial-peaking networks to achieve wideband impedance matching. The inductor L_{load}, parasitic capacitor C_{out} and resistor R_{load} form the shunt-peaking load to achieve a large GBW. The feedback network composed of R_f and C_f is used to further extend the bandwidth and reduce the gain fluctuations. The source follower composed of M3 and M4 is added as the output buffer for the measurement.

Although the power consumption and area are larger than those of a single-ended circuit, differential topology is adopted

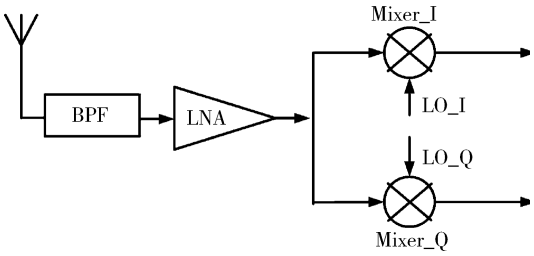

Fig. 1. Topology of the zero-IF UWB receiver.

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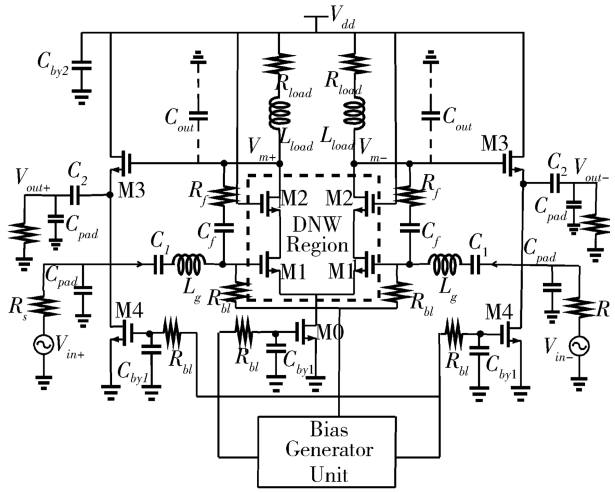

Fig. 2. Complete schematic of the proposed UWB LNA

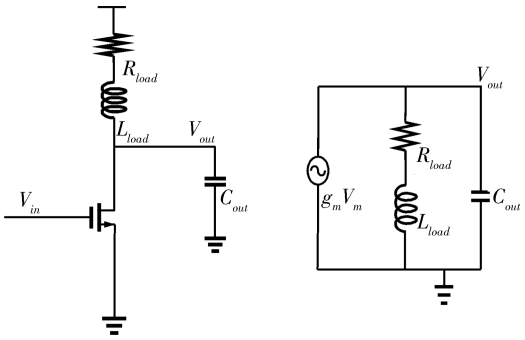

Fig. 3. Complete schematic of the proposed UWB LNA

due to its obvious advantages. It shows much higher immunity to the common mode noise. Also, the second-order nonlinearity (IIP2) is very detrimental in zero-IF receivers, and differential circuits have a better rejection to it.

3. Circuit design and analysis

3.1. Flat gain analysis

The shunt peaking technique shown in Fig. 3 is introduced in Ref. [14]. This technique enhances the bandwidth of the amplifier by transforming the frequency response from that of a single pole to one with two poles and a zero.

$$A_1(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{g_{\text{m}}(R + sL)}{1 + sRC + s^2LC}. \tag{1}$$

The zero is determined solely by the L/R time constant and is primarily responsible for the bandwidth enhancement. The frequency response of this shunt-peaked amplifier is characterized by the ratio of the L/R and RC time constants. This ratio is denoted by m so that $L = mR^2C$.

Figure 4 illustrates the frequency response of the shunt-peaked amplifier for various values of m. The case with no shunt peaking (m = 0) is used as the reference so that its low-frequency gain and its (3-dB bandwidth) are equal to one (RC = 1 and $g_{\text{m}}R$ = 1). As expected, the 3-dB bandwidth increases as m increases. The maximum bandwidth is obtained when m = 0.71 and yields an 85% improvement in bandwidth. However, as can be clearly seen in the magnitude plot, this comes at the cost of significant gain peaking. The maximally flat response can be obtained for m = 0.41, and the bandwidth still has an impressive improvement of 72%. So in the design of the wideband flat gain LNA, m is optimized to set around 0.41.

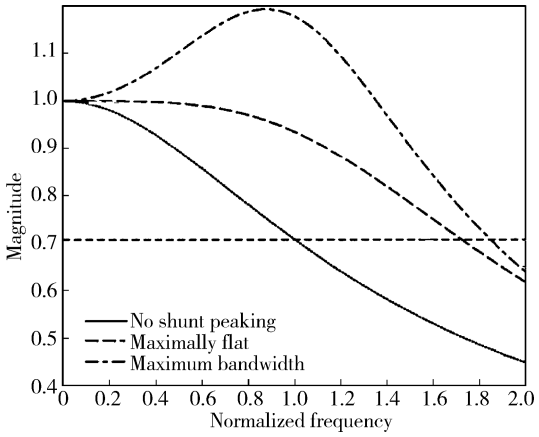

Fig. 4. Frequency response of shunt-peaked load.

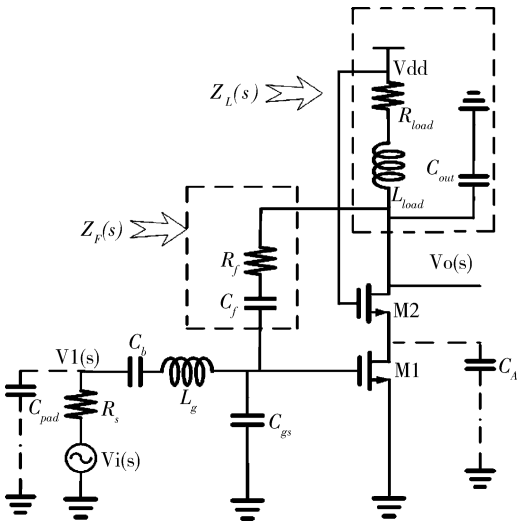

Fig. 5. Circuit for gain analysis without buffer.

However, this bandwidth extension method is still not large enough to achieve a bandwidth as large as 2 GHz with very small gain variation. Feedback networks composed of resistor R_{f} and AC-coupling capacitor C_{f} are introduced to further extend the bandwidth as Figure 5 shows. Due to the negative feedback, the whole amplifier possesses an attenuated sensitivity to changes in the forward gain, and the distortions in the circuit are greatly decreased.

The closed-loop gain of Fig. 5 can be expressed as follows (on the condition of perfect input matching):

$$A(s) = A_1(s)A_0(s) = \frac{V_1(s)}{V_{\text{i}}(s)}\frac{V_{\text{o}}(s)}{V_1(s)} \tag{2}$$

$$= \frac{1}{2}\frac{Z_{\text{L}}(s)Z_{\text{F}}(s)[1 - g_{\text{m}}Z_{\text{F}}(s)]}{C(s) - B(s)}, \tag{3}$$

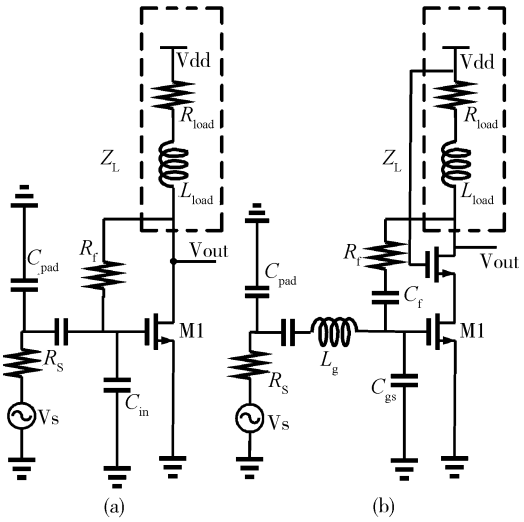

Fig. 6. Input matching circuit comparisons: (a) Conventional circuit; (b) Improved circuit.

where

$$C(s) = (s^2 L_g C_{gs} Z_F(s) + sL_g + Z_F(s))(Z_L(s) + Z_F(s)), \quad (4)$$

$$B(s) = Z_L(s)(1 - g_m Z_F(s))sL_g, \quad (5)$$

$$Z_L(s) = (R_{load} + sL_{load})//(1/sC_{out}), \quad (6)$$

$$Z_F(s) = R_f + 1/sC_f. \quad (7)$$

It can be seen that the presence of feedback, along with the presence of input matching networks and parasitic capacitance, results in a more complex frequency response compared to the single-zero, double-pole system described earlier. Nevertheless, the simple treatment discussed earlier serves as an excellent starting point.

3.2. Wideband input matching analysis

The circuit topology of a conventional resistive shunt feedback LNA is shown in Fig. 6(a). The input impedance is a parallel combination of C_{all} and $R_F/(1 + A)$, where the latter must be set equal to $R_S(50\ \Omega)$ for the matching requirement. To achieve an input reflection coefficient of –10 dB at 5 GHz, the maximum tolerable C_{all} can be derived as $C_{all} = 1/(\pi R_S f \sqrt{|\Gamma|^2/(1-|\Gamma|^2)}) \cong 400$ fF[6], where C_{all} is the sum of the parasitic capacitance of pads C_{pad} and the source-gate capacitances of M1 C_{in}. To satisfy this requirement with a CMOS amplifier while achieving sufficient gain, a low noise figure and low power consumption is very difficult.

A serial peaking inductor is used at the input to enhance the input wideband matching characteristic shown in Fig. 6(b). The inductor L_g can tolerate a larger size of M1 which means a higher g_m can be obtained. Also, the adding of the inductor also benefits the higher gain and lower noise figure.

Figure 7 is the small-signal equivalent circuit of Fig. 6(b). The effects of all transistor parasitic elements, except the input capacitance C_{gs} of M1, are assumed to be negligible (the Miller effect of C_{gd} of M1 can be neglected due to the cascode topology). With these assumptions the input impedance of Fig. 7 can

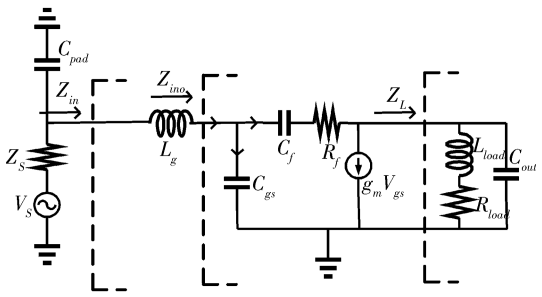

Fig. 7. Small-signal equivalent circuit of input networks.

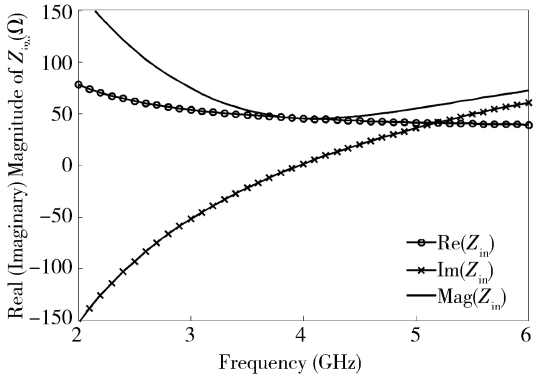

Fig. 8. Input impedance of Z_{in}.

be expressed as:

$$Z_{ino}(s) = \frac{1 + \dfrac{Z_L(s)}{Z_F(s)}}{sC_{gs} + \dfrac{Z_L(s)}{Z_F(s)}\left(sC_{gs} + \dfrac{1}{Z_L(s)} + g_m\right)}. \quad (8)$$

With the assumption of $g_m \omega L_{load} \gg 1$, $R_f \gg \omega L_{load}$, Equation (8) can be rewritten as:

$$Z_{ino} = \{Z_F(s) + g_m \omega^2 L_{load}^2 - j[\omega Z_F^2(s) C_{gs} + \omega Z_F(s) \times g_m L_{load}]\} / \{(1 - \omega^2 L_{load} C_{gs})^2 + \omega^2 [Z_F(s) C_{gs} + g_m L_{load}]^2\}. \quad (9)$$

When the imaginary part of the Z_{ino} is chosen to resonate with inductor L_g at the frequency of interest (ω_0), input matching can be obtained by making the input source resistance equivalent to the real part of the Z_{ino}, as follows:

$$\omega_0 = \frac{1}{2\pi \sqrt{L_g I_m(Z_{ino})}}. \quad (10)$$

and

$$R_s = R_e(Z_{ino}), \quad (11)$$

$$Z_{in}(j\omega) = j\omega L_g + Z_{ino}(j\omega). \quad (12)$$

After extracting the necessary parameters from the circuit, the curves of $Z_{in}(j\omega)$ are plotted by Matlab as Figure 8 shows. It can be seen that the real part of Z_{in} remains very close to 50 Ω from 3 to 5 GHz, while the impedance of the imaginary part is zero near 4 GHz, and the magnitude of Z_{in} remains not far from 50 Ω, which means that a wideband input matching condition is achieved.

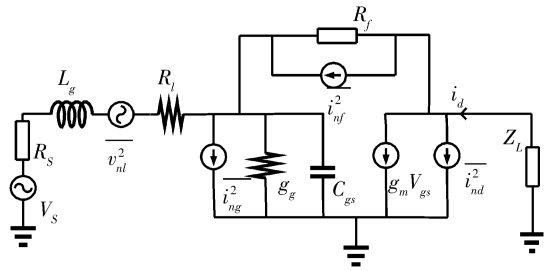

Fig. 9. Equivalent circuit of shunt-feedback amplifier for noise analysis.

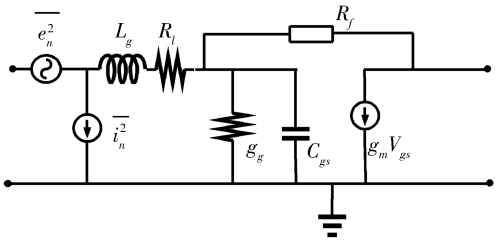

Fig. 10. Two-port noise model of the shunt-feedback amplifier.

3.3. Noise analysis

From Fig. 2, the noise arising from the bias generation unit is isolated from the RF signal path by the large resistors $R_{\rm bl}$ and bypassed to the ground by the decoupling capacitors $C_{\rm by1}$. The noise generated from the power supply is bypassed to the ground through $C_{\rm by2}$. Thermal channel noise from M2 would worsen the circuit noise figure at higher frequencies because the parasitic capacitances represented by $C_{\rm A}$ shown in Fig. 5 decrease the effective impedance at the source terminal of M2, so the size of M2 and M1 cannot be selected too large so as to resist this effect. The thermal noise from the tail current M0 is common mode noise and can be reduced by the differential circuit topology. Based on the analysis above, the small-signal noise circuit is shown in Fig. 9.

$\overline{i_{\rm nd}^2}$ represents the mean-square drain noise current and it can be expressed as:

$$\overline{i_{\rm nd}^2} = 4kT\gamma g_{\rm d0}\Delta f, \tag{13}$$

where $g_{\rm d0}$ is the drain-source conductance at zero $V_{\rm ds}$. The parameter γ is a bias-dependent factor.

$\overline{i_{\rm ng}^2}$ is used to model the gate-induced noise at saturation, and is given by:

$$\overline{i_{\rm ng}^2} = 4kT\delta g_{\rm g}\Delta f, \tag{14}$$

where $g_{\rm g} = \omega^2 C_{\rm gs}^2/5g_{\rm d0}$ and δ is the gate noise coefficient.

$R_{\rm l}$ represents the series resistance of the inductor $L_{\rm g}$, and the noise is represented by $\overline{V_{\rm nl}^2}$,

$$\overline{V_{\rm nl}^2} = 4kTR_{\rm l}\Delta f. \tag{15}$$

$\overline{i_{\rm nf}^2}$ represents the noise of the feedback resistor $R_{\rm f}$, and can be expressed as :

$$\overline{i_{\rm nf}^2} = \frac{4kT}{R_{\rm f}}\Delta f. \tag{16}$$

All the internal noise sources of the amplifier can be represented in a two-port noise model[8] as shown in Fig. 10. The mean-square of the input referred noise voltage and current is given as:

$$\overline{e_{\rm n}^2} = (\frac{4kT\gamma g_{\rm d0}}{g_{\rm m}^2} + 4kTR_{\rm l})\Delta f, \tag{17}$$

$$\overline{i_{\rm n}^2} = \overline{i_{\rm ng}^2} + (j\omega C_{\rm gs})^2\overline{e_{\rm n}^2} + \frac{\overline{e_{\rm n}^2}}{R_{\rm f}^2} + \frac{4kT\Delta f}{R_{\rm f}}. \tag{18}$$

In general, the noise voltage and current sources are correlated. The correlation admittance $Y_{\rm c}$ can be found as

$$Y_{\rm c} = \frac{1}{R_{\rm f}} + j\omega C_{\rm gs}\left(1 + \alpha\,|c|\sqrt{\frac{\delta}{5\gamma}}\right), \tag{19}$$

where

$$c = \frac{\overline{i_{\rm ng}i_{\rm nd}^*}}{\sqrt{\overline{i_{\rm ng}^2 i_{\rm nd}^2}}}, \tag{20}$$

$$\alpha = \frac{g_{\rm m}}{g_{\rm d0}}. \tag{21}$$

Based on the two-port noise model, the four noise figure parameters of the shunt-feedback CMOS amplifier can be derived as [7]:

$$R_{\rm n} = \frac{\gamma g_{\rm do}}{g_{\rm m}^2} + R_{\rm l}, \tag{22}$$

$$G_{\rm opt} \cong \frac{g_{\rm m}}{g_{\rm do}}\sqrt{\frac{\delta(1-|c|^2)\omega_2 C_{\rm gs}^2}{5\gamma} + \frac{g_{\rm do}}{\gamma R_{\rm f}}}, \tag{23}$$

$$B_{\rm opt} = -\omega C_{\rm gs}\left(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right), \tag{24}$$

$$F_{\rm min} = 1 + 2\left[\sqrt{\frac{\delta(1-|c|^2)\gamma}{5}\left(\frac{\omega}{\omega_{\rm T}}\right)^2 + \frac{\gamma g_{\rm d0}}{g_{\rm m}^2 R_{\rm f}}} + \frac{\gamma g_{\rm d0}}{g_{\rm m}^2 R_{\rm f}}\right]. \tag{25}$$

So the noise factor can be expressed as:

$$F = F_{\rm min} + \frac{R_{\rm n}}{G_{\rm s}}\left[(G_{\rm s} - G_{\rm opt})^2 + (B_{\rm s} - B_{\rm opt})^2\right]. \tag{26}$$

Equations (23) and (24) show that shunt feedback will change only the conductance of the optimal input noise matching admittance. From Eq. (25), the shunt feedback resistor $R_{\rm f}$ will increase the amplifier minimum noise figure. However, the feedback resistance is usually pretty large so the noise added to the amplifier is limited. The large value of $R_{\rm f}$ will also result in little deviation of the $G_{\rm opt}$ of the amplifier from the value without feedback. The thermal noise from inductor $L_{\rm g}$ is added to the input signal directly, so the Q-factor of $L_{\rm g}$ is kept as high as possible in the design. Thermal noises generated by the gate resistor are not shown, and can be decreased with proper layout techniques.

In summary, the purpose of LNA input matching design lies in enhancing the gain and minimizing the noise figure. The shunt feedback provides a way to achieve a better design tradeoff between the gain and noise characteristics of the broadband CMOS LNA.

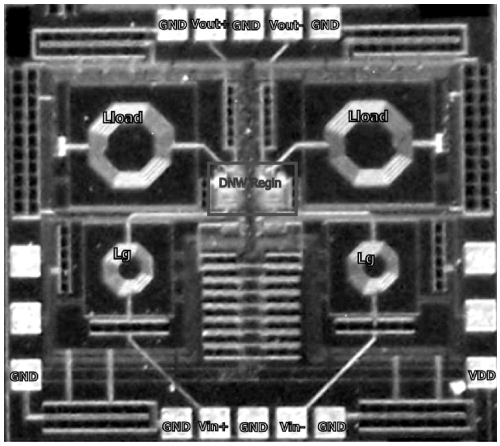

Fig. 11. Chip microphotograph.

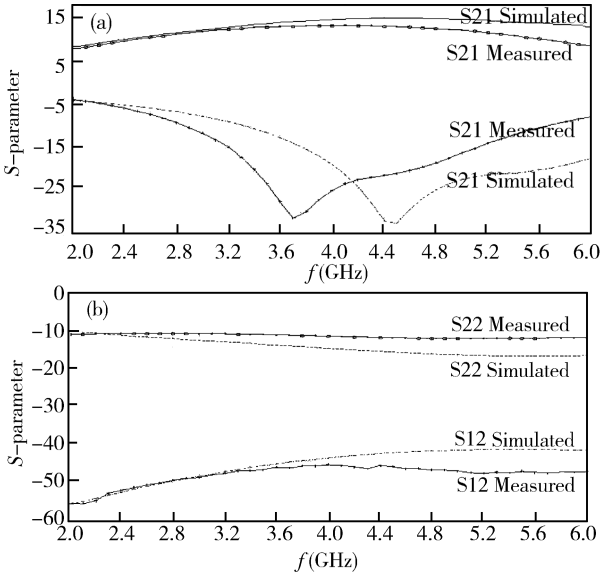

Fig. 12. Measured and simulated S-parameter.

4. Measurement results and analysis

The wideband differential LNA is fabricated in the SMIC 0.18 μm RFCMOS process. A microphotograph of this UWB LNA, which occupies an area of 0.7×1.0 mm^2, is shown in Fig. 11.

The S-parameter is simulated with Cadence SpectreRF and measured by an Agilent 8722ES vector network analyzer on the probe station of a SUMMIT Model 11000. The comparisons between measured and simulated results are shown in Fig. 12.

From Fig. 12, the measured S_{21} achieves a maximum of 13.2 dB with a good gain flatness of $\pm$0.45 dB from 3 to 5 GHz which shows the effectiveness of the design method proposed. The reason why the measured gain is lower than the simulated one is due to the lower self-resonating frequency and Q-factor of the inductor after tape out. This has been taken into consideration, and some design margins are given in simulation. The input return loss S_{11} remains better than –13 dB across 2.9–5.4 GHz due to the improved input matching networks. The output return loss S_{22} remains better than –10 dB from 2 to 6 GHz.

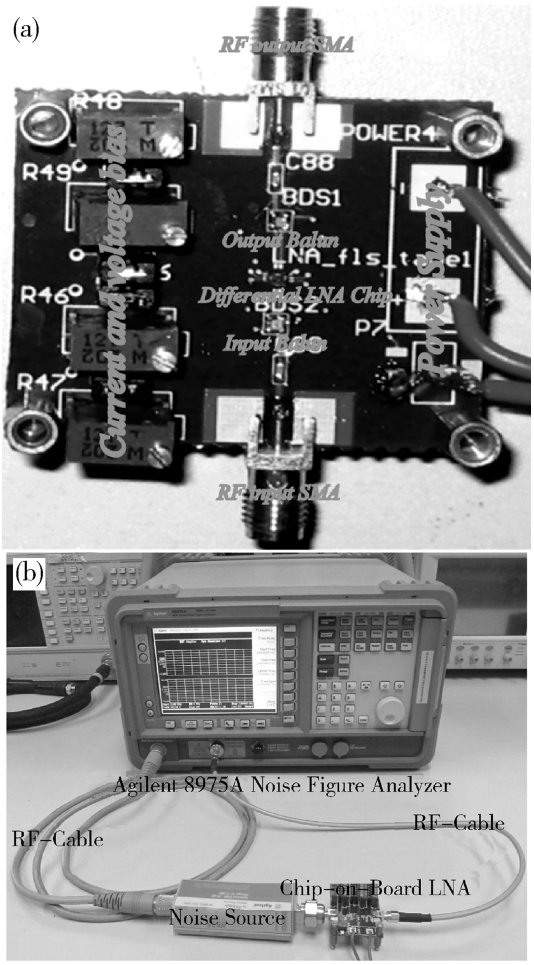

Fig. 13. Method of noise figure measurement.

The measured reverse isolation S_{12} is below –45 dB across 2–6 GHz which indicates the good stability performance of the circuit.

The noise figure is measured by an Agilent 8975A noise figure analyzer on an FR-4 PCB test board (COB) as Figure 13 shows. If the total insertion loss (dB) of the passive balun is loss_{in} and loss_{out} for the input and output terminal of the LNA, then the noise figure of the LNA can be calculated from the following cascaded formula[11]:

$$\text{NF}_{\text{cas}} = \text{NF}_1 + \frac{\text{NF}_2 - 1}{G_1} + \frac{\text{NF}_3 - 1}{G_1 G_2}, \tag{27}$$

where $\text{NF}_1 = \text{loss}_{\text{in}}$, $G_1 = 1/\text{loss}_{\text{in}}$, $\text{NF}_3 = \text{loss}_{\text{out}}$, $G_3 = 1/\text{loss}_{\text{out}}$ (from the formula of the passive microwave component), while $\text{NF}_2 = \text{NF}_{\text{LNA}}$ and $G_2 = G_{\text{LNA}}$. We can then get[12]:

$$\text{NF}_{\text{LNA,dB}} \approx \text{NF}_{\text{cas,dB}} - \text{loss}_{\text{in,dB}}. \tag{28}$$

The type of the wideband passive balun is BD3150N50100 with 0.6 dB insertion loss. The simulated, measured and measured after de-embedding noise figures are shown together in Fig. 14. The measured noise figure after de-embedding is 3.2–5.5 dB across 3–5 GHz. The difference between the simulated and measured NF at high frequency probably results from the lower Q-factors of the inductors than in the simulation and

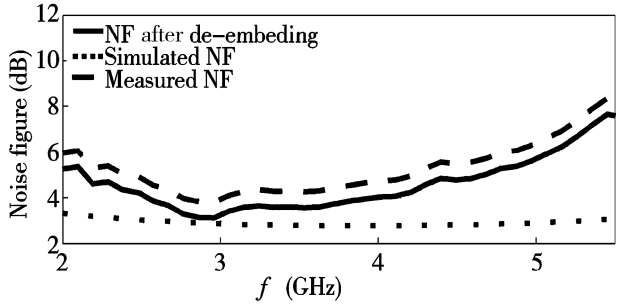

Fig. 14. Measured and simulated noise figures.

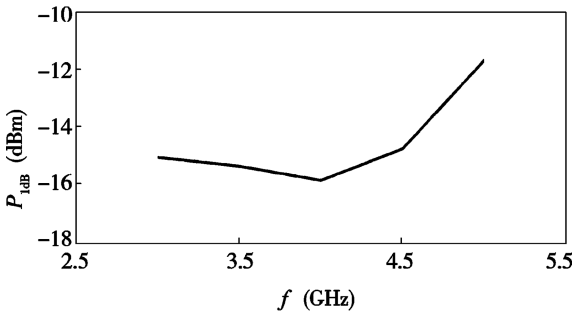

Fig. 15. Measured input 1dB compression point.

Table 1. Comparison of wideband LNA.

Reference	Gain flatness (dB) (BW∼GHz)	NF (dB) (BW∼GHz)	BW $_{3dB}$ (GHz)	Max gain (dB)	S_{11}	IP1dB (dBm)	Power consumption (mW)	Technology	Year
Ref. [3]	±1.5 (2.0–4.6)	2.3–5.2[a] (2.0–5.0)	2.0–4.6	9.8 [b]	< −8.2	–11.8	14 @ 1.8V[c]	0.18 CMOS	2005
Ref. [11]	±0.4 (3.1–5.2)	3.4–5.0 (2.4–5.2)	2.0–6.0	18.2	< −10	–17	39.6 @ 1.8 V	0.18 CMOS	2005
Ref. [9]	±1.3 (3.0–5.0)	5.0–5.3 (3.0–5.0)	3.0–5.0	14	< −10	–19.3	16.4 @ 1.8 V[c]	0.18 CMOS	2005
Ref. [10]	±1.5 (2.0–4.6)	3.5–5.4 (3.1–5.0)	2.0–4.6	9.5[b]	< −10	–10.4	16.5 @ 1.5 V	0.13 CMOS	2006
Ref. [13]	±1.4 (3.1–10.6)	2.3±0.43 (3.1–10.6)	3.1–10.6	15.1	< −9.9	–14.7	9 @ 1.2 V[c]	0.13 CMOS	2007
Ref. [15]	±0.9 (3.0–5.0)	4.7–5.0 (3.0–5.0)	2.0–5.3	11.5	< −12.7	–16	5.7 @ 1.8 V[c]	0.18 CMOS	2008
This work	±0.45 (3.0–5.0)	3.2–5.5 (2.2–5.0)	2.5–5.5	13.2[b]	< –13	–11.7	17.2 @ 1.8 V (8.6 mW for half circuit)	0.18 CMOS	2009

[a] With external inductors. [b] Approximately 6 dB loss due to output buffer. [c] Single-ended topology.

the imprecision of the transistor's noise model at high frequencies.

Figure 15 gives the measured P_{1dB} with a value of –15.9 to –11.7 dBm across 3–5 GHz which shows the large signal processing ability of the circuit.

Table 1 summarizes the performance of the proposed CMOS UWB LNA, and comparisons with recently reported designs are shown.

5. Conclusion

A 3–5 GHz broadband flat gain resistive-feedback low-noise amplifier (LNA) is designed and analyzed. In this design a method to realize flat gain is introduced. Serial and shunt peaking techniques applied to a resistive feedback topology make broadband input matching and a large GBW feasible. The measured maximum power gain is 13.2 dB with a good gain flatness of ±0.45 dB across 3–5 GHz and the minimum noise figure is 3.2 dB. The circuit shows an excellent input matching characteristic with the measured S_{11} below –13 dB. The input referred 1-dB compression point (IP1dB) is –11.7 dBm at 5 GHz. The core circuit consumes 9.6 mA current from a supply of 1.8 V.

References

[1] Siwiak K, Withington P, Phelan S. Ultra-wide band radio: the emergence of an important new technology. IEEE VTC, 2001

[2] Andersson S, Svensson C, Drugge O. Wideband LNA for a multistandard wireless receiver in 0.18 μm CMOS. Proc ESSCIRC, 2003: 655

[3] Kim C W, Kang M S, Anh P T, et al. An ultra-wideband COMS low noise amplifier for 3–5 GHz UWB system. IEEE J Solid-State Circuits, 2005, 40(2): 544

[4] Bevilacqua A, Niknejad A M. An ultrawideband CMOS LNA for 3.1–10.6 GHz wireless receiver. IEEE ISSCC Dig Tech Paper, 2004: 382

[5] Reiha M T, Long J R. A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS. IEEE J Solid-State Circuits, 2007, 42(5): 1023

[6] Liao C F, Liu S I. A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers. JSSC, 2007, 42: 329

[7] Chen Y J, Huang Y I. Development of integrated broadband CMOS low noise amplifiers. Circuits and Systems I, 2007: 2120

[8] Lee T H. The design of CMOS radio frequency integrated circuits. Cambridge, 2006

[9] Chen S C, Wang R L, Kung M L, et al. An integrated CMOS low noise amplifier for 3–5 GHz UWB applications. IEEE Conference Electron Devices and Solid-State Circuits, 2005: 225

[10] Bevilacqua A, Sandner C, Gerosa A. A fully integrated differential CMOS LNA for 3–5 GHz ultrawideband wireless receivers. IEEE Microwave and Wireless Components Letters, 2006, 16(3): 134

[11] Chang C P, Yen C C, Chuang H R. A 0.18-μm 2.4–6 GHz CMOS broadband differential LNA for WLAN and UWB receiver. 2005:

645

[12] Abidi A A, Leete J C. De-embedding the noise figure of differential amplifiers. IEEE J Solid-State Circuits, 1999, 34: 882

[13] Chang T, Chen J, Rigge L, et al. A packaged and ESD -protected inductorless 0.1–9.2 GHz wideband CMOS LNA. IEEE Microwave and Wireless Components Letters, 2008, 18(6): 416

[14] Mohan S S, Hershenson M D M, Boyd S P, et al. Bandwidth extension in CMOS with optimized on-chip inductors. IEEE J Solid-State Circuits, 2000, 35(3): 346

[15] Huang Z Y, Huang C C, Chen C C. A CMOS low-noise amplifier with impedance feedback for ultra-wideband wireless receiver system. IEEE International Symposium on VLSI-DAT, 2008: 51