Trench gate IGBT structure with floating P region

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Abstract: A new trench gate IGBT structure with a floating P region is proposed, which introduces a floating P region into the trench accumulation layer controlled IGBT (TAC-IGBT). The new structure maintains a low on-state voltage drop and large forward biased safe operating area (FBSOA) of the TAC-IGBT structure while reduces the leakage current and improves the breakdown voltage. In addition, it enlarges the short circuit safe operating area (SCSOA) of the TAC-IGBT, and is simple in fabrication and design. Simulation results indicate that, for IGBT structures with a breakdown voltage of 1200 V, the leakage current of the new trench gate IGBT structure is one order of magnitude lower than the TAC-IGBT structure and the breakdown voltage is 150 V higher than the TAC-IGBT.

Key words: TAC-IGBT; CT-IGBT; accumulation channel; floating P region; SCSOA
DOI: 10.1088/1674-4926/31/2/024003 **EEACC:** 2560

1. Introduction

The insulated gate bipolar transistor (IGBT) has become the major switching device in power electronic applications because it possesses the best feature of the bipolar and MOSFET structure[1]. The planar gate IGBT is gradually being replaced by the trench gate IGBT (T-IGBT) because the T-IGBT can provide a lower on-state voltage drop and higher latching current[2–4]. But for higher blocking voltage non-punch-through IGBTs (NPT-IGBTs), an increase of on-state voltage drop and on-state loss will be observed. Besides, the latching current level of the conventional trench gate IGBT (CT-IGBT) decreases with increasing temperature, which reduces the FBSOA of the CT-IGBT in high temperature environments[5].

Based on the planar accumulation channel field effect transistor structure proposed by Bobde and Baliga[6, 7], a trench accumulation layer controlled IGBT (TAC-IGBT) was put forward by us in ISPSD'09. The proposed device has a lower on-state voltage drop and wider FBSOA while maintaining a reasonable forward breakdown voltage[8].

2. Device structure

Cross-sections of half cell structures of the CT-IGBT and TAC-IGBT are shown in Figs. 1(a) and 1(b), respectively. The TAC-IGBT structure completely eliminates the P base region of the CT-IGBT structure, which results in a reduced latch-up effect and a larger FBSOA. Consequently, the TAC-IGBT can be operated with a lower on-state voltage drop because of the higher electron concentration in the accumulation layer near the emitter side. The TAC-IGBT, however, has a larger saturation current level and a poor SCSOA due to the higher electron concentration in the accumulation channel.

A cross-section of the half cell structure of the proposed trench gate IGBT structure with a floating P region is shown in Fig. 1(c) which relaxes the electric field at the corner of the trench bottom due to the introduction of the floating P region and a higher forward breakdown can be obtained. Additionally, as shown in Fig. 1(c), the JFET region "A", which is due to the incorporation of the floating P region, gives a smaller saturation current level and an improved SCSOA while maintaining a low forward voltage drop.

Unlike the conventional trench gate IGBT process, the P base implant and push in process is eliminated here, and emitter trench etching is performed in the TAC-IGBT process be-

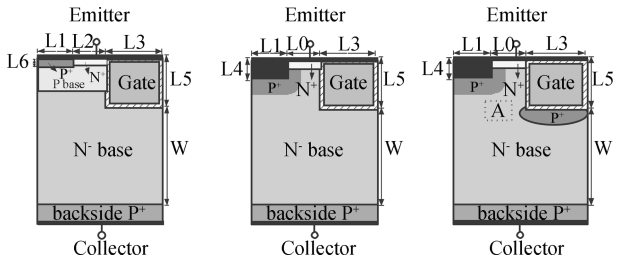

Fig. 1. Cross-section of (a) CT-IGBT, (b) TAC-IGBT, and (c) TAC-IGBT with floating P region.

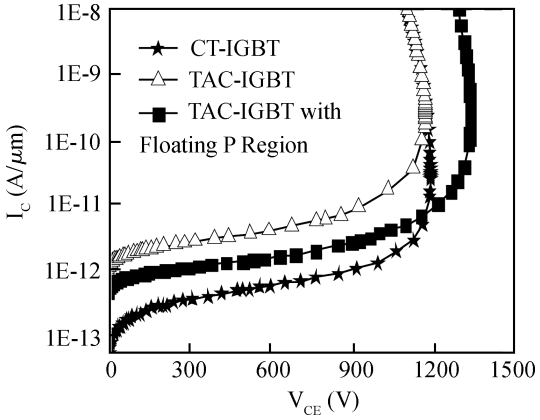

Fig. 2. Simulated forward blocking characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region.

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Received 2 August 2009, revised manuscript received 15 October 2009

Table 1. Parameters for CT-IGBT and TAC-IGBT.

Name	Explanation	Value
L_0	Gap distance	2 μm
L_1	P^+ length	1 μm
L_2	N^+ emitter length	2 μm
L_3	Gate electrode length	1 μm
L_4	Emitter trench depth	2.5 μm
L_5	Trench gate depth	9 μm
L_6	N^+ emitter depth	0.4 μm
W	N^- base thickness	169 μm
R	N^- base resistivity	55 Ω·cm
T_{ox}	Gate oxide thickness	100 nm
D_1	N^+ emitter dosage	1×10^{16} cm^{-2}
D_2	P^+ dosage	1×10^{16} cm^{-2}
D_3	P base dosage	1.5×10^{14} cm^{-2}
D_4	Backside P^+ dosage	1×10^{14} cm^{-2}

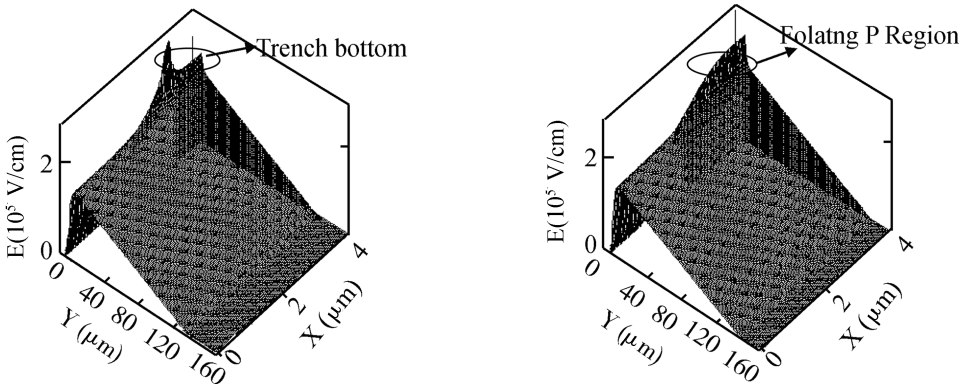

Fig. 3. 3D E-field distribution. (a) TAC-IGBT. (b) TAC-IGBT with floating P region.

fore the emitter P^+ implant process. A tilt of 7° and energy of 100 keV was used for the P^+ implant of the TAC-IGBT in this example. After being implanted, the boron ions are activated by the subsequent BPSG reflow process for 20 min at 900 ℃. The other processes for the TAC-IGBT are the same as for the conventional one. The process for the TAC-IGBT with a floating P region needs no extra masks and is almost the same as the TAC-IGBT process except that additional boron implantation is needed after trench gate etching.

3. Results and discussion

In order to gain insight into the operation of these trench gate IGBT structures, two-dimensional numerical simulations were performed by using TSUPREM IV and MEDICI[8]. A lifetime of 1 μs is used for both electrons and holes in the simulation and some other important simulation parameters are listed in Table 1.

The forward blocking characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region are shown in Fig. 2. As seen from Fig. 2, the forward breakdown voltage of the CT-IGBT and TAC-IGBT is about 1200 V while the forward breakdown voltage of the TAC-IGBT with floating P region is 1350 V, which is 150 V higher. Three-dimensional views of the electric field distributions for the TAC-IGBT and TAC-IGBT with floating P region are shown in Fig. 3. It is seen from the figure that the electric field concentration at the corner of the trench bottom is relaxed due to the presence of the floating P region and the maximum electric field is shifted from the corner of the trench bottom to the floating P region. Therefore, a larger forward breakdown voltage can be obtained for the TAC-IGBT with floating P region. Besides, a JFET region "A" which has a shielding effect for the accumulation channel is introduced by the presence of the floating P region, as illustrated in Fig. 1(c). The leakage current of the proposed TAC-IGBT with floating P region is one order of magnitude lower when compared to the TAC-IGBT with the same blocking voltage.

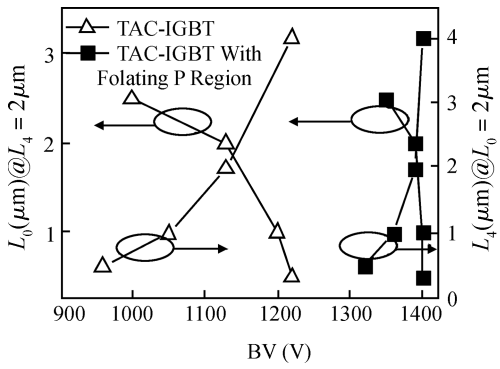

Fig. 4. Simulated forward blocking voltage of the TAC-IGBT and TAC-IGBT with floating P region with changing L_0 and L_4.

Figure 4 shows the forward blocking voltage of the TAC-IGBT and TAC-IGBT with floating P region with different val-

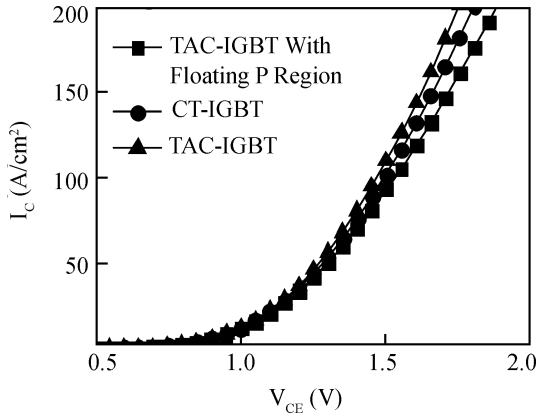

Fig. 5. On-state characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region.

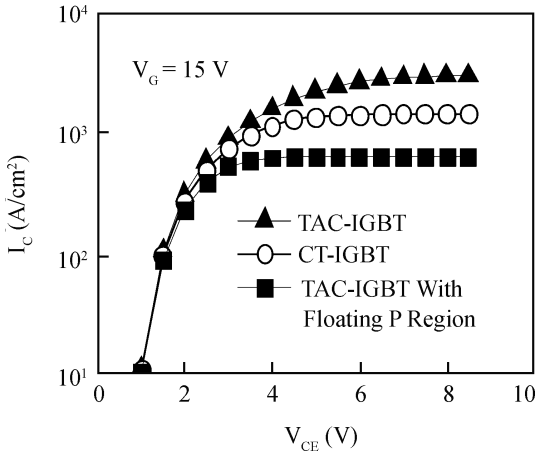

Fig. 6. I–V characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region at V_G = 15 V.

ues of L_0 and L_4. In order to obtain a reasonable blocking voltage, we need to carefully design the critical values for the gap distance L_0 and the emitter trench depth L_4 of the TAC-IGBT. The breakdown voltage will be decreased and a large leakage current will be generated if a large value of L_0 or a smaller value of L_4 is used, as indicated in Fig. 4. The proposed TAC-IGBT with floating P region has a large forward blocking voltage and lower leakage current due to the presence of the floating P region. The forward blocking voltage of this new device is less dependent on the design parameters, which make it easy and more suitable for real fabrication.

The on-state characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region are shown in Fig. 5. The figure shows that the on-state voltage drop of all three devices is around 1.5 V at 100 A/cm^2 due to the high electron concentration in the accumulation layer around the gate trench.

Figure 6 shows the I–V characteristics of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region at $V_G = 15$ V. The TAC-IGBT with floating P region has a lower saturation current level due to the existence of the JFET region "A", the resistance of which will increase when increasing the collector voltage. The saturation current densities of the CT-IGBT, TAC-IGBT and TAC-IGBT with floating P region under the same conditions are 1600 A/cm^2, 3000 A/cm^2 and 600 A/cm^2, respectively. Thus, a large short circuit safe operation area (SCSOA) will be obtained for the TAC-IGBT with floating P region due to the JFET effect between the P^+ and floating P region.

4. Conclusion

A new trench gate IGBT structure with a floating P region is proposed in this paper, which introduces a floating P region into the TAC-IGBT structure. The new structure maintains the low on-state voltage drop and large FBSOA of the TAC-IGBT. Results show that the floating P region is very effective in reducing the leakage current and improving the forward blocking voltage of the TAC-IGBT structure. In addition, a large SCSOA can be acquired due to the JFET effect created by introducing the floating P region. It is also simple and more flexible in terms of designing this new device.

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