Design of 20–44 GHz broadband doubler MMIC

Li Qin(李芹)†, Wang Zhigong(王志功), and Li Wei(李伟)

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: This paper presents the design and performance of a broadband millimeter-wave frequency doubler MMIC using active 0.15 μm GaAs PHEMT and operating at output frequencies from 20 to 44 GHz. This chip is composed of a single ended-into differential-out active Balun, balanced FETs in push-push configuration, and a distributed amplifier. The MMIC doubler exhibits more than 4 dB conversion gain with 12 dBm of output power, and the fundamental frequency suppression is typically −20 dBc up to 44 GHz. The MMIC works at $V_{DD} = 3.5$ V, $V_{SS} = -3.5$ V, $I_d = 200$ mA and the chip size is 1.5×1.8 mm^2.

Key words: frequency doubler; active Balun; distributed amplifier
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1. Introduction

The strong demand for high-speed wireless applications has stimulated the development of low power, broadband and compact millimeter-wave wireless equipment. A frequency doubler is a key component to realize the transmitter and the local part. Most single-ended transistor-based doublers have been reported in Refs. [1–3]. This topology exhibits compact size, high conversion loss, narrow bandwidth and requires some buffer amplifier stages. Compared to single-ended designs, a balanced doubler topology offers the potential of superior odd-harmonic suppression and broadband performance[4, 5]. However, the performance of balanced doublers is limited by the hybrids or Balun which usually occupy a large chip area and have insertion loss of more than 3 dB[6].

In this paper, a compact configuration of frequency doubler is presented. Thanks to a differential PHEMT structure and the distributed amplifier, the doubler exhibits broadband characteristics with an active frequency range, from 20 to 44 GHz. Experimental results show the doubler achieves more than 4 dB conversion gain and 15 dB fundamental frequency suppression (FFS) over 20–44 GHz.

2. Analysis of balanced doubler operation

The basic configuration of the balanced frequency doubler is shown in Fig. 1. It consists of two identical transistors and a 180° hybrid. The I–V relationship of the transistor can be expressed by a Taylor series[7]:

$$i(t) \cong A_0 + A_1 V_{gs}(t) + A_2 V_{gs}^2(t) + A_3 V_{gs}^3(t) + \cdots, \quad (1)$$

where V_{gs}(t) is the gate–source input voltage of each transistor containing DC and AC components.

Considering the hybrid characteristics, the input voltage of the transistors can be expressed as:

$$\begin{cases} V_{gs1} = V_{g01} + a_0 \cos(\omega_0 t), \\ V_{gs2} = V_{g02} + a_0 k \cos(\omega_0 t + 180° + \varphi(\omega_0)), \end{cases} \quad (2)$$

where $k(\omega)$ and $\varphi(\omega)$ are amplitude unbalance and phase unbalance between the two output of the hybrid. Combining Eqs. (1) and (2), the total current spectrums $I_t(\omega)$ are deduced. It is found that the output power of the fundamental frequency is proportional to[8]:

$$P^1(\omega_0) \propto P_{in}(\omega_0) A^2(V_{g0})[1 + k^2(\omega_0) - 2k(\omega_0)\cos\varphi(\omega_0)], \quad (3)$$

where $P_{in}(\omega) = 2a_0^2$ is the power input to the doubler and $A(V_{g0}) = A_1/2 + A_2 V_{g0}$ is a constant depending from the transistors and their bias.

The fundamental-frequency rejection defined as the ratio between the input power and the output power of the fundamental frequency can be expressed in decibels as:

$$S_{0dB}(\omega_0) = -A_{dB} - 10\lg[1 + k^2(\omega_0) - 2k(\omega_0)\cos\varphi(\omega_0)], \quad (4)$$

where $A_{dB} = 20\lg(\mathrm{abs}(A))$.

In the same way, the output power of the second harmonic can be deduced as follows[8]:

$$P^2(\omega_0) = \frac{P_{max}^2(\omega_0)}{4\left[1 + k^4(\omega_0) + 2k^2(\omega_0)\cos 2\varphi(\omega_0)\right]}. \quad (5)$$

Equation (4) shows that the fundamental-frequency rejection is highly dependent on the phase and amplitude unbalance

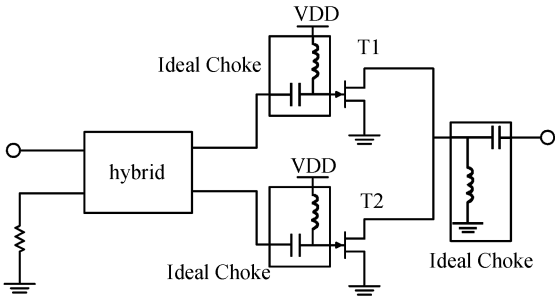

Fig. 1. Basic configuration of a balanced active doubler.

† Corresponding author. Email: liqin_iroi@seu.edu.cn
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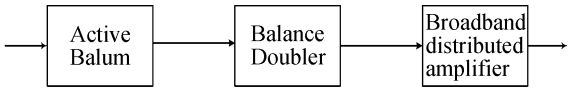

Fig. 2. Configuration of the broadband doubler.

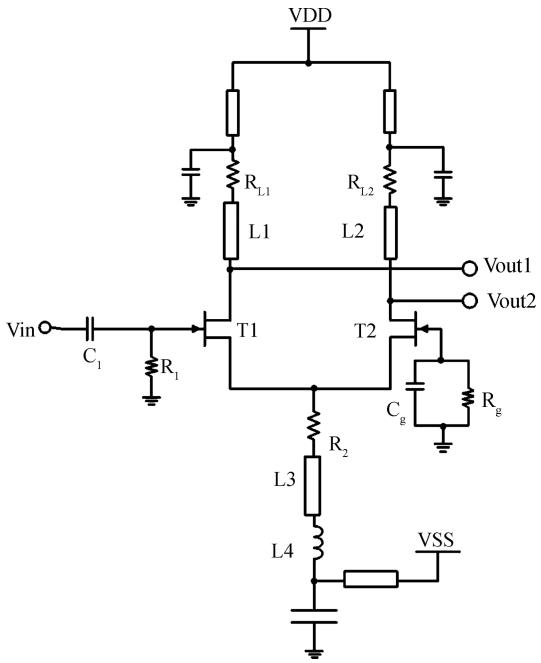

Fig. 3. Detail schematic diagram of active Balun.

of the hybrid. Infinite frequency rejection is achieved when both the amplitude and phase of the hybrid are balanced. As shown in Eq. (5), the output power of the second harmonics is at a maximum when both amplitude and phase of the hybrid are balanced. However, it is not strongly affected by the performance of the hybrid so its degradation with frequency is expected to be mainly due to input and output mismatching.

3. Circuit design

The top simplified configuration of the doubler is shown in Fig. 2. An active Balun comprising a differential amplifier is used in this MMIC to reduce MMIC size and increase conversion gain. A balanced device topology consisting of a pair of 2×25 μm PHEMTs is used to produce the doubling action. This topology has inherently good fundamental and odd harmonic rejection capability. The bandwidth of such topology could be made quite large if a proper Balun is designed. The last part of this MMIC, distributed amplifier works as a medium power amplifier to output the second harmonics to more than 12 dBm.

The schematic diagram of the active Balun is presented in Fig. 3. It consists of a differential pair comprising two 2×50 μm PHEMT devices with a series resistive-inductive load and single-ended feed. The input fundamental signal is split into the two balanced ports of 'Vout1' and 'Vout2', with identical power and a phase difference of 180°. However, this active Balun loses its amplitude and phase balance as frequency increases[9]. The reason for imbalance of amplitude and phase is that the gate of T2 is directly ac grounded while the gate of

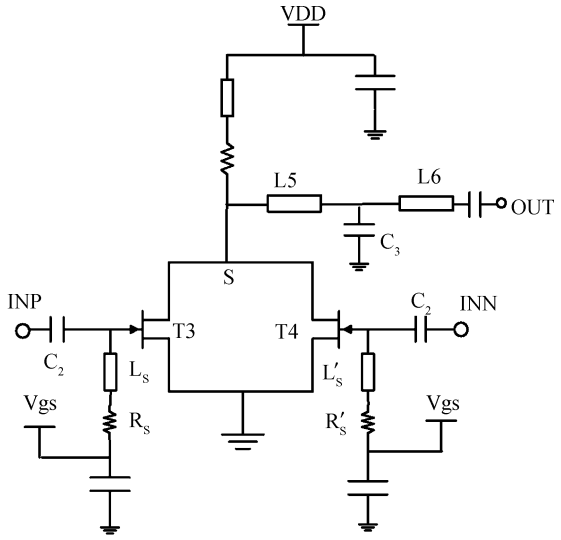

Fig. 4. Schematic of balanced doubler.

T1 connects some sort of network. As the frequency increases, the effect of this mismatch shows up at the outputs of 'T1' and 'T2' and causes amplitude and phase mismatch. The imbalance of the Balun is improved by asymmetric output loading of the differential amplifier that will be described in the next section.

The schematic of a balanced doubler is shown in Fig. 4. The drains of T3 and T4 are connected together. Since the input signals from the Balun's output have equal amplitude and are anti-phase, the second harmonic signal will in-phase combine and the fundamental signal will 180° out-of-phase cancel in the RF output port. T3 and T4 are biased near the pinch-off region, –1.4 V, where the nonlinearity of trans-conductance versus gate-to-source voltage is used for frequency doubling. The L–C network consisting of L5, L6 and C_3 is designed to provide as much suppression as possible for fundamental frequency and also to provide a match at the second harmonic frequency.

Any imbalance from Balun would develop a finite voltage at node 'S' (Fig. 4) and it would no longer be a virtual ground point. This will allow the passing of the fundamental signal and other odd harmonics to the output port, which will degrade suppression and conversion loss. To minimize this problem, the R_S–L_S and R'_S–L'_S serial network are no longer the same value and have been optimized to minimize amplitude and phase mismatch in feed waveforms from T1 and T2. The simulated waveforms at 20 GHz from the active Balun at node 'Vout1' and 'Vout2' are shown in Fig. 5. Figure 5(a) shows asymmetrical waveform before the circuit was optimized. Figure 5(b) shows the optimized circuit symmetries the waveform at node 'Vout1' & 'Vout2'.

The last part of this design is a distributed amplifier working as a broadband buffer. The detailed schematic of the distributed amplifier is shown in Fig. 6. It is composed of two cascaded stages and each stage consists of three active devices. The input signal travels down to the transmission lines and goes through the transistor. It is finally absorbed by the gate termination resistor. The output signal passes the active devices and transmits to the output port. Some of the backward wave of the

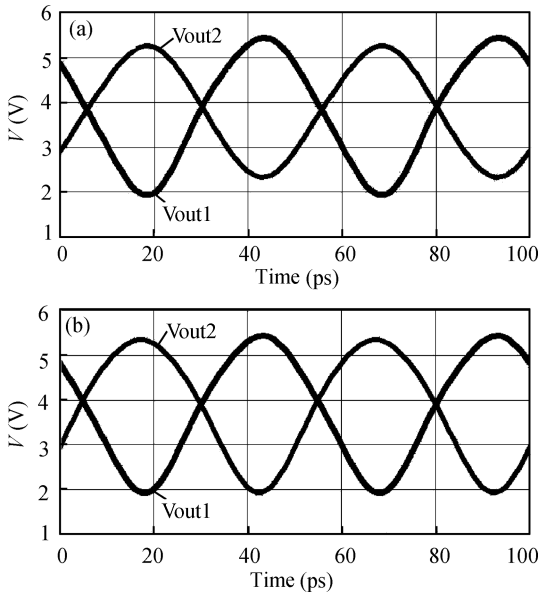

Fig. 5. (a) Asymmetrical waveform at node Vout1 & Vout2. (b) Symmetrized waveform at node Vout1 & Vout2.

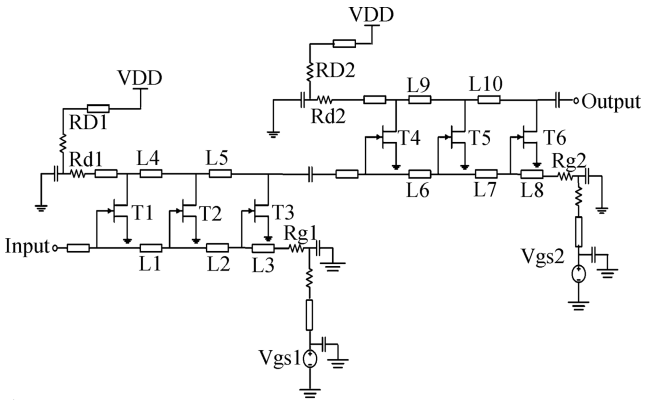

Fig. 6. Detail schematic of distributed amplifier.

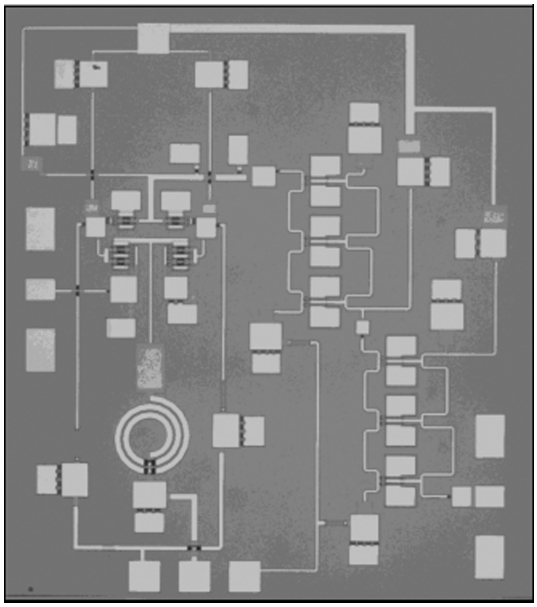

Fig. 7. Microscope photo of broadband doubler.

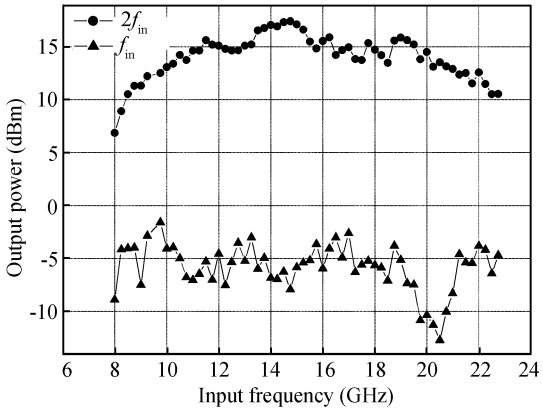

Fig. 8. Output power of the fundamental and the second harmonic versus frequency.

output signal will reflect to the circuit output due to the drain termination resistor. The gain of the cascaded distributed amplifier can be expressed as[10]:

$$G = \frac{n^2 g_{\mathrm{m}}^2 R_{\mathrm{gL}} R_{\mathrm{dL}}}{4}, \tag{6}$$

where R_{gL} and R_{dL} are the characteristic impedance of the gate and drain lines respectively.

4. Circuit fabrication

To design the broadband frequency doubler, the layout was verified using Agilent ADS Momentum and Cadence Virtuso design environment software. The MMIC fabrication is based on WIN Semiconductors' 0.15-μm, high-power, 6-inch InGaAs/AlGaAs/GaAs pseudomorphic HEMT process (PP15-20). This process exhibits a peak trans-conductance g_{m} = 495 mS/mm, a nominal transit frequency f_{t} = 85 GHz and I_{dss} = 500 mA/mm on a 100-μm substrate with 50 Ω/□ thin-film resistors and 400 pF/mm^2 metal–insulator–metal capacitors. There are two metal layers available in this process. The wafer is thinned to 4 mil for the gold planting of backside and reactive ion etching via-holes are used for dc grounding. A photograph of the fabricated frequency doubler is shown in Fig. 7. The chip dimension is reduced to 1.5 × 1.8 mm^2.

5. Circuit performance

The fabricated MMIC doubler was attached on carrier plates for testing. The measurements of signals were provided by the coplanar GSG on-wafer probes measurement system based on the HP8564E spectrum analyzer. The losses of the probes and cables were also calibrated by the PNA E8364A network analyzer.

The V_{DD} is +3.5 V and the V_{SS} = –3.5 V. The DC current is about 200 mA and P_{in} = +8 dBm. The measured output power of 2nd harmonic ($2f_{\mathrm{in}}$) and fundamental (f_{in}) as functions of the fundamental frequency, are shown in Fig. 8. The P_{out} of the 2nd harmonic varies from +12 to +17.2 dBm from 20 to 44 GHz and the conversion gain varies from 4 to 9 dB during the whole bandwidth. Figure 9 shows the fundamen-

Table 1. Comparison of published broadband FET/HEMT MMIC doublers.

Reference	Technology	Output frequency (GHz)	G_c (dB)	P_{out} (dBm)	Chip area (mm^2)	Fundamental suppression (dBc)
Ref. [11]	0.15-μm GaAs PHEMT	30–50	−7 to −5	3–5	1.5	9–25
Ref. [12]	0.12-μm GaAs PHEMT	22–42	−10 to −2	3–9	2	13.4–26
Ref. [13]	0.1-μm InP HEMT	54–70	−5 to −2	NA	0.89	22–30.5
Ref. [14]	0.25-μm GaAs HEMT	20–40	–12	NA	2.25	20
This work	0.15-μm GaAs PHEMT	20–44	4–9	12–17	2.7	15–26

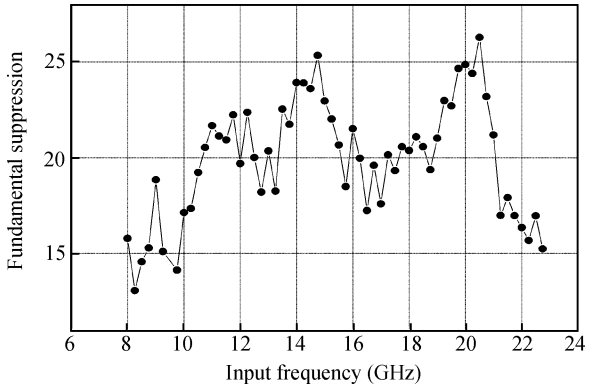

Fig. 9. Fundamental suppression versus the input frequency.

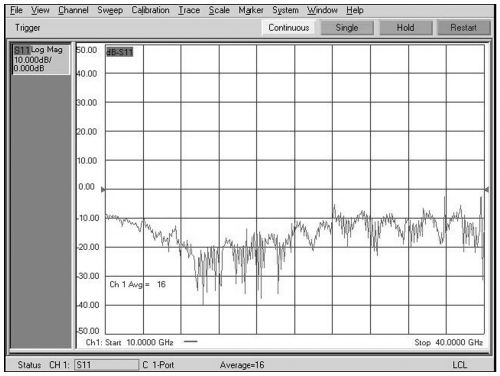

Fig. 10. Output return loss of doubler.

tal suppression of the MMIC as a function of input frequency. Fundamental suppression is better than 17 dBc from 20 to 44 GHz. The degradation in fundamental frequency suppression after 40 GHz is caused by an active Balun performance as its amplitude and phase balance degrades beyond 40 GHz and also due to overlapping input and output frequencies (f_{in} and $2f_{in}$). It can be seen in Fig. 10 that the output return loss is less than about –10 dB during all frequency bands.

6. Conclusion

A compact frequency doubler using an active Balun, balanced amplifiers and a distributed amplifier has been described in this paper. From 20 to 44 GHz, the MMIC can provide a broadband millimeter signal of more than 12 dBm. The conversion gain is 4–9 dB with an input power of 8 dBm and the fundamental suppression is better than 15 dBc, at input frequencies from 10 to 22 GHz with a compact chip size of only 1.5×1.8 mm^2. A comparison of the frequency doubler to the previously reported works is summarized in Table 1. The proposed doubler has the highest conversion gain and the widest bandwidth among the reported doublers.

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