A 1.4-V 25-mW 600-MS/s 6-bit folding and interpolating ADC in 0.13-μm CMOS*

Lin Li(林俪), Ren Junyan(任俊彦)†, and Ye Fan(叶凡)

(ASIC and System State Key Laboratory, Fudan University, Shanghai 201203, China)

Abstract: A 600-MSample/s 6-bit folding and interpolating analog-to-digital converter (ADC) is presented. This ADC with single track-and-hold (T/H) circuits is based on cascaded folding amplifiers and input-connection-improved active interpolating amplifiers. The prototype ADC achieves 5.55 bits of the effective number of bits (ENOB) and 47.84 dB of the spurious free dynamic range (SFDR) at 10-MHz input and 4.3 bit of ENOB and 35.65 dB of SFDR at 200-MHz input with a 500 MS/s sampling rate; it achieves 5.48 bit of ENOB and 43.52 dB of SFDR at 1-MHz input and 4.66 bit of ENOB and 39.56 dB of SFDR at 30.1-MHz input with a 600-MS/s sampling rate. This ADC has a total power consumption of 25 mW from a 1.4 V supply voltage and occupies 0.17 mm^2 in the 0.13-μm CMOS process.

Key words: analog-to-digital converter; cascaded folding; active interpolating
DOI: 10.1088/1674-4926/31/2/025009 **EEACC:** 1265H; 1280; 2570D

1. Introduction

In high-speed wireless interconnect systems, like ultra-wide-band (UWB) physical layers, a high-speed ADC is required. Typically, a 6-bit resolution is adequate[1]. With the increase of speed, power consumption is getting greater and greater. But low power consumption and low supply voltage are critical for embedded and portable applications. A flash ADC is almost the fastest of all kinds of ADCs. However, its power consumption is unacceptable in low-power applications. A folding and interpolating ADC has speed benefits similar to the flash ADC but with reduced circuit complexity and power consumption. It is preferable for embedded and portable applications.

Folding and interpolating circuits are the most important part of folding and interpolating ADCs. The folding architecture can produce more than one zero-crossing, which reduces the number of comparators. The interpolating architecture can reduce the number of preamplifiers followed by folding amplifiers. There are mainly two architectures of folding amplifiers such as single-stage folding amplifiers[2] and cascaded folding amplifiers[3]. Single-stage folding architecture is suitable for high-voltage and low-speed applications, whereas cascaded folding architecture is suitable for low-voltage and high-speed applications. Cascaded folding amplifiers are adopted in the proposed ADC. A detailed analysis and optimization are presented in the paper. Resistive interpolation[2, 4] and current-mode interpolation[4, 5] mostly use interpolating architecture. However, they are both unsuitable for low-voltage application. An input-connection-improved active interpolating amplifier is presented in the paper, which is able to overcome the drawbacks of resistive interpolation and current-mode interpolation.

2. Architecture

The presented folding and interpolating ADC, shown in Fig. 1, consists of a T/H, a reference ladder, preamplifiers, folding amplifiers, active interpolating amplifiers, comparators and a digital processing block.

The T/H samples and holds the differential input analog signals, including bootstrapped switches and holding capacitances. The bootstrapped switch is able to depress the change of switch resistance influenced by the variation of input signal when the switch is on. Thus the linearity of the T/H is improved. Due to the use of T/Hs, the speed requirement of the following analog circuits is relaxed. The reference ladder is used to generate the reference voltages of the flash-type ADC. The offset-averaging resistors are used to reduce the offset caused mainly by the mismatch of the devices and the input capacitance. The cascaded folding amplifiers are used to produce folded signals, which provide more than one zero-crossing at one output. Thus the number of comparators is reduced. This is one of the most important functional modules of the ADC. Active interpolation produces more evenly spaced intermediate zero-crossings compared to existing ones. The comparators check the zero-crossings and produce a cyclic thermometer code. The digital processing block converts the cyclic thermometer code to a binary representation.

In this work, a coarse sub-ADC is used to resolve the high three bits and a fine sub-ADC is used to resolve the low three bits. According to the resolution of the coarse sub-ADC, the folding factor should be eight. The interpolating factor is related to the number of preamplifiers: the larger the interpolating factor, the smaller the number of preamplifiers. In this work, the interpolating factor is two, so thirty-three preamplifiers are used in the fine channel including two preamplifiers used to judge out-of-range. Four cascaded folding amplifiers with a folding factor of 9 are used and produce four folded signals. Between the neighboring cascaded folding amplifiers, one active interpolating amplifier is connected, as shown in Fig. 2. Four active interpolating amplifiers are used to double the folded signals. As a result, only eight comparators are enough in the

* Project supported by the National Natural Science Foundation of China (No. 90407003), the Science and Technology Commission of Shanghai Municipality (Nos. 067062003, 08XD14007), and the Shanghai-Applied Materials Research and Development Fund (No. 07SA16).

† Corresponding author. Email: jyren@fudan.edu.cn

Received 17 August 2009, revised manuscript received 10 September 2009

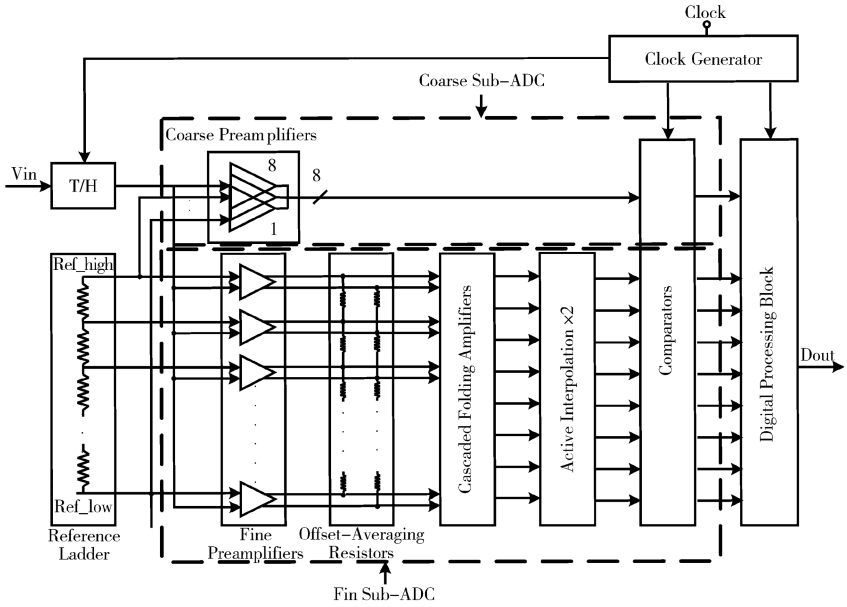

Fig. 1. Block diagram of the presented folding and interpolating ADC.

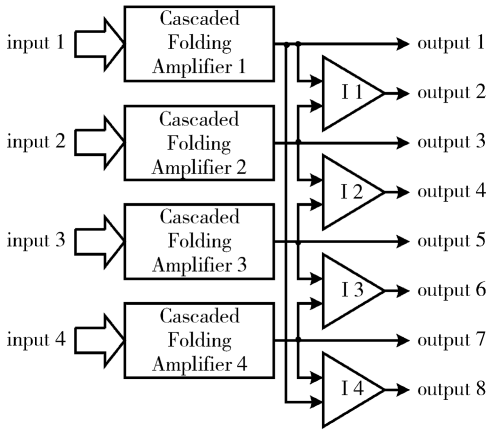

Fig. 2. Block diagram of the folding and interpolating architecture.

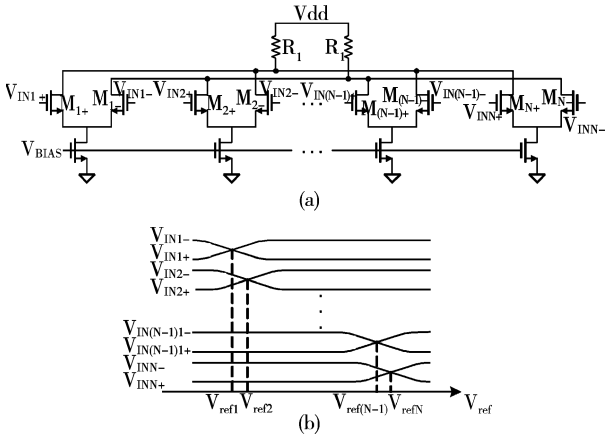

Fig. 3. (a) Single-stage folding amplifier; (b) Probable inputs of the single-stage amplifier at low supply voltage.

fine sub-ADC. The outputs of the comparators are cyclic thermometer code. Thus eight outputs can provide 4-bit information, that is, the lowest bit of the coarse sub-ADC can be decided by the fine sub-ADC. In order to achieve bit synchronization[6] between two sub-ADCs, dummy preamplifiers are used in the coarse sub-ADC.

3. Circuit implementation

3.1. Cascaded folding amplifier

The single-stage differential folding amplifier[2] with a folding factor of N used in most folding and interpolating ADCs is shown in Fig. 3(a). It consists of N input differential pairs $(W/L)_1$, N biasing current sources (I_1) and a pair of resistors (R_1). The voltage drop of the load resistors (V_R) is

$$V_R = \frac{1}{2} N I_1 R_1. \tag{1}$$

With the scaling-down of voltage supply, $I_1 R_1$ should not be large, or the differential input transistors will work in the triode region. Thus, voltage gain (A_{v1}) is limited, which is proportional to $R_1\sqrt{I_1}$ with the same process and width–length ratio. Due to the frequency multiplication effect, the frequency of the folded signals is proportional to N. The -3 dB bandwidth of single-stage folding architecture is proportional to the reciprocal of the output capacitance. A high folding factor needs a large -3 dB bandwidth, but results in high parasitic capacitance. Thus, the bandwidth requirement is hardly met. Besides, the reference voltage difference between two consecutive differential pairs decreases with the scaling-down of the supply voltage. The working zones of consecutive differential pairs would overlap. When V_{IN1+} is equal to V_{IN1-}, as shown in Fig. 3(b), the currents flowing through the left R_1 and the right R_1 are respectively

$$I_{left} = (1-\alpha) I_1 + \left(\frac{N}{2} - 1\right) I_1, \tag{2}$$

$$I_{right} = \alpha I_1 + \frac{N}{2} I_1. \tag{3}$$

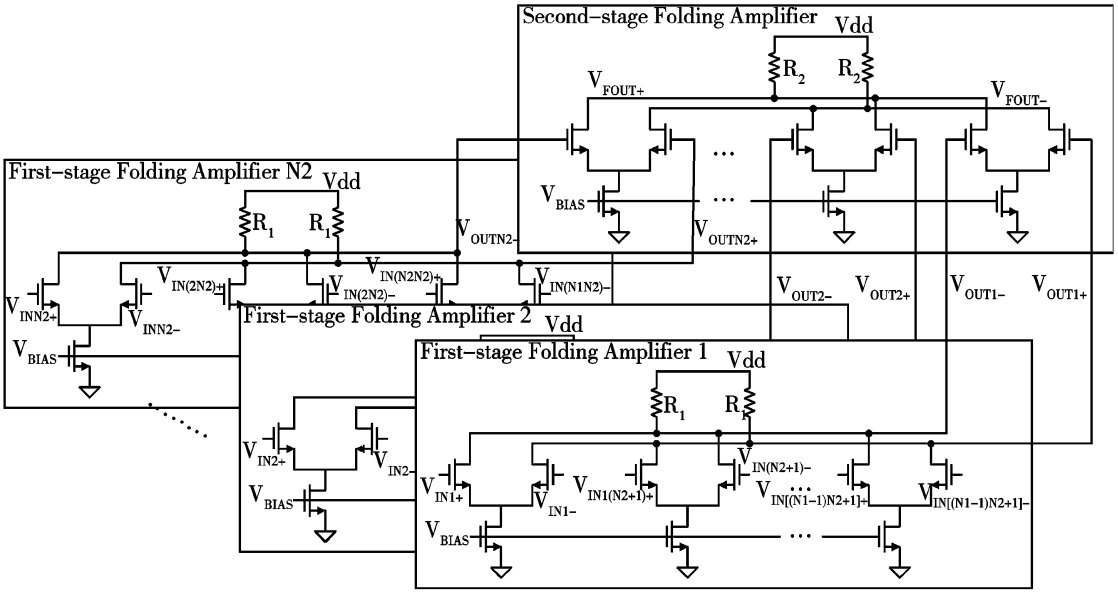

Fig. 4. Schematic of two-stage cascaded folding amplifier.

If all the bias current flows through M2−($\alpha = 0$), I_{left} is equal to I_{right}. A correct zero-crossing is generated. However, as shown in Fig. 3(b), some bias current flows through M2+ ($\alpha > 0$). Thus, I_{left} is smaller than I_{right}. A wrong zero-crossing is generated.

In low-voltage and high-speed applications, single-stage folding architecture has gain and speed limitations and will generate wrong zero-crossings. A cascaded folding amplifier overcoming these disadvantages is used in this work. According to Ref. [3], a differential cascaded folding architecture with a folding factor of $N_1 N_2$ is proposed, as shown in Fig. 4. It consists of N_2 folding amplifiers in the first stage and one folding amplifier in the second stage. Each first-stage folding amplifier has N_1 input differential pairs $(W/L)_{2.1}$, N_1 biasing current sources ($I_{2.1}$) and a pair of load resistors ($R_{2.1}$), and the second-stage folding amplifier has N_2 input differential pairs $(W/L)_{2.2}$, N_2 biasing current sources ($I_{2.2}$) and a pair of load resistors ($R_{2.2}$). The signal of each first-stage folding amplifier is folded N_1 times and the phase difference between these N_2 folded signals is $360°/N_2$. At the output of the second folding amplifier, the signal is folded $N_1 N_2$ times.

In this structure, $I_{2.1}R_{2.1}$ and $I_{2.2}R_{2.2}$ can both be larger. Its voltage gain (A_{v2}) can be expressed as

$$A_{\text{v2}} = k' R_{2.1} R_{2.2} \sqrt{I_{2.1} I_{2.2} \left(\frac{W}{L}\right)_{2.1} \left(\frac{W}{L}\right)_{2.2}}, \quad (4)$$

where k' is a constant related to the process.

It is much easier to achieve enough gain to meet the requirement of the system. The capacitances of the critical nodes in a cascaded folding amplifier are much smaller and the necessary bandwidth of the first-stage folding amplifiers is smaller. The reference voltage difference between two adjacent differential pairs is N_2 times larger by connecting every N_2 input to the same folding amplifier. Non-overlapping g_{m}-curves of differential pairs reduce the wrong zero-crossings.

The gain–bandwidth (GBW) of the cascaded folding amplifier is

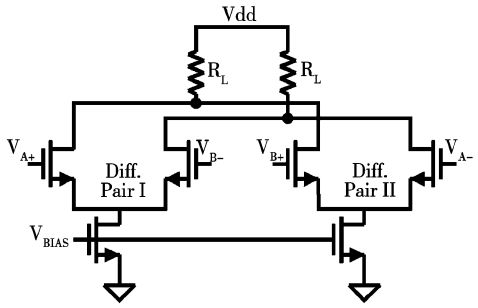

Fig. 5. Input-connection-improved active interpolating amplifier.

$$\text{GBW} = \frac{k'}{1.1\pi} \sqrt{\left(\frac{W}{L}\right)_{2.1} \left(\frac{W}{L}\right)_{2.2}} \sqrt{\frac{V_{\text{R1}} V_{\text{R2}}}{N_1 N_2}} \times \left(\frac{C_1^2}{\alpha_{\text{R}}} + \alpha_{\text{R}} C_2^2\right)^{-\frac{1}{2}}, \quad (5)$$

where α_{R} is the ratio of the load resistors of the second-stage folding amplifier to that of the first-stage one, C_1 and C_2 are the load capacitances of the first-stage and the second-stage folding amplifiers respectively. When α_{R} is equal to the ratio of C_1 and C_2, GBW reaches the maximum. According to Eq. (5), the cascaded folding amplifier can be optimized. However, increasing the folding factor ($N_1 N_2$) still reduces GBW.

In this work, $N_1 N_2 = 9$, $C_1 \approx C_2$, $\Delta V_{\text{C1}} = \Delta V_{\text{C2}}$. The simulation results show that the cascaded folding amplifier achieves a GBW of 1.5 GHz and a gain of 7.43 dB.

3.2. Input-connection-improved active interpolating amplifier

Most published folding and interpolating ADCs use resistive interpolation[2, 4] and current-mode interpolation[5, 6]. These two kinds of interpolation have two drawbacks: no contribution to the gain and high requirement on linearity. A low

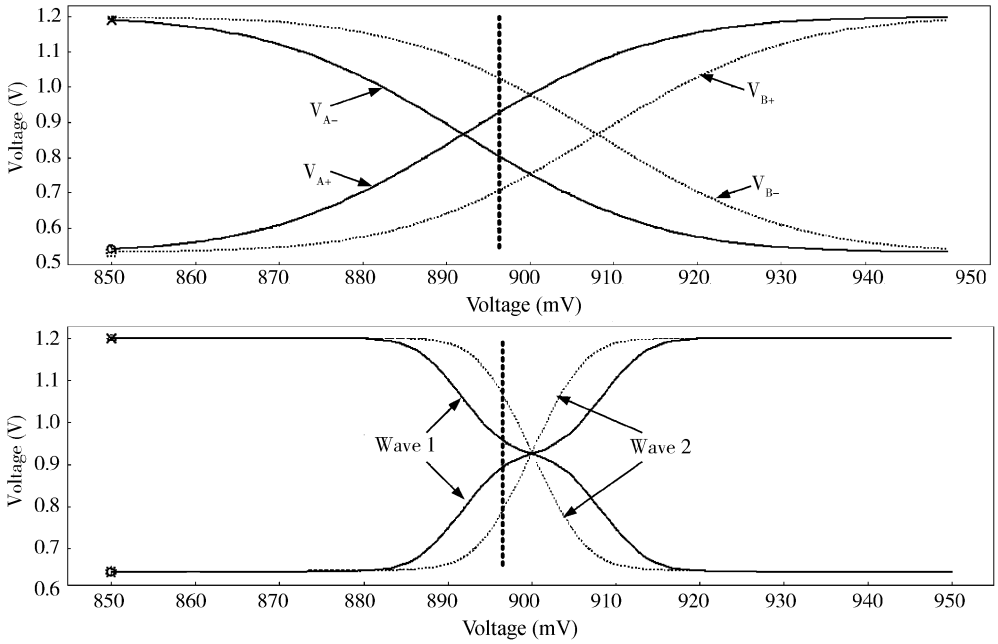

Fig. 6. (a) Input signals of active interpolating amplifiers; (b) Output waves of active interpolating amplifiers.

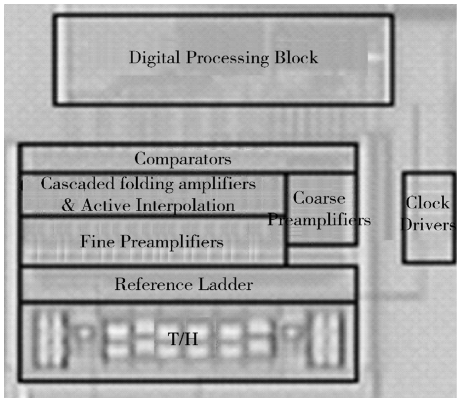

Fig. 7. Layout of the 6-bit 600-MSample/s folding and interpolating ADC.

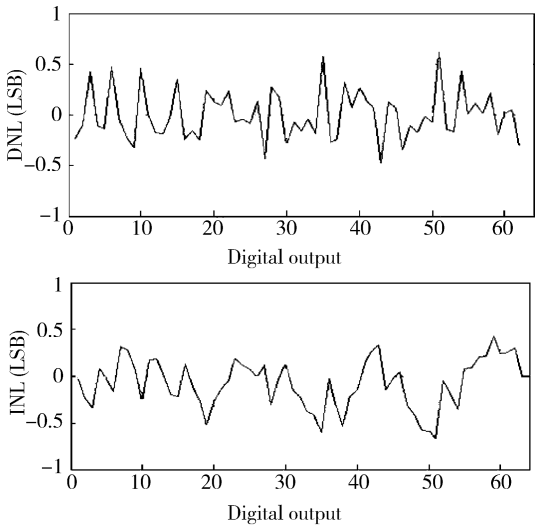

Fig. 8. Measured DNL/INL performance.

supply voltage results in low gain and a small input linear range. In this paper, an input-connection-improved active interpolating amplifier is proposed to cope with these circumstances.

An input-connection-improved active interpolating amplifier is shown in Fig. 5. It provides signal gain to overcome offsets from the comparators.

Signals v_{A+}/v_{B-} and v_{B+}/v_{A-} are respectively connected to differential pairs I and II. Signals v_{A+}/v_{A-} and v_{B+}/v_{B-} are the differential output signals from the neighboring folding amplifiers. This kind of active interpolating amplifier not only provides voltage gain to the signals, but also improves the input linear range.

In the linear working zone, shown in Fig. 6(a), the difference of v_{A+} and v_{B+} is equal to the difference of v_{A-} and v_{B-}, that is,

$$v_{A+} - v_{B+} = v_{B-} - v_{A-}. \tag{6}$$

Thus,

$$v_{A+} - v_{B-} = v_{B+} - v_{A-}. \tag{7}$$

The differential voltages of both differential pairs are the same, and are always smaller than the difference of v_{A+} and v_{A-} or v_{B+} and v_{B-}. Large differential signals will not appear at the inputs of the amplifiers. The input-connection-improved active interpolating amplifier has a good linearity performance. As shown in Fig. 6(b), the solid lines are output waves of the active interpolating amplifier without improving the input connection and the broken lines are output waves of the active interpolating amplifier with an improved input connection. The linearity of wave 1 is obviously worse than that of wave 2 near the zero-crossing. With the increase of input differential voltages, a 'dead area' will appear at the outputs of the ac-

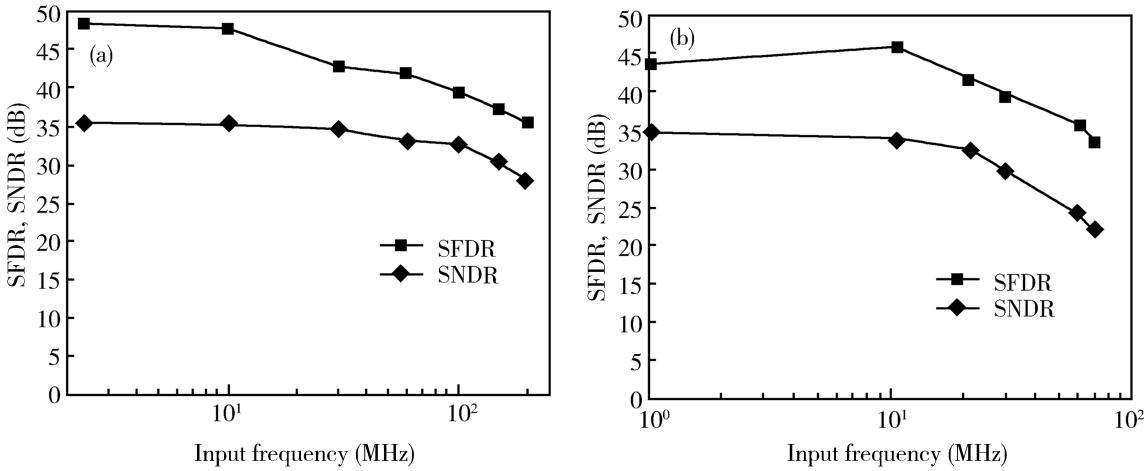

Fig. 9. (a) SNDR and SFDR versus input frequency at 500 MS/s. (b) SNDR and SFDR versus. input frequency at 600 MS/s.

Table 1. Comparison of high-speed low-resolution CMOS folding and interpolating ADCs.

Parameter	Ref. [5]	Ref. [6]	Ref. [7]	This work
Technology	0.5-μm BiCMOS (CMOS only)	0.35-μm 2P4M CMOS	0.18-μm 1P4M CMOS	0.13-μm 1P8M CMOS
Resolution (bit)	6	7	8	6
Power supply (V)	3.2	3.3	3.3/1.8	1.4
Sampling rate (MS/s)	400	300	600	600
Power consumption (mW)	200	200 (excluding SH)	200	25
DNL/INL (LSB)	—	0.6/1	0.4/0.8	0.62/0.66
SNDR (dB)	32.9 @ 1 MHz, 450 MS/s	38 @ 60 MHz, 300 MS/s	43.9 @ 5 MHz, 600 MS/s	35.2 @ 10 MHz, 500 MS/s 33.3 @ 60 MHz, 500 MS/s 34 @ 5 MHz, 600 MS/s
Active area (mm^2)	0.6	1.2	0.2	0.17

Table 2. Performance summary.

Parameter	Value
Technology	0.13-μm 1P8M CMOS
Resolution	6 bit
Power supply	1.4 V
Sampling rate	600 MS/s
Power consumption	25 mW
DNL/INL	0.62/0.66 LSB
SNDR/SFDR	27.65/35.65 dB @ 200 MHz, 500 MS/s 29.81/39.56 dB @ 30.1 MHz, 600 MS/s
ENOB @ DC	5.55 bit @ 500 MS/s 5.48 bit @ 600 MS/s
Active area	0.17 mm^2

tive interpolating amplifier without improving the input connection.

4. Measurement results

The circuit is fabricated in 0.13 μm CMOS technology. A die microphotograph of the ADC is presented in Fig. 7, and occupies an active area of 0.17 mm^2. Figure 8 shows DNL and INL performance for a 1-Hz input signal at 600 MS/s. The measurement results of SNDR and SFDR versus analog input frequency at a sampling rate of 500 MS/s and at a sampling rate of 600 MS/s are shown in Fig. 9. The total power dissipation is 25 mW from a 1.4 V supply. A comparison of high-speed low-resolution CMOS folding and interpolating ADCs is shown in Table 1. The dynamic and static performances of the ADCs listed in Table 1 are comparable. The measurement performances are summarized in Table 2. This work has a great power consumption advantage.

5. Conclusion

A 1.4-V 25-mW 600-MS/s 6-bit folding and interpolating ADC is implemented in this paper. It is composed of a coarse sub-ADC and a fine sub-ADC. In the fine sub-ADC, cascaded folding amplifiers and input-connection-improved active interpolating amplifiers are used. The ADC is realized in 0.13 μm CMOS technology. It features a low power consumption of 25 mW and a small area of 0.17 mm^2.

References

[1] Saberinia E, TewJik A H, Chang K C, et al. Analog to digital converter resolution of multi-band OFDM and pulsed-OFDM ultra wideband systems. IEEE Int Symp Control, Communications and Signal Processing, 2004: 787

[2] Venes A G W, van de Plassche R J. An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing. IEEE J Solid-State Circuits, 1996, 31(12): 1846

[3] Pan H, Abidi A A. Signal folding in A/D converters. IEEE Trans Circuits Syst I: Regular Papers, 2004, 51(1): 3

[4] Vorenkamp P, Roovers R. A 12-b, 60-MSample/s cascaded folding and interpolating ADC. IEEE J Solid-State Circuits, 1997, 32(12): 1876

[5] Flynn M P, Sheahan B. A 400-Msample/s, 6-b CMOS folding and interpolating ADC. IEEE J Solid-State Circuits, 1998, 33(12): 1932

[6] Li Y, Sánchez-Sinencio E. A wide input bandwidth 7-bit 300-MSample/s folding and current-mode interpolating ADC. IEEE J Solid-State Circuits, 2003, 38(8): 1405

[7] Geelen G, Paulus E. An 8b 600 MS/s 200 mW CMOS folding A/D converter using an amplifier preset technique. IEEE Int Solid-State Circuits Conf Dig Tech Papers, 2004